MYSON TECHNOLOGY

MTV312M64
(Rev 0.95)

8051 Embedded Monitor Controller Flash Type with ISP

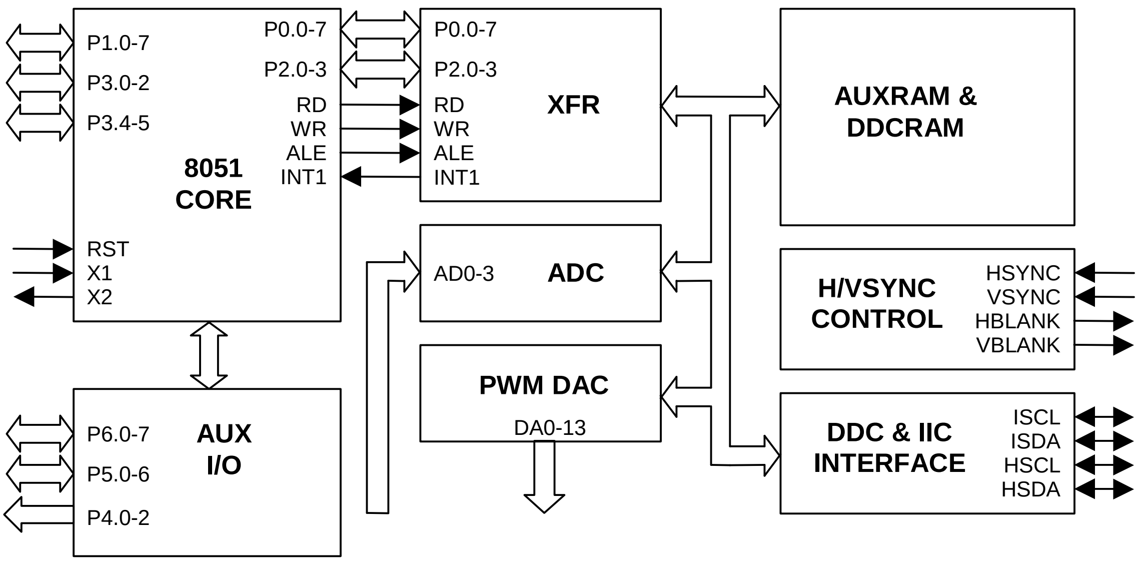
FEATURES

- 8051 core, 12MHz operating frequency with double CPU clock option.
- 0.35uM process; 5V/3.3V power supply and I/O; 3.3V core operating.
- 1024-byte RAM; 64K-byte program Flash-ROM support In System Programming (ISP).
- Maximum 14 channels of PWM DAC.
- Maximum 31 I/O pins.
- SYNC processor for composite separation/insertion, H/V polarity/frequency check and polarity adjustment.
- Built-in low power reset circuit.
- Built-in self-test pattern generator with four free-running timings.
- Compliant with VESA DDC1/2B/2Bi/2B+ standard.
- Dual slave IIC addresses; H/W auto transfer DDC1/DDC2x data.
- Single master IIC interface for internal device communication.
- Maximum 4-channel 6-bit ADC.
- Watchdog timer with programmable interval.
- 40-pin DIP, 42-pin SDIP or 44-pin PLCC package.

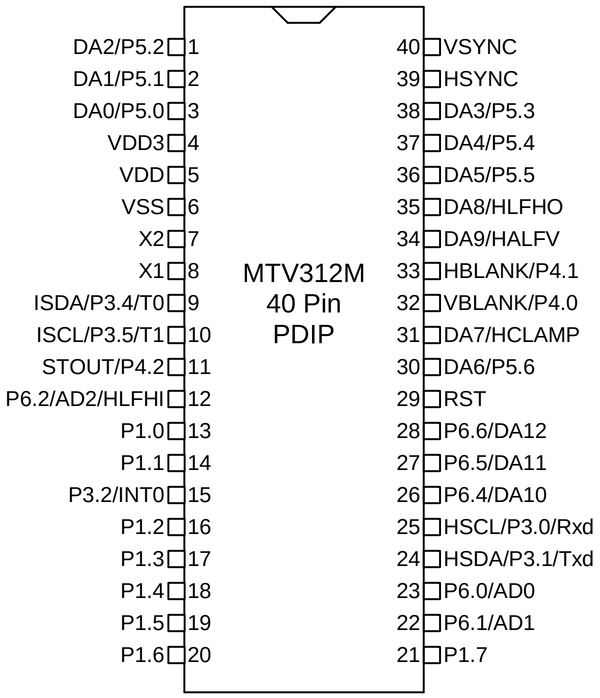
GENERAL DESCRIPTIONS

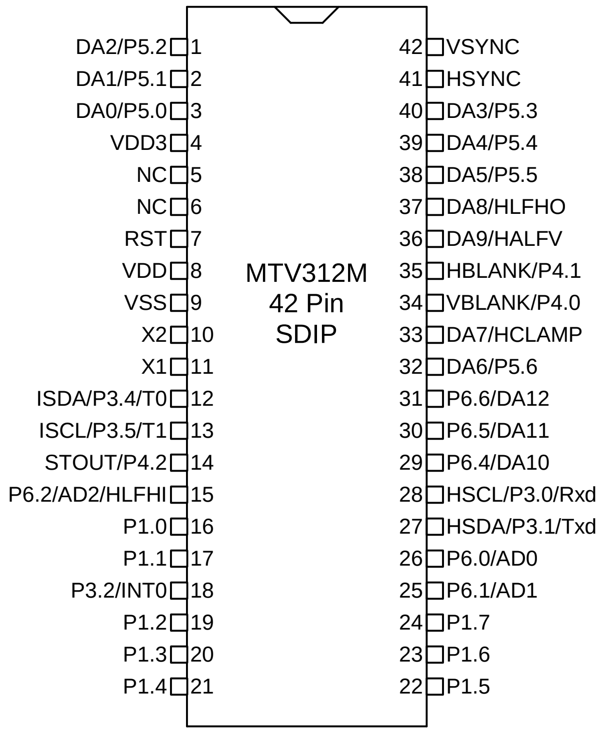
The MTV312M micro-controller is an 8051 CPU core embedded device especially tailored to CRT/LCD Monitor applications. It includes an 8051 CPU core, 1024-byte SRAM, 14 built-in PWM DACs, VESA DDC interface, 4-channel A/D converter, and a 64K-byte internal program Flash-ROM.

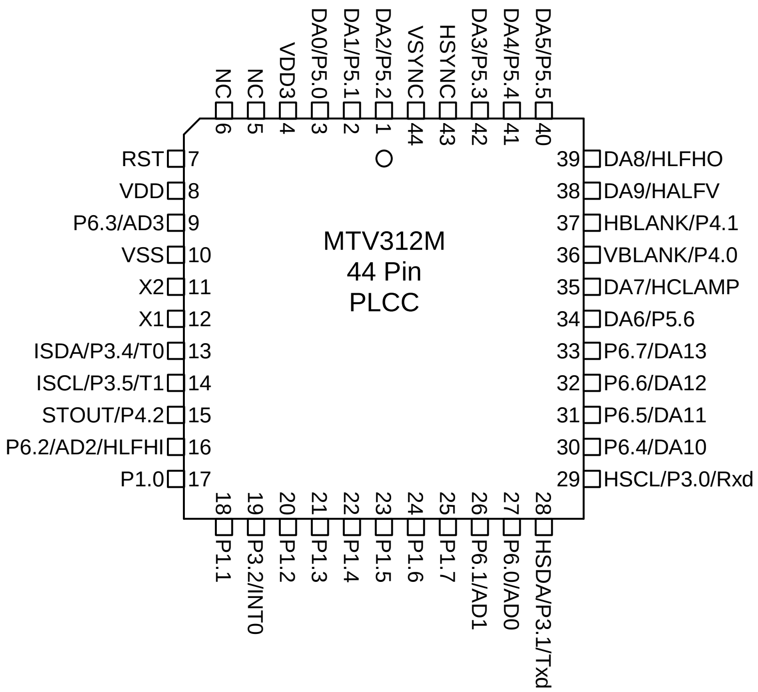
BLOCK DIAGRAM



PIN CONNECTION

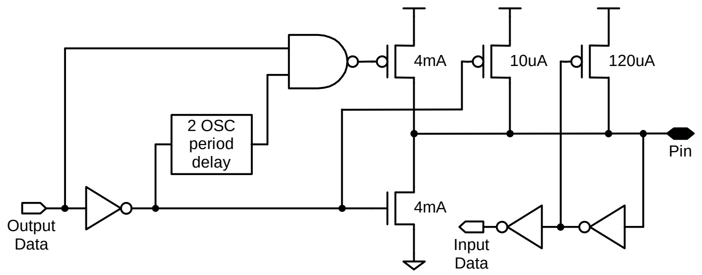




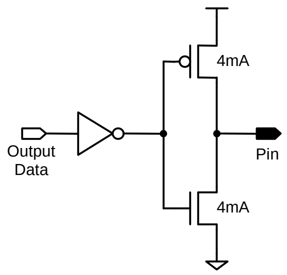


PIN CONFIGURATION

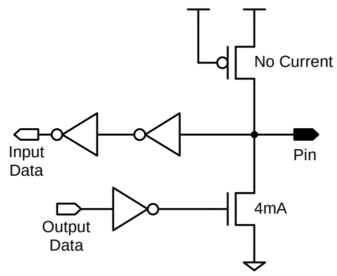
A “CMOS output pin” means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.
A “open drain pin” means it can sink at least 4mA current but only drive 10~20uA to VDD. It can be used as input or output function and needs an external pull up resistor.
A “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.



8051 Standard Pin



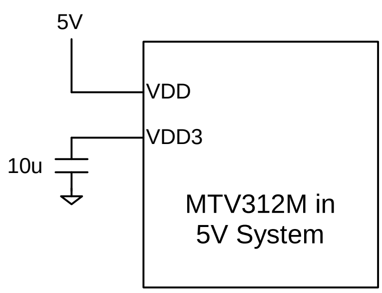
CMOS Output Pin

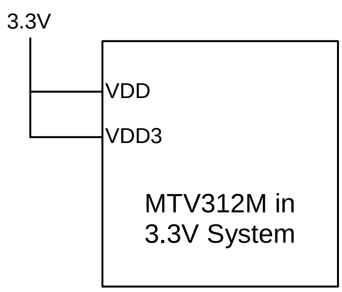


Open Drain Pin

POWER CONFIGURATION

The MTV312M can work on 5V or 3.3V power supply system. In 5V power system, the VDD pin is connected to 5V power and the VDD3 needs an external capacitor, all output pins can swing from 0~5V, input pins can accept 0~5V input range. However OSC1, OSC2 and ADC input (if selected) pins must be kept below 3.3V. In 3.3V power system, the VDD and VDD3 are connected to 3.3V power, all output pins swing from 0~3.3V, HSYNC, VSYNC and open drain pin can accept 0~5V input range, other pins must be kept below 3.3V.





PIN DESCRIPTION

Name	PIN NO.			Type	Description
	40	42	44		
VDD3	4	4	4	O	3.3V core power
VDD	5	8	8	-	5V or 3.3V Positive Power Supply
VSS	6	9	10	-	Ground
X2	7	10	11	O	Oscillator output
X1	8	11	12	I	Oscillator input
RST	29	7	7	I	Active high reset
DA0/P5.0	3	3	3	I/O	PWM DAC output / General purpose I/O (CMOS)
DA1/P5.1	2	2	2	I/O	PWM DAC output / General purpose I/O (CMOS)
DA2/P5.2	1	1	1	I/O	PWM DAC output / General purpose I/O (CMOS)
DA3/P5.3	38	40	42	I/O	PWM DAC output / General purpose I/O (CMOS)
DA4/P5.4	37	39	41	I/O	PWM DAC output / General purpose I/O (CMOS)
DA5/P5.5	36	38	40	I/O	PWM DAC output / General purpose I/O (CMOS)
DA6/P5.6	30	32	34	I/O	PWM DAC output / General purpose I/O (CMOS)
DA7/HCLAMP	31	33	35	O	PWM DAC output / Hsync clamp pulse output (CMOS)
DA8/HLFHO	35	37	39	O	PWM DAC output / Hsync half freq. Output (open drain)
DA9/HALFV	34	36	38	O	PWM DAC output / Vsync half freq. Output (open drain)
HSCL/P3.0/Rxd	25	28	29	I/O	Slave IIC clock / General purpose I/O / Rxd (open drain)
HSDA/P3.1/Txd	24	27	28	I/O	Slave IIC data / General purpose I/O / Txd (open drain)
P3.2/INT0	15	18	19	I/O	General purpose I/O / INT0 (8051 standard)
ISDA/P3.4/T0	9	12	13	I/O	Master IIC data / General purpose I/O / T0 (open drain)
ISCL/P3.5/T1	10	13	14	I/O	Master IIC clock / General purpose I/O / T1 (open drain)
P1.0	13	16	17	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.1	14	17	18	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.2	16	19	20	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.3	17	20	21	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.4	18	21	22	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.5	19	22	23	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.6	20	23	24	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.7	21	24	25	I/O	General purpose I/O (CMOS output or 8051 standard)
P6.0/AD0	23	26	27	I/O	General purpose I/O / ADC Input (CMOS)
P6.1/AD1	22	25	26	I/O	General purpose I/O / ADC Input (CMOS)
P6.2/AD2/HLFHI	12	15	16	I/O	General purpose I/O / ADC Input / Half Hsync input (CMOS)
P6.3/AD3	-	-	9	I/O	General purpose I/O / ADC Input (CMOS)
P6.4/DA10	26	29	30	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.5/DA11	27	30	31	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.6/DA12	28	31	32	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.7/DA13	-	-	33	I/O	General purpose I/O / PWM DAC output (CMOS)
VBLANK/P4.0	32	34	36	O	Vertical blank (CMOS) / General purpose Output (CMOS)
HBLANK/P4.1	33	35	37	O	Horizontal blank (CMOS) / General purpose Output (CMOS)
STOUT/P4.2	11	14	15	O	Self-test video output (CMOS) / General purpose Output (CMOS)
HSYNC	39	41	43	I	Horizontal SYNC or Composite SYNC Input
VSYNC	40	42	44	I	Vertical SYNC input

FUNCTIONAL DESCRIPTIONS

1. 8051 CPU Core

The CPU core of MTV312M is compatible with the industry standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers, five interrupt sources and serial interface. The CPU core fetches its program code from the 64K bytes Flash in MTV312M. It uses Port0 and Port2 to access the “external special function register” (XFR) and external auxiliary RAM (AUXRAM).
The CPU core can run at double rate when FclkE is set. Once the bit is set, the CPU runs as if a 24MHz X’tal is applied on MTV312M, but the peripherals (IIC, DDC, H/V processor) still run at the original frequency.

Note: All registers listed in this document reside in 8051’s external RAM area (XFR). For internal RAM memory map please refer to 8051 spec.

2. Memory Allocation

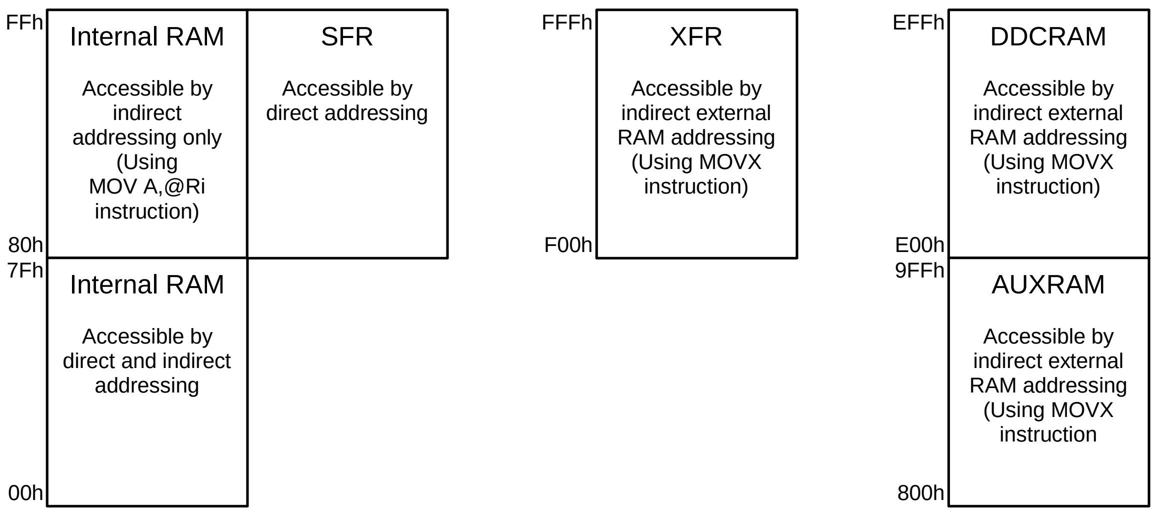
2.1 Internal Special Function Registers (SFR)
The SFR is a group of registers that are the same as standard 8051.

2.2 Internal RAM
There is a total of 256 bytes internal RAM in MTV312M, the same as standard 8052.

2.3 External Special Function Registers (XFR)
The XFR is a group of registers allocated in the 8051 external RAM area F00h - FFFh. These registers are used for special functions. Programs can use "MOVX" instruction to access these registers.

2.4 Auxiliary RAM (AUXRAM)
There is a total of 512 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - 9FFh. Programs can use "MOVX" instruction to access the AUXRAM.

2.5 Dual Port RAM (DDCRAM)
There are 256 bytes Dual Port RAM allocated in the 8051 external RAM area E00h - EFFh. Program can use "MOVX" instruction to access the RAM. The external DDC1/2 Host can access the RAM as if a 24LC02 EEPROM is connected on the interface.



3. Chip Configuration

The Chip Configuration registers define configuration of the chip and function of the pins.

Reg name	addr	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0
PADMOD	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	F51h(w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	HIICE	IIICE	HLFVE	HLFHE	HCLPE	P42E	P41E	P40E
PADMOD	F53h(w)		P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w)	PWMF	DIV253	FclkE		ENSCL	Msel	MIICF1	MIICF0

PADMOD (w) : Pad mode control registers. (All are "0" in Chip Reset)

DA13E = 1 → Pin "P6.7/DA13" is DA13.
= 0 → Pin "P6.7/DA13" is P6.7.
DA12E = 1 → Pin "P6.6/DA12" is DA12.
= 0 → Pin "P6.6/DA12" is P6.6.
DA11E = 1 → Pin "P6.5/DA11" is DA11.
= 0 → Pin "P6.5/DA11" is P6.5.
DA10E = 1 → Pin "P6.4/DA10" is DA10.
= 0 → Pin "P6.4/DA10" is P6.4.
AD3E = 1 → Pin "P6.3/AD3" is AD3.
= 0 → Pin "P6.3/AD3" is P6.3.
AD2E = 1 → Pin "P6.2/AD2" is AD2.
= 0 → Pin "P6.2/AD2" is P6.2.
AD1E = 1 → Pin "P6.1/AD1" is AD1.
= 0 → Pin "P6.1/AD1" is P6.1.
AD0E = 1 → Pin "P6.0/AD0" is AD0.
= 0 → Pin "P6.0/AD0" is P6.0.
P56E = 1 → Pin "DA6/P5.6" is P5.6.
= 0 → Pin "DA6/P5.6" is DA6.
P55E = 1 → Pin "DA5/P5.5" is P5.5.
= 0 → Pin "DA5/P5.5" is DA5.
P54E = 1 → Pin "DA4/P5.4" is P5.4.
= 0 → Pin "DA4/P5.4" is DA4.
P53E = 1 → Pin "DA3/P5.3" is P5.3.
= 0 → Pin "DA3/P5.3" is DA3.
P52E = 1 → Pin "DA2/P5.2" is P5.2.
= 0 → Pin "DA2/P5.2" is DA2.
P51E = 1 → Pin "DA1/P5.1" is P5.1.
= 0 → Pin "DA1/P5.1" is DA1.
P50E = 1 → Pin "DA0/P5.0" is P5.0.
= 0 → Pin "DA0/P5.0" is DA0.
HIICE = 1 → Pin "HSCL/P3.0/Rxd" is HSCL; pin "HSDA/P3.1/Txd" is HSDA.
= 0 → Pin "HSCL/P3.0/Rxd" is P3.0/Rxd; pin "HSDA/P3.1/Txd" is P3.1/Txd.
IIICE = 1 → Pin "ISDA/P3.4/T0" is ISDA; pin "ISCL/P3.5/T1" is ISCL.
= 0 → Pin "ISDA/P3.4/T0" is P3.4/T0; pin "ISCL/P3.5/T1" is P3.5/T1.
HLFVE = 1 → Pin "DA9/HALFV" is VSYNC half frequency output.
= 0 → Pin "DA9/HALFV" is DA9.
HLFHE = 1 → Pin "DA8/HALFH" is HSYNC half frequency output.
= 0 → Pin "DA8/HALFH" is DA8.

HCLPE	= 1	→ Pin “DA7/HCLAMP” is HSYNC clamp pulse output.
	= 0	→ Pin “DA7/HCLAMP” is DA7.
P42E	= 1	→ Pin “STOUT/P4.2” is P4.2.
	= 0	→ Pin “STOUT/P4.2” is STOUT.
P41E	= 1	→ Pin “HBLANK/P4.1” is P4.1.
	= 0	→ Pin “HBLANK/P4.1” is HBLANK.
P40E	= 1	→ Pin “VBLANK/P4.0” is P4.0.
	= 0	→ Pin “VBLANK/P4.0” is VBLANK.
P56oe	= 1	→ P5.6 is output pin.
	= 0	→ P5.6 is input pin.
P55oe	= 1	→ P5.5 is output pin.
	= 0	→ P5.5 is input pin.
P54oe	= 1	→ P5.4 is output pin.
	= 0	→ P5.4 is input pin.
P53oe	= 1	→ P5.3 is output pin.
	= 0	→ P5.3 is input pin.
P52oe	= 1	→ P5.2 is output pin.
	= 0	→ P5.2 is input pin.
P51oe	= 1	→ P5.1 is output pin.
	= 0	→ P5.1 is input pin.
P50oe	= 1	→ P5.0 is output pin.
	= 0	→ P5.0 is input pin.
P67oe	= 1	→ P6.7 is output pin.
	= 0	→ P6.7 is input pin.
P66oe	= 1	→ P6.6 is output pin.
	= 0	→ P6.6 is input pin.
P65oe	= 1	→ P6.5 is output pin.
	= 0	→ P6.5 is input pin.
P64oe	= 1	→ P6.4 is output pin.
	= 0	→ P6.4 is input pin.
P63oe	= 1	→ P6.3 is output pin.
	= 0	→ P6.3 is input pin.
P62oe	= 1	→ P6.2 is output pin.
	= 0	→ P6.2 is input pin.
P61oe	= 1	→ P6.1 is output pin.
	= 0	→ P6.1 is input pin.
P60oe	= 1	→ P6.0 is output pin.
	= 0	→ P6.0 is input pin.
COP17	= 1	→ Pin “P1.7” is CMOS Output.
	= 0	→ Pin “P1.7” is 8051 standard I/O.
COP16	= 1	→ Pin “P1.6” is CMOS Output.
	= 0	→ Pin “P1.6” is 8051 standard I/O.
COP15	= 1	→ Pin “P1.5” is CMOS Output.
	= 0	→ Pin “P1.5” is 8051 standard I/O.
COP14	= 1	→ Pin “P1.4” is CMOS Output.
	= 0	→ Pin “P1.4” is 8051 standard I/O.
COP13	= 1	→ Pin “P1.3” is CMOS Output.
	= 0	→ Pin “P1.3” is 8051 standard I/O.
COP12	= 1	→ Pin “P1.2” is CMOS Output.
	= 0	→ Pin “P1.2” is 8051 standard I/O.
COP11	= 1	→ Pin “P1.1” is CMOS Output.
	= 0	→ Pin “P1.1” is 8051 standard I/O.

COP10 = 1 → Pin “P1.0” is CMOS Output.
= 0 → Pin “P1.0” is 8051 standard I/O.

OPTION (w): Chip option configuration (All are "0" in Chip Reset).
PWMF = 1 → Selects 94KHz PWM frequency.
= 0 → Selects 47KHz PWM frequency.
DIV253 = 1 → PWM pulse width is 253 step resolution.
= 0 → PWM pulse width is 256 step resolution.
FclkE = 1 → CPU is running at double rate
= 0 → CPU is running at normal rate
ENSCL = 1 → Enables slave IIC block to hold HSCL pin low while MTV212M64i is unable to Catch-up the external master's speed.
Msel = 1 → Master IIC block connected to HSCL/HSDA pins.
= 0 → Master IIC block connected to ISCL/ISDA pins.
MIICF1,MIICF0 = 1,1 → Selects 400KHz Master IIC frequency.
= 1,0 → Selects 200KHz Master IIC frequency.
= 0,1 → Selects 50KHz Master IIC frequency.
= 0,0 → Selects 100KHz Master IIC frequency.

4. I/O Ports

4.1 Port1
Port1 is a group of pseudo open drain pins or CMOS output pins. It can be used as general purpose I/O. Behavior of Port1 is the same as standard 8051.

4.2 P3.0-2, P3.4-5
If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Behavior of Port3 is the same as standard 8051.

4.3 Port4, Port5 and Port6
Port5 and Port6 are used as general purpose I/O. S/W needs to set the corresponding P5(n)oe and P6(n)oe to define whether these pins are input or output. Port4 is pure output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42

PORT5 (r/w) : Port 4 data input/output value.

PORT6 (r/w) : Port 5 data input/output value.
PORT4 (w) : Port 6 data output value.

5. PWM DAC

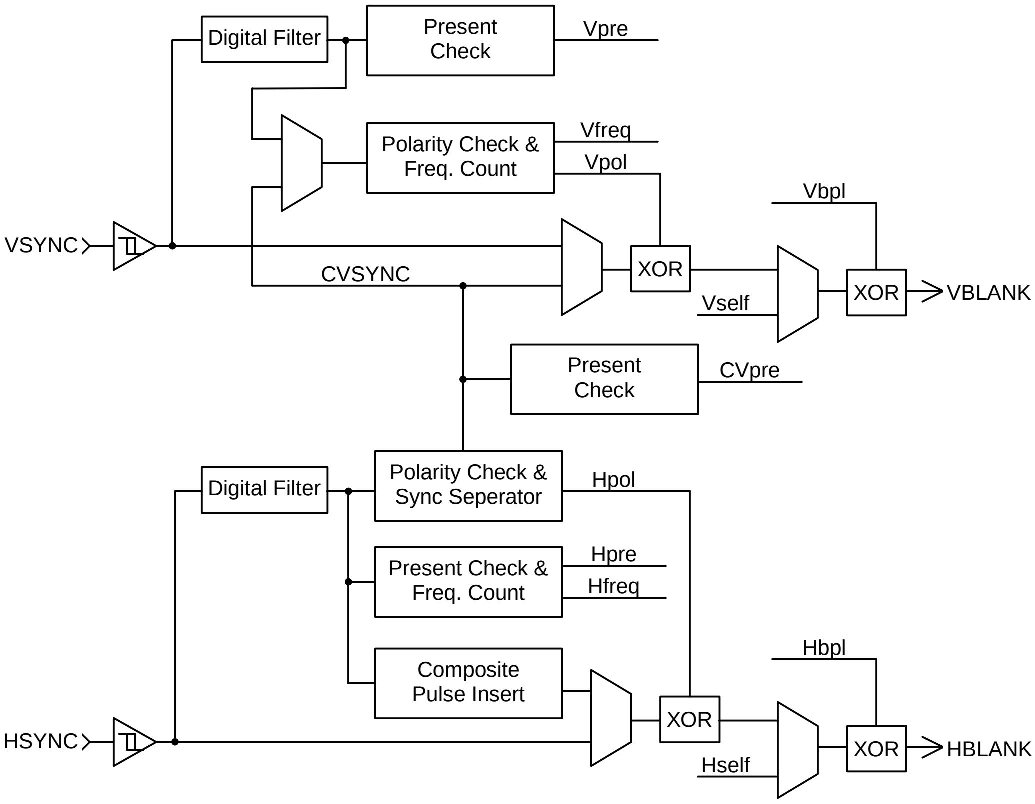
Each output pulse width of PWM DAC converter is controlled by an 8-bit register in XFR. The frequency of PWM clock is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							
DA6	F26h(r/w)	Pulse width of PWM DAC 6							
DA7	F27h(r/w)	Pulse width of PWM DAC 7							
DA8	F28h(r/w)	Pulse width of PWM DAC 8							
DA9	F29h(r/w)	Pulse width of PWM DAC 9							
DA10	F2Ah(r/w)	Pulse width of PWM DAC 10							
DA11	F2Bh(r/w)	Pulse width of PWM DAC 11							
DA12	F2Ch(r/w)	Pulse width of PWM DAC 12							
DA13	F2Dh(r/w)	Pulse width of PWM DAC 13							

DA0-13 (r/w) : The output pulse width control for DA0-13.
* All of PWM DAC converters are centered with value 80h after power on.

6. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation/insertion. SYNC inputs presence check, frequency counting, polarity detection and control, as well as the protection of VBLANK output while VSYNC speeds up in high DDC communication clock rate.
Based on the digital filter, the present and frequency function block treat any pulse shorter than one OSC period (83.33ns) as noise, between one and two OSC period (83.33ns to 166.67ns) as unknown region, and longer than two OSC period (166.67ns) as pulse.



H/V SYNC Processor Block Diagram

6.1 Composite SYNC separation/insertion

The MTV312M continuously monitors the input HSYNC, if the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and users can select the extracted "CVSYNC" for the source of polarity check, frequency count, and VBLANK output. The CVSYNC will have 8us delay compared to the original signal. The MTV312M can also insert pulse to HBLANK output during composite VSYNC's active time. The width of insert pulse is 1/8 HSYNC period and the insertion frequency can adapt to original HSYNC. The insert pulse of HBLANK can be disabled or enabled by setting "NoHins" control bit.

6.2 H/V Frequency Counter

MTV312M can discriminate HSYNC/VSYNC frequency and save the information in XFRs. The 14 bits Hcounter counts the time of 64xHSYNC period, then loads the result into the HCNTH/HCNTL latch. The output value will be [(128000000/H-Freq) - 1], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present. The 12 bits Vcounter counts the time between two VSYNC pulses, then loads the result into the VCNTH/VCNTL latch. The output value will be (62500/V-Freq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is set when VCNT/HCNT value changes or overflows. Table 6.2.1 and Table 6.2.2 show the HCNT/VCNT value under the operations of 12MHz.

6.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (14 bits)
		12MHz OSC (hex / dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

6.2.2 V-Freq Table

V-Freq(Hz)		Output value (12bits)
		12MHz OSC (hex / dec)
1	56	45Ch / 1116
2	60	411h / 1041
3	70	37Ch / 892
4	72	364h / 868
5	75	341h / 833
6	85	2DFh / 735

6.3 H/V Present Check

The Hpresent function checks the input HSYNC pulse, Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse, the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value change.

6.4 H/V Polarity Detect

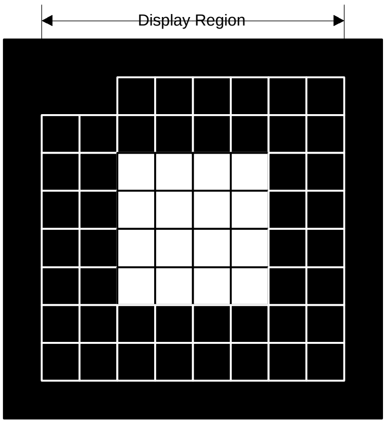
The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

6.5 Output HBLANK/VBLANK Control and Polarity Adjust

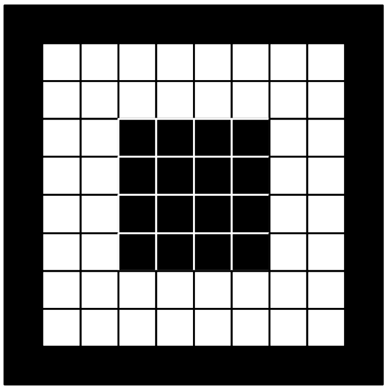
The HBLANK is the mux output of HSYNC, composite Hpulse and self-test horizontal pattern. The VBLANK is the mux output of VSYNC, CVSYNC and self-test vertical pattern. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 250Hz. The HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

6.6 Self Test Pattern Generator

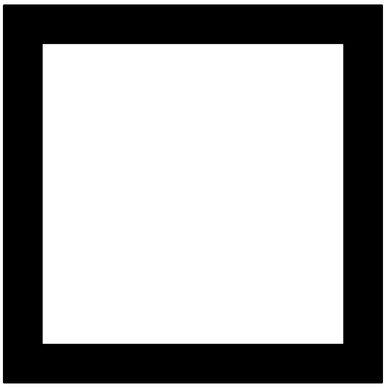
For testing purposes, this generator can generate 4 display patterns, which are positive cross-hatch, negative cross-hatch, full white, and full black (shown as figures below). The HBLANK output frequency of the pattern can be chosen to 95.2KHz, 63.5KHz, 47.6KHz and 31.75KHz. The VBLANK output frequency of the pattern is 72Hz or 60Hz. It is originally designed to support monitor manufacturer to do burn-in test, or offer end-user a reference to check the monitor. The output STOUT of the generator shares the output pin with P4.2.



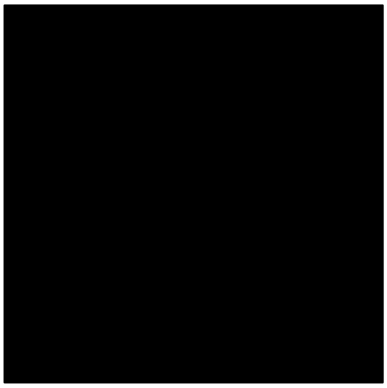
Positive cross-hatch



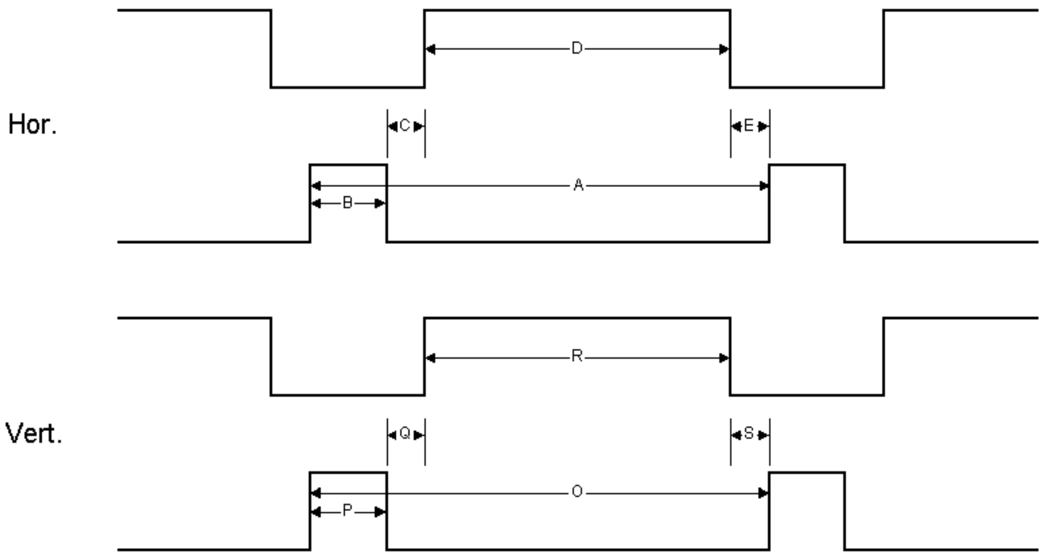
Negative cross-hatch



Full white



Full black



MTV312M Self-Test Pattern Timing

	63.5KHz, 60Hz		47.6KHz, 60Hz		31.7KHz, 60Hz		95.2KHz, 72Hz	
	Time	**H dots**	**Time**	**H dots**	**Time**	**H dots**	**Time**	**H dots**
Hor. Total time (A)	15.75us	1280	21.0us	1024	31.5us	640	10.5us	1600
Hor. Active time (D)	12.05us	979.3	16.07us	783.2	24.05us	488.6	8.03us	1224
Hor. F. P. (E)	0.2us	16.25	0.28us	12	0.45us	9	0.14us	21
SYNC pulse width (B)	1.5us	122	2us	90	3us	61	1.0us	152
Hor. B. P. (C)	2us	162.54	2.67us	110	4us	81.27	1.33us	203

	Time	**V lines**	**Time**	**V lines**	**Time**	**V lines**	**Time**	**V lines**
Vert. Total time (O)	16.66ms	1024	16.66ms	768	16.66ms	480	13.89ms	1200
Vert. Active time (R)	15.65ms	962	15.65ms	721.5	15.65ms	451	13.03ms	1126
Vert. F. P. (S)	0.063ms	3.87	0.063ms	2.9	0.063ms	1.82	0.052ms	4.5
SYNC pulse width (P)	0.063ms	3.87	0.063ms	2.9	0.063ms	1.82	0.052ms	4.5
Vert. B. P. (Q)	0.882ms	54.2	0.882ms	40.5	0.882ms	25.4	0.756ms	65

* 8 x 8 blocks of cross hatch pattern in display region.

6.7 HSYNC Clamp Pulse Output

The HCLAMP output is active by setting “HCLPE” control bit. The leading edge position, pulse width and polarity of HCLAMP are S/W controllable.

6.8 VSYNC Interrupt

The MTV312M checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC flag is set each time when MTV312M detects a VSYNC pulse. The flag is cleared by S/W writing a "0".

6.9 H/V SYNC Processor Register

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	F43h(r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h(w)	C1	C0	NoHins	SelExH	IVHlfH	HlfHE	HBpl	VBpl
HVCTR2	F42h(w)			Selft	STF1	STF0	Rt1	Rt0	
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
INTFLG	F48h(r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h(w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync

HVSTUS (r) : The status of polarity, present and static level for HSYNC and VSYNC.

CVpre = 1 → The extracted CVSYNC is present.
= 0 → The extracted CVSYNC is not present.

Hpol = 1 → HSYNC input is positive polarity.
= 0 → HSYNC input is negative polarity.

Vpol = 1 → VSYNC (CVSYNC) is positive polarity.
= 0 → VSYNC (CVSYNC) is negative polarity.

Hpre = 1 → HSYNC input is present.
= 0 → HSYNC input is not present.

Vpre = 1 → VSYNC input is present.
= 0 → VSYNC input is not present.

Hoff* = 1 → Off level of HSYNC input is high.

= 0 → Off level of HSYNC input is low.
V_{off}* = 1 → Off level of VSYNC input is high.
= 0 → Off level of VSYNC input is low.
*H_{off} and V_{off} are valid when H_{pre}=0 or V_{pre}=0.

HCNTH (r) : H-Freq counter's high bits.
Hovf = 1 → H-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
HF13 - HF8 : 6 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low byte.

VCNTH (r) : V-Freq counter's high bits.
Vovf = 1 → V-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
VF11 - 8 : 4 high bits of V-Freq counter.

VCNTL (r) : V-Freq counter's low byte.

HVCTR0 (w) : H/V SYNC processor control register 0.
C1, C0 = 1,1 → Selects CVSYNC as the polarity, freq and VBLANK source.
= 1,0 → Selects VSYNC as the polarity, freq and VBLANK source.
= 0,0 → Disables composite function.
= 0,1 → H/W automatically switches to CVSYNC when CVpre=1 and VSpre=0.
NoHins = 1 → HBLANK has no insert pulse in composite mode.
= 0 → HBLANK has insert pulse in composite mode.
SelExH = 1 → Input source of HLFHO is HLFHI.
= 0 → Input source of HLFHO is HSYNC.
IVHlfH = 1 → HLFHO is inverted.
= 0 → HLFHO is not inverted.
HlfHE = 1 → HLFHO is half freq. of HSYNC/HLFHI.
= 0 → HLFHO is same freq. of HSYNC/HLFHI.
HB_{pl} = 1 → Negative polarity HBLANK output.
= 0 → Positive polarity HBLANK output.
VB_{pl} = 1 → Negative polarity VBLANK output.
= 0 → Positive polarity VBLANK output.

HVCTR2 (w) : Self-test pattern generator control.
Selft = 1 → Enables generator.
= 0 → Disables generator.
STF1,STF0 = 1,1 → 95.2KHz(horizontal)/72Hz(vertical) output selected.
= 1,0 → 63.5KHz(horizontal)/60Hz(vertical) output selected.
= 0,1 → 47.6KHz(horizontal) /60Hz(vertical) output selected.
= 0,0 → 31.75KHz(horizontal) /60Hz(vertical) output selected.
Rt1,Rt0 = 0,0 → Positive cross-hatch pattern output.
= 0,1 → Negative cross-hatch pattern output.
= 1,0 → Full white pattern output.
= 1,1 → Full black pattern output.

HVCTR3 (w) : HSYNC clamp pulse control register.
CLPEG = 1 → Clamp pulse follows HSYNC leading edge.
= 0 → Clamp pulse follows HSYNC trailing edge.
CLPPO = 1 → Positive polarity clamp pulse output.
= 0 → Negative polarity clamp pulse output.
CLPW2 : CLPW0 : Pulse width of clamp pulse is

[(CLPW2:CLPW0) + 1] x 0.167 µs for 12MHz X'tal selection.

INTFLG (w) : Interrupt flag. An interrupt event sets its individual flag, and, if the corresponding interrupt enable bit is set, the INT1 source of 8051 core will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

HPRchg= 1 → No action.
= 0 → Clears HSYNC presence change flag.
VPRchg= 1 → No action.
= 0 → Clears VSYNC presence change flag.
HPLchg= 1 → No action.
= 0 → Clears HSYNC polarity change flag.
VPLchg= 1 → No action.
= 0 → Clears VSYNC polarity change flag.
HFchg = 1 → No action.
= 0 → Clears HSYNC frequency change flag.
VFchg = 1 → No action.
= 0 → Clears VSYNC frequency change flag.
Vsync = 1 → No action.
= 0 → Clears VSYNC interrupt flag.

INTFLG (r) : Interrupt flag.

HPRchg= 1 → Indicates a HSYNC presence change.
VPRchg= 1 → Indicates a VSYNC presence change.
HPLchg= 1 → Indicates a HSYNC polarity change.
VPLchg= 1 → Indicates a VSYNC polarity change.
HFchg = 1 → Indicates a HSYNC frequency change or counter overflow.
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow.
Vsync = 1 → Indicates a VSYNC interrupt.

INTEN (w) : Interrupt enable.

EHPR = 1 → Enables HSYNC presence change interrupt.
EVPR = 1 → Enables VSYNC presence change interrupt.
EHPL = 1 → Enables HSYNC polarity change interrupt.
EVPL = 1 → Enables VSYNC polarity change interrupt.
EHF = 1 → Enables HSYNC frequency change / counter overflow interrupt.
EVF = 1 → Enables VSYNC frequency change / counter overflow interrupt.
EVsync = 1 → Enables VSYNC interrupt.

7. DDC & IIC Interface

7.1 DDC1/DDC2x Mode, DDCRAM and SlaveA block

The MTV312M enters DDC1 mode after Reset. In this mode, VSYNC is used as data clock. The HSCL pin should remain at high. The data output to the HSDA pin is taken from a shift register in MTV312M. The shift register automatically fetches EDID data from the lower 128 bytes of the Dual Port RAM (DDCRAM), then sends it in 9 bits packet formats which includes a null bit (=1) as packet separator. S/W may enable/disable the DDC1 function by setting/clearing the DDC1en control bit.
The MTV312M switches to DDC2x mode when it detects a high to low transition on the HSCL pin. In this mode, the SlaveA IIC block automatically transmits/receives data to/from the IIC Master. The transmitted/received data is taken-from/saved-to the DDCRAM. In simple words, MTV312M can act as 24LC02 EEPROM behavior. The only thing S/W needs to do is to write the EDID data to DDCRAM. The slave address of SlaveA block can be chosen by S/W as 5-bits, 6-bits or 7-bits. For example, if S/W chooses 5-bits slave address as 10100b, the slave IIC block A responds to slave address 10100xxb. The SlaveA can be enabled/disabled by setting/clearing the EnslvA bit. The lower/upper DDCRAM can/cannot

be written by the IIC Master by setting/clearing the EN128w/En256w bit. Besides, if the Only128 control bit is set, the SlaveA will only access the lower 128 bytes of the DDCRAM.
The MTV312M returns to DDC1 mode if HSCL is kept high for 128 VSYNC clock period. However, it locks in DDC2B mode if a valid IIC address (1010xxxb) is detected on HSCL/HSDA bus. The DDC2 flag reflects the current DDC status, S/W may clear it by writing a "0" to it.

7.2 SlaveB Block

The SlaveB IIC block is connected to HSDA and HSCL pins. The block can receive/transmit data using IIC protocols. S/W may write the SLVBADR register to determine the slave addresses.
In receive mode, the block first detects IIC slave address matching the condition then issues a SlvBMI interrupt. The data from HSDA is shifted into shift register then written to RCBBUF register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCBI (receives buffer full interrupt) every time when the RCBBUF is loaded. If S/W is not able to read out the RCBBUF in time, the next byte in shift register will not be written to RCBBUF and the slave block will return NACK to the master. This feature guarantees the data integrity of communication. The WadrB flag can tell S/W whether the data in RCBBUF is a word address.
In transmit mode, the block first detects IIC slave address matching the condition, then issues a SlvBMI interrupt. In the meantime, the data pre-stored in the TXBBUF is loaded into shift register, resulting in TXBBUF emptying and generates a TXBI (transmit buffer empty interrupt). S/W should write the TXBBUF a new byte for the next transfer before shift register empties. A failure of this process causes data corrupt. The TXBI occurs every time when shift register reads out the data from TXBBUF.
The SlvBMI is cleared by writing "0" to corresponding bit in INTFLG register. The RCBI is cleared by reading out RCBBUF. The TXBI is cleared by writing TXBBUF.

*Please see the attachments about "Slave IIC Block Timing".

7.3 Master Mode IIC Function Block

The master mode IIC block can be connected to the ISDA /ISCL pins or the HSDA/HSCL pins, select by Msel control bit. Its speed can be selected to 50KHz-400KHz by S/W setting the MIICF1/MIICF0 control bit. The software program can access the external IIC device through this interface. A summary of master IIC access is described as follows.

7.3.1. To write IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV312M transmit this byte, a MbufI interrupt will be triggered.
4. Program can write MBUF to transfer next byte or set P bit to stop.
* Please see the attachments about "Master IIC Transmit Timing".

7.3.2. To read IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV312M transmit this byte, a MbufI interrupt will be triggered.
4. Set or reset the MAckO flag according to the IIC protocol.
5. Read out MBUF the useless byte to continue the data transfer.
6. After the MTV312M receives a new byte, the MbufI interrupt is triggered again.
7. Read MBUF also trigger the next receive operation, but set P bit before read can terminate the operation.

* Please see the attachments about "Master IIC Receive Timing".

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)	DDC2					MAckO	P	S
IICSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MAckIn
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	STOPI	ReStaI	WSlvAI		MbufI
INTFLG	F03h (w)			SlvBMI	STOPI	ReStaI	WSlvAI		MbufI

INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ESTOPI	EReStaI	EWSlvAI		EMbufI
MBUF	F05h (r/w)	Master IIC receive/transmit data buffer							
DDCCTR	F06h (w)	DDC1en	En128W	En256W	Only128			SlvAbs1	SlvAbs0
SLVAADR	F07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	F08h (r)	Slave B IIC receive buffer							
TXBBUF	F08h (w)	Slave B IIC transmit buffer							
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address						

IICCTR (r/w) : IIC interface control register.

MAckO = 1 → In master receive mode, NACK is returned by MTV312M.
= 0 → In master receive mode, ACK is returned by MTV312M.
S, P = ↑, 0 → Start condition when Master IIC is not during transfer.
= X, ↑ → Stop condition when Master IIC is not during transfer.
= 1, X → Resume transfer after a read/write MBUF operation.

IICSTUS (r) : IIC interface status register.

WadrB = 1 → The data in RCBBUF is word address.
SlvRWB = 1 → Current transfer is slave transmit
= 0 → Current transfer is slave receive
SAckIn = 1 → The external IIC host respond NACK.
SLVS = 1 → The slave block has detected a START, cleared when STOP detected.
MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.
= 0 → ACK received from the slave IIC device.

INTFLG (w) : Interrupt flag. A interrupt event sets its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source is then driven by a zero level. Software MUST clear this register while serving the interrupt routine.

SlvBMI = 1 → No action.
= 0 → Clears SlvBMI flag.
STOPI = 1 → No action.
= 0 → Clears STOPI flag.
ReStaI = 1 → No action.
= 0 → Clears ReStaI flag.
WSlvAI = 1 → No action.
= 0 → Clears WSlvAI flag.
MbufI = 1 → No action.
= 0 → Clears Master IIC bus interrupt flag (MbufI).

INTFLG (r) : Interrupt flag.

TXBI = 1 → Indicates the TXBBUF need a new data byte, cleared by writing TXBBUF.
RCBI = 1 → Indicates the RCBBUF has received a new data byte, cleared by reading RCBBUF.
SlvBMI = 1 → Indicates the slave IIC address B match condition.
STOPI = 1 → Indicates the slave IIC has detected a STOP condition.
ReStaI = 1 → Indicates the slave IIC has detected a repeat START condition.
WSlvAI = 1 → Indicates the slave A IIC has detected a STOP condition of write mode.
MbufI = 1 → Indicates a byte is sent/received to/from the master IIC bus.

INTEN (w) : Interrupt enable.

ETXBI = 1 → Enables TXBBUF interrupt.
ERCBI = 1 → Enables RCBBUF interrupt.
ESlvBMI = 1 → Enables slave address B match interrupt.
ESTOPI = 1 → Enables IIC bus STOP interrupt.

EReStaI = 1 → Enables IIC bus repeat START interrupt.
EWSlvAI = 1 → Enables slave A IIC bus STOP of write mode interrupt.
EMbufI = 1 → Enables Master IIC bus interrupt.

Mbuf (w) : Master IIC data shift register, after START and before STOP condition, write this register resumes MTV312M's transmission to the IIC bus.

Mbuf (r) : Master IIC data shift register, after START and before STOP condition, read this register resumes MTV312M's receiving from the IIC bus.

DDCCTR (w) : DDC interface control register.
DDC1en = 1 → Enables DDC1 data transfer in DDC1 mode.
= 0 → Disables DDC1 data transfer in DDC1 mode.
En128W = 1 → The lower 128 bytes (00-7F) of DDCRAM can be written by IIC master.
= 0 → The lower 128 bytes (00-7F) of DDCRAM cannot be written by IIC master.
En256W = 1 → The higher 128 bytes (80-FF) of DDCRAM can be written by IIC master.
= 0 → The higher 128 bytes (80-FF) of DDCRAM cannot be written by IIC master.
Only128 = 1 → The SlaveA always accesses EDID data from the lower 128 bytes of DDCRAM.
= 0 → The SlaveA accesses EDID data from the whole 256 bytes DDCRAM.
SlvAbs1,SlvAbs0 : Slave IIC block A's slave address length.
= 1,0 → 5-bits slave address.
= 0,1 → 6-bits slave address.
= 0,0 → 7-bits slave address.

SLVAADR (w) : Slave IIC block A's enable and address.
ENslvA = 1 → Enables slave IIC block A.
= 0 → Disables slave IIC block A.
bit6-0 : Slave IIC address A to which the slave block should respond.

RCBBUF (r) : Slave IIC block B receives data buffer.

TXBBUF (w) : Slave IIC block B transmits data buffer.

SLVBADR (w) : Slave IIC block B's enable and address.
ENslvB = 1 → Enables slave IIC block B.
= 0 → Disables slave IIC block B.
bit6-0 : Slave IIC address B to which the slave block should respond.

8. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of power supply is below 3.8V (+/-0.2V) for a specific period of time, the LVR generates a chip reset signal. After the power supply is above 3.8V (+/-0.2V), LVR stays in reset state for 144 Xtal cycle to guarantee the chip exit reset condition with a stable X'tal oscillation.
The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is 0.25 sec x N, where N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power on reset, users can activate this function by setting WEN, and clear the timer by setting WCLR.

9. A/D converter

The MTV312M is equipped with four VDD range 6-bit A/D converters. S/W can select the current convert channel by setting the SADC1/SADC0 bit. The refresh rate for the ADC is OSC freq./1536.

The ADC compares the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 63). The ADC output value is N when pin voltage is greater than VDD*N/64 and smaller than VDD*(N+1)/64.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)			ADC convert result					
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

WDT (w) : Watchdog Timer control register.

WEN = 1 → Enables Watchdog Timer.
WCLR = 1 → Clears Watchdog Timer.
WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.
= 1 → Overflow interval = 1 x 0.25 sec.
= 2 → Overflow interval = 2 x 0.25 sec.
= 3 → Overflow interval = 3 x 0.25 sec.
= 4 → Overflow interval = 4 x 0.25 sec.
= 5 → Overflow interval = 5 x 0.25 sec.
= 6 → Overflow interval = 6 x 0.25 sec.
= 7 → Overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.

ENADC = 1 → Enables ADC.
SADC0 = 1 → Selects ADC0 pin input.
SADC1 = 1 → Selects ADC1 pin input.
SADC2 = 1 → Selects ADC2 pin input.
SADC3 = 1 → Selects ADC3 pin input.

ADC (r) : ADC convert result.

10. In System Programming function (ISP)

The Flash memory can be programmed by a specific WRITER in parallel mode, or by IIC Host in serial mode while the system is working. The features of ISP are outlined as below:

1. Single 3.3V power supply for Program/Erase/Verify.
2. Block Erase: 512 Byte, 10mS time
3. Whole Flash erase (Blank): 10mS
4. Byte/Word programming Cycle time: 60uS per byte
5. Read access time: 40ns
6. Only one two-pin IIC bus (shared with DDC2) is needed for ISP in user/factory mode.
7. IIC Bus clock rates up to 140KHz.
8. Whole 64K-byte Flash programming within 6 Sec.
9. CRC check provides 100% coverage for all single/double bit errors.

After Power On/Reset, The MTV312M runs the original Program Code. Once the S/W detects an ISP request (by key or IIC), S/W accepts the request following the steps below:

1. Clear watchdog to prevent reset during ISP period.
2. Disable all interrupt to prevent CPU wake-up.
3. Write IIC address of ISP slave to ISPSLV for communication.
4. Write 93h to ISP enable register (ISPEN) to enable ISP.
5. Enter 8051 idle mode.

When ISP is enabled, the MTV312M disables Watchdog reset and switches the Flash interface to ISP host in 15-22.5uS. So S/W MUST enter idle mode immediately after enabling ISP. In the 8051 idle mode, PWM DACs and I/O pins keep running at their former status. There are 4 types of IIC bus transfer protocols in ISP mode.

```
Command Write
    S-tttttt10k-cccccxxxk-AAAAAAAAk-P
Command Read
    S-tttttt11k-cccccXXXK-AAAAAAAAK-aaaaaaaaK-RRRRRRRRK-rrrrrrrrK-P
Data Write
    S-tttttt00k-aaaaaaaak-ddddddddk-ddddddddk- ... -P
Data Read
    S-tttttt00k-aaaaaaaak-(P)-
    S-tttttt01k-ddddddddK-ddddddddK- ... -P
where
    S = start or re-start                P = stop
    K = ack by host (0 or 1)             k = ack by slave
    tttttt = ISP slave address           ccccc = command
    x = don't care                       X = not defined
    AAAAAAAA = address[15:8]             aaaaaaaa = address[7:0]
    RRRRRRRR = CRC_register[15:8]        rrrrrrrr = CRC_register[7:0]
    dddddddd = data
    ccccc = 10100 → Program
    ccccc = 00110 → Page Erase 512 bytes (Erase)
    ccccc = 01101 → Erase entire Flash (Blank)
    ccccc = 11010 → Clear CRC_register (Clr_CRC)
    ccccc = 01001 → Reset MTV312M (Reset_CPU)
```

10.1 ISP Command Write

The 2nd byte of "Command Write" can define the operating mode of MTV312M in its "Data Write" stage, clear CRC register, or reset MTV312M. The 3rd byte of Command Write defines the page address. A Command Write may consist of 1,2 or 3 bytes.

10.2 ISP Command Read

The 2nd byte echoes the current command in ISP slave. The 3rd and 4th bytes reflect the current Flash address. The 5th and 6th bytes report the CRC result. A Command Read may consist of 2,3,4,5 or 6 bytes.

10.3 ISP Data Write

The 2nd byte defines the low address of Flash. After receiving the 3rd byte, the MTV312M executes a Program/Erase/Blank command depending on the preceding "Command Write". The low address of Flash increases every time when ISP slave acknowledges the data byte. The Blank/Erase command needs one data byte (with content "don't care"). The executing time is 10mS. During the 10mS period, the ISP slave does not accept any command/data and returns non-ack to any IIC bus activity. The Program command may have 1-256 data bytes. The program cycle time is 60us. If the ISP slave is not able to complete the program cycle in time, it returns non-ack to the following data byte. In the meantime, the low address does not increase and the CRC does not count the non-acked data byte. A Data Write may consist of 1,2 or more bytes.

```
Data Write (Blank/Erase)
    S-tttttt00k-aaaaaaaak-ddddddddk-P ... S-ttttttxxk-
                                  |----Min. 10mS----|

Data Write (Program)
    S-tttttt00k-aaaaaaaak-ddddddddk-ddddddddk- ...
                                  |Min. 60uS|
```

10.4 ISP Data Read
The 1st and 2nd bytes are the same as "Data Write" to define the low address of Flash. Between 2nd and 3rd bytes, the ISP host may issue Stop-Start or only Re-Start. From the 4th byte, the ISP slave sends the data byte of Flash to ISP Host. The low address automatically increases every time when data byte transferred.

10.5 Cyclic Redundancy Check (CRC)
To shorten the verify time, the ISP slave provides a simple way to check whether data error occurs during the program data transfer. After the ISP Host sends a lot of data byte to ISP slave, Host can use Command Read to check result of CRC register instead of reading every byte in Flash. The CRC register counts every data byte which ISP slave acknowledges during "Data Write" period. However, the low address byte and the data byte of Erase/Blank are not counted. The Clear CRC command writes all "1" to the 16-bit CRC register. For CRC generation, the 16-bit CRC register is seeded with all "1" pattern (by device reset or Clear CRC command). The data byte shifted into the CRC register is Msb first. The real implementation is described as follows:

```
    CRCin = CRC[15]^DATAin;
    CRC[15:0] = {CRC[14]^CRCin, CRC[13:2], CRC[1]^CRCin, CRC[0], CRCin};
          Where ^ = XOR

 example:
    data_byte   CRC_register_remainder
                        FFFFH
       F6H              FF36H
       28H              34F2H
       C3H              7031H
```

10.6 Reset Device
After the Flash been program completed and verified OK, the ISP Host can use "Command Write" with Reset_CPU command to wake up MTV312M.

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							

Memory Map of XFR

Reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)	DDC2					MAckO	P	S
IICSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MAckIn
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	STOPI	ReStaI	WSlvAI		MbufI
INTFLG	F03h (w)			SlvBMI	STOPI	ReStaI	WSlvAI		MbufI
INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ESTOPI	EReStaI	EWSlvAI		EMbufI
MBUF	F05h (r/w)	Master IIC receives/transmits data buffer							
DDCCTR	F06h (w)	DDC1en	En128W	En256W	Only128			SlvAbs1	SlvAbs0
SLVAADR	F07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	F08h (r)	Slave B IIC receives buffer							
TXBBUF	F08h (w)	Slave B IIC transmits buffer							
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address						
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC	F10h (r)			ADC convert Result					
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							
DA6	F26h(r/w)	Pulse width of PWM DAC 6							
DA7	F27h(r/w)	Pulse width of PWM DAC 7							
DA8	F28h(r/w)	Pulse width of PWM DAC 8							
DA9	F29h(r/w)	Pulse width of PWM DAC 9							
DA10	F2Ah(r/w)	Pulse width of PWM DAC 10							
DA11	F2Bh(r/w)	Pulse width of PWM DAC 11							
DA12	F2Ch(r/w)	Pulse width of PWM DAC 12							
DA13	F2Dh(r/w)	Pulse width of PWM DAC 13							
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	F43h(r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h(w)	C1	C0	NoHins	HlfHE	IVHlfH		HBpl	VBpl
HVCTR2	F42h(w)			Selft	STF1	STF0	Rt1	Rt0	
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
INTFLG	F48h(r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h(w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF		EVsync
PADMOD	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	F51h(w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	HIICE	IIICE	HLFVE	HLFHE	HCLPE	P42E	P41E	P40E
PADMOD	F53h(w)		P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w)	PWMF	DIV253	FclkE		ENSCL	Msel	MIICF1	MIICF0
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42

ELECTRICAL PARAMETERS

1. Absolute Maximum Ratings

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +4.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	^{o}C
Maximum Storage Temperature	Tstg	-25 to +125	^{o}C

2. Allowable Operating Conditions

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	3.0	3.6	V
Input "H" Voltage	Vih1	0.7 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.25 x VDD	V
Operating Freq.	Fopg	-	15	MHz

3. DC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=5.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, open drain pin	Voh1	Ioh=0uA	4			V
Output "H" Voltage, 8051 I/O port pin	Voh2	Ioh=-50uA	4			V
Output "H" Voltage, CMOS output	Voh3	Ioh=-4mA	4			V
Output "L" Voltage	Vol	Iol=5mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	150		250	Kohm
Pin Capacitance	Cio				15	pF

4. AC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=5.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		7.5	uS
VS input pulse Width	tVIPW	fXtal=12MHz	3			uS
HSYNC to Hblank output jitter	tHHBJ				5	nS
H+V to Vblank output delay	tVVBD	fXtal=12MHz		8		uS
VS pulse width in H+V signal	tVCPW	FXtal=12MHz	20			uS

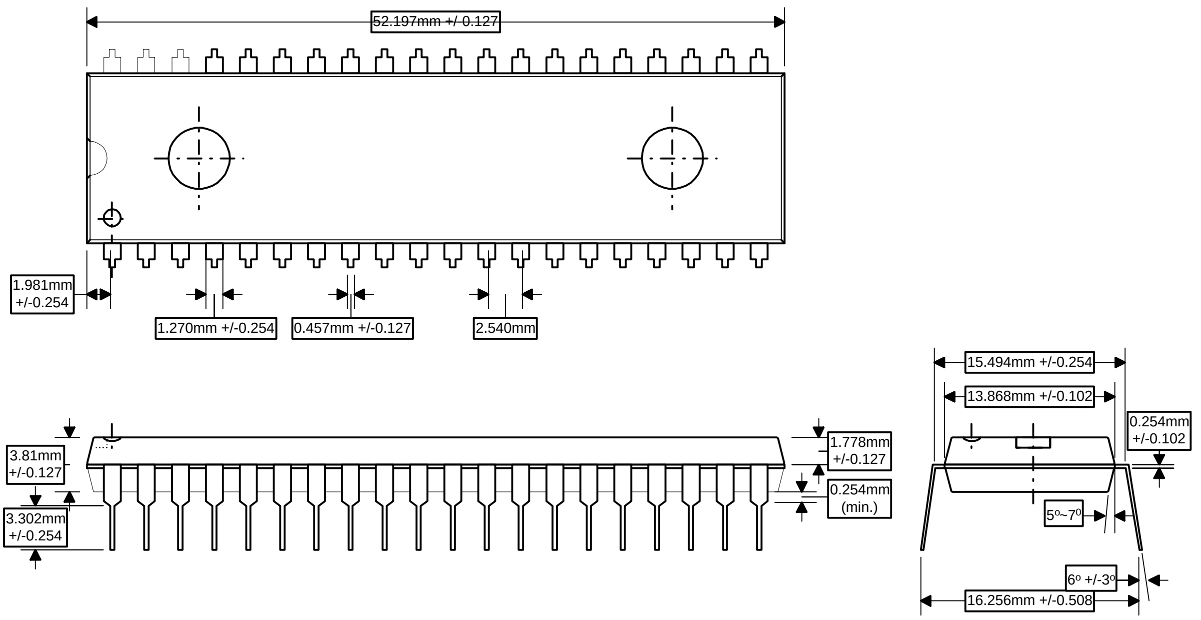
Test Mode Condition

In normal application, users should avoid the MTV312M entering its test mode or writer mode, outlined as follows, adding pull-up resistor to DA8 and DA9 pins is recommended.

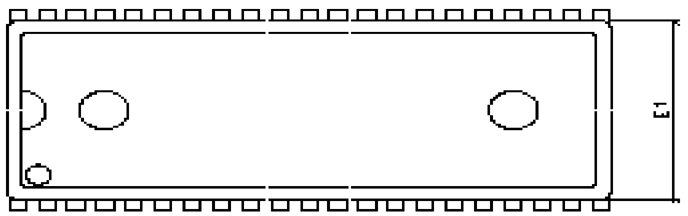
Test Mode A: RESET=1 & DA9=1 & DA8=0 & STO=0
Test Mode B: RESET's falling edge & DA9=1 & DA8=0 & STO=1
Writer Mode: RESET=1 & DA9=0 & DA8=1

PACKAGE DIMENSION

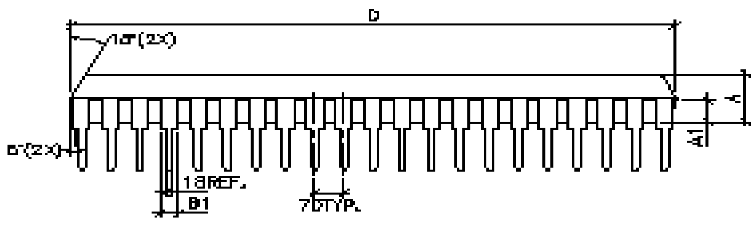
1. 40-pin PDIP 600 mil

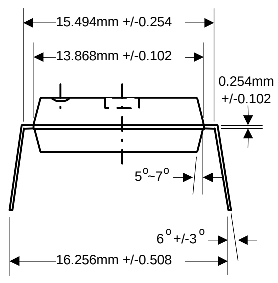


2. 42-pin SDIP Unit: mm

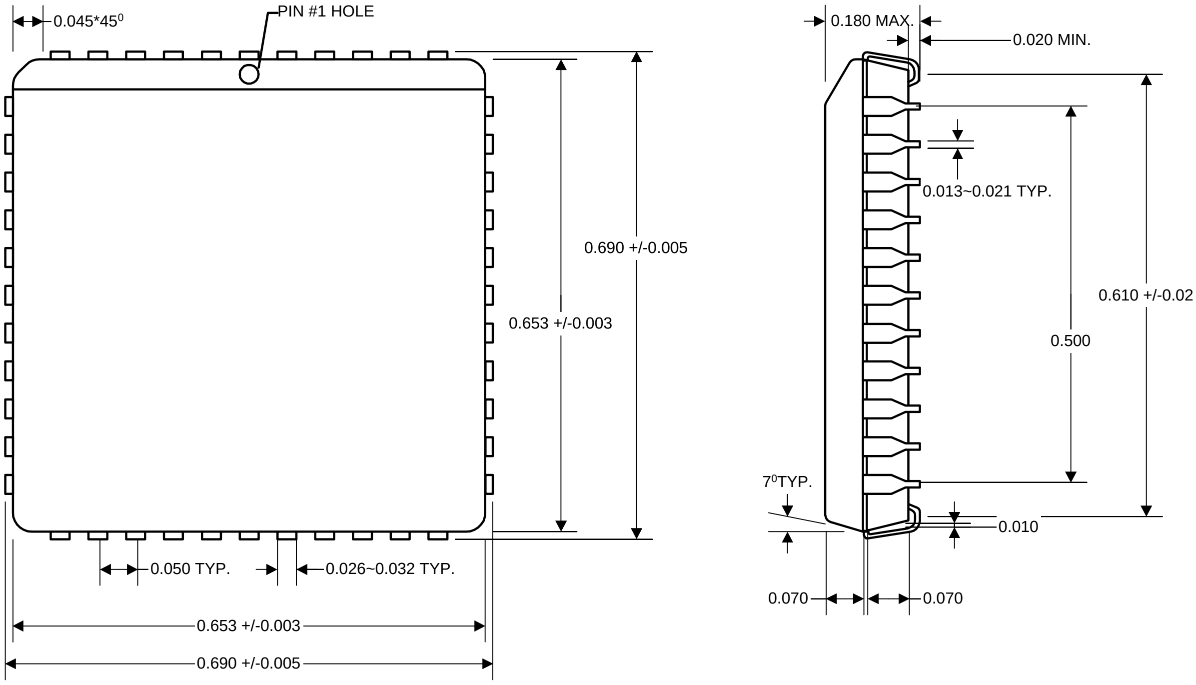


Symbol	Dimension in mm		
	Min	Nom	Max
A	3.937	4.064	4.2
A1	1.78	1.842	1.88
B1	0.914	1.270	1.118
D	36.78	36.83	36.88
E1	13.945	13.970	13.995
F	15.19	15.240	15.29
eB	15.24	16.510	17.78
θ	0°	7.5°	15°





3. 44-pin PLCC Unit:



Ordering Information

Standard Configurations:

Prefix	Part Type	Package Type	ROM Size (K)
MTV	312M	N: PDIP S: SDIP V: PLCC	64

Part Numbers:

Prefix	Part Type	Package Type	ROM Size (K)
MTV	312M	N	64
MTV	312M	S	64
MTV	312M	V	64