MYSON-CENTURY TECHNOLOGY

MTV412M (Rev 0.9)

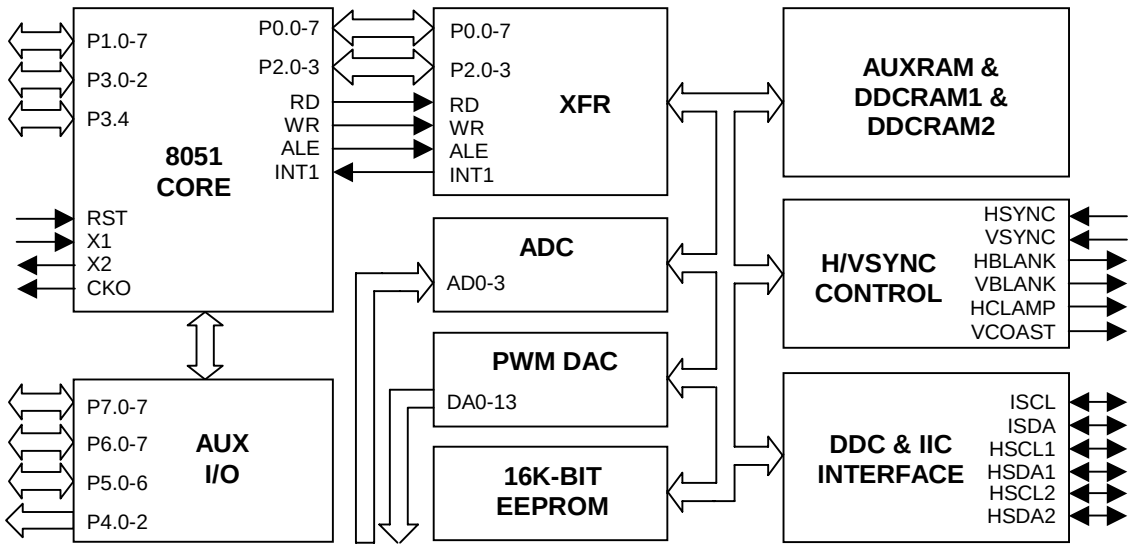
8051 Embedded Monitor Controller 128K Flash Type with ISP

FEATURES

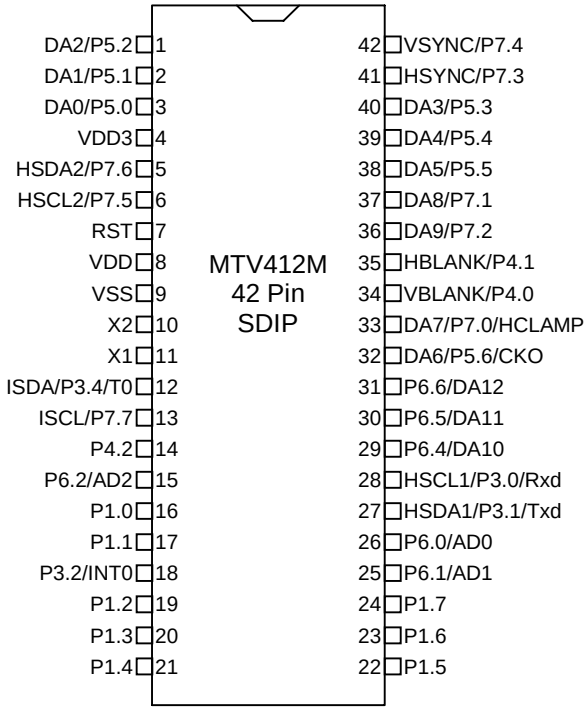
- 8051 core, 12MHz operating frequency with double CPU clock option
- 0.35um process; 3.3V/5V power supply; 5V I/O tolerant
- 1024-byte RAM; 128K-byte program Flash-ROM support In System Programming (ISP) without boot code
- Maximum 14 channels of PWM DAC
- Maximum 38 (44-pin) or 36 (42-pin) I/O pins
- SYNC processor for composite separation/insertion, H/V polarity/frequency check and polarity adjustment
- Clock output to drive other devices
- Built-in low power reset circuit
- Compliant with VESA DDC1/2B/2Bi/2B+ standard
- Triple slave IIC addresses; two H/W auto transfer DDC1/DDC2x data for both D-sub and DVI interfaces
- Single master IIC interface for internal device communication
- Maximum 4-channel 8-bit A/D converter
- Flash-ROM program code protection selection
- 42-pin SDIP or 44-pin PLCC/PQFP package

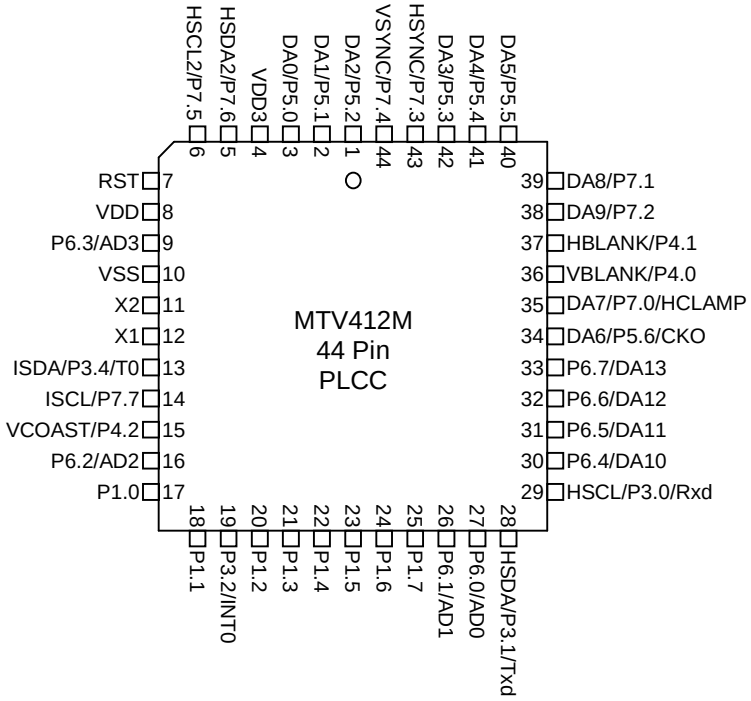
GENERAL DESCRIPTIONS

The MTV412M micro-controller is an 8051 CPU core embedded device targeted for LCD Monitor, LCD TV or smart panel applications. It includes an 8051 CPU core, 1024-byte SRAM, on-chip 16K-bit EEPROM, 14 PWM DACs, VESA DDC for both D-sub and DVI interfaces, 4-channel 8-bit ADC, hardware ISP without boot code and a 128K-byte internal program Flash-ROM in 42-pin SDIP, 44-pin PLCC/PQFP package.



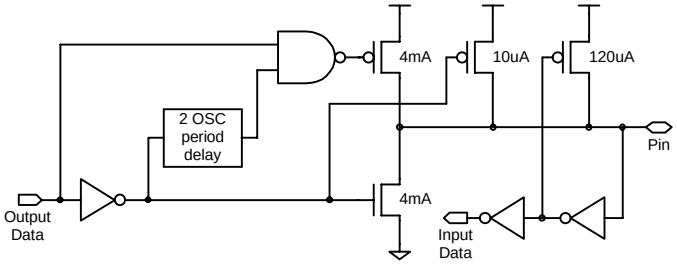
PIN CONNECTION



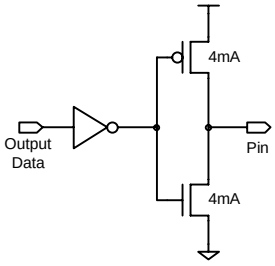


PIN CONFIGURATION

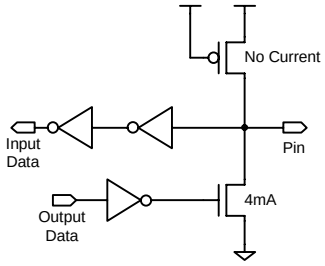
A “CMOS output pin” means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.
A “open drain pin” means it can sink at least 4mA current but only drive 10~20uA to VDD. It can be used as input or output function and needs an external pull up resistor.
A “8051 standard pin” is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.



8051 Standard Pin



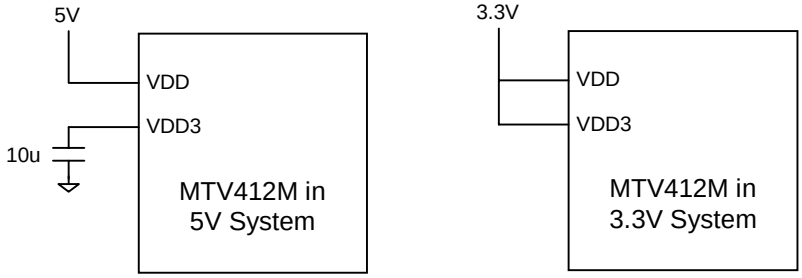
CMOS Output Pin



Open Drain Pin

POWER CONFIGURATION

The MTV412M can work on 5V or 3.3V power supply system.
In 5V power system, the VDD pin is connected to 5V power and the VDD3 needs an external capacitor, all output pins can swing from 0~5V, input pins can accept 0~5V input range. And ADC conversion range is 5V. However, X1 and X2 pins must be kept below 3.3V.
In 3.3V power system, the VDD and VDD3 are connected to 3.3V power, all output pins swing from 0~3.3V, HSYNC, VSYNC and open drain pin can accept 0~5V input range, other pins must be kept below 3.3V. And the ADC conversion range is 3.3V.



PIN DESCRIPTION

Name	PIN NO. 42	PIN NO. 44	Type	Description
VDD3	4	4	O	3.3V core power
VDD	8	8	-	5V or 3.3V Positive Power Supply
VSS	9	10	-	Ground
X2	10	11	O	Oscillator output
X1	11	12	I	Oscillator input
RST	7	7	I	Active high reset
DA0/P5.0	3	3	I/O	PWM DAC output / General purpose I/O (CMOS)
DA1/P5.1	2	2	I/O	PWM DAC output / General purpose I/O (CMOS)
DA2/P5.2	1	1	I/O	PWM DAC output / General purpose I/O (CMOS)
DA3/P5.3	40	42	I/O	PWM DAC output / General purpose I/O (CMOS)
DA4/P5.4	39	41	I/O	PWM DAC output / General purpose I/O (CMOS)
DA5/P5.5	38	40	I/O	PWM DAC output / General purpose I/O (CMOS)
DA6/P5.6/CKO	32	34	I/O	PWM DAC output / General purpose I/O / Oscillator Freq. clock output (CMOS)
DA7/P7.0/HCLAMP	33	35	I/O	PWM DAC output / General purpose I/O / Hsync clamp pulse output (CMOS)
DA8/P7.1	37	39	I/O	PWM DAC output / General purpose I/O (open drain)
DA9/P7.2	36	38	I/O	PWM DAC output / General purpose I/O (open drain)
HSCL1/P3.0/Rxd	28	29	I/O	Slave IIC 1 clock / General purpose I/O / Rxd (open drain)
HSDA1/P3.1/Txd	27	28	I/O	Slave IIC 1 data / General purpose I/O / Txd (open drain)
HSCL2/P7.5	6	6	I/O	Slave IIC 2 clock / General purpose I/O (open drain)
HSDA2/P7.6	5	5	I/O	Slave IIC 2 data / General purpose I/O (open drain)
P3.2/INT0	18	19	I/O	General purpose I/O / INT0 (8051 standard)
ISDA/P3.4/T0	12	13	I/O	Master IIC data / General purpose I/O / T0 (open drain)
ISCL/P7.7	13	14	I/O	Master IIC clock / General purpose I/O (open drain)
P1.0	16	17	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.1	17	18	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.2	19	20	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.3	20	21	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.4	21	22	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.5	22	23	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.6	23	24	I/O	General purpose I/O (CMOS output or 8051 standard)
P1.7	24	25	I/O	General purpose I/O (CMOS output or 8051 standard)
P6.0/AD0	26	27	I/O	General purpose I/O / ADC Input (CMOS)
P6.1/AD1	25	26	I/O	General purpose I/O / ADC Input (CMOS)
P6.2/AD2	15	16	I/O	General purpose I/O / ADC Input / Half Hsync input (CMOS)
P6.3/AD3	-	9	I/O	General purpose I/O / ADC Input (CMOS)
P6.4/DA10	29	30	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.5/DA11	30	31	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.6/DA12	31	32	I/O	General purpose I/O / PWM DAC output (CMOS)
P6.7/DA13	-	33	I/O	General purpose I/O / PWM DAC output (CMOS)
VBLANK/P4.0	34	36	O	Vertical blank (CMOS) / General purpose Output (CMOS)
HBLANK/P4.1	35	37	O	Horizontal blank (CMOS) / General purpose Output (CMOS)
P4.2	14	15	O	General purpose Output (CMOS)
HSYNC/P7.3	41	43	I/O	Horizontal SYNC or Composite SYNC Input / General purpose I/O (CMOS)
VSYNC/P7.4	42	44	I/O	Vertical SYNC input / General purpose I/O (CMOS)

FUNCTIONAL DESCRIPTIONS

1. 8051 CPU Core

The CPU core of MTV412M is compatible with the industry standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers, five interrupt sources and a serial interface. The CPU core fetches its program code from the 128K bytes Flash in MTV412M. It uses Port0 and Port2 to access the "external special function register" (XFR) and external auxiliary RAM (AUXRAM).
The CPU core can run at double rate when FclkE is set. Once the bit is set, the CPU runs as if a 24MHz X'tal is applied on MTV412M, but the peripherals (IIC, DDC, H/V processor) still run at the original frequency.

Note: All registers listed in this document reside in 8051's external RAM area (XFR). For internal RAM memory map, please refer to 8051 spec.

2. Memory Allocation

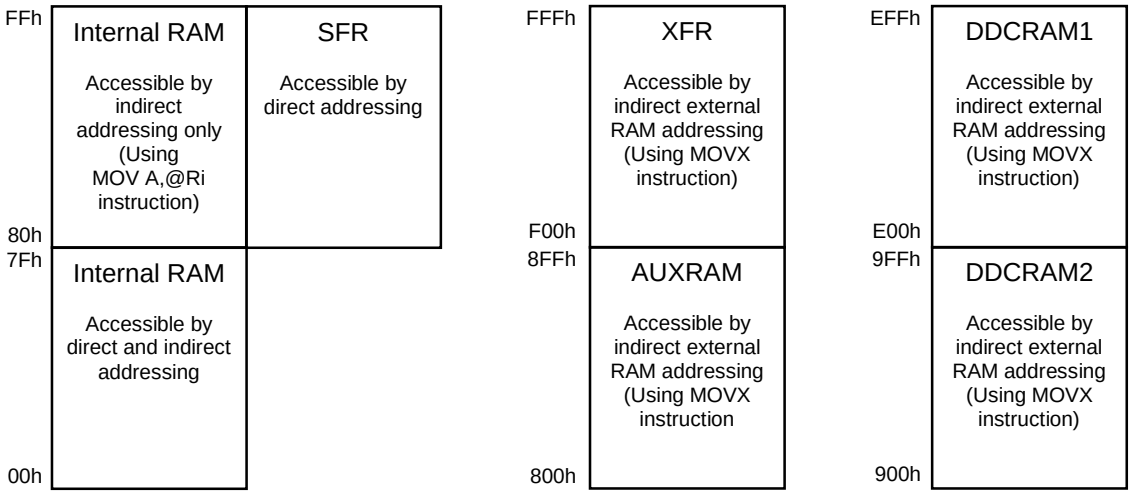
2.1 Internal Special Function Registers (SFR)
The SFR is a group of registers that are the same as standard 8051.

2.2 Internal RAM
There are total 256 bytes internal RAM in MTV412M, the same as standard 8052.

2.3 External Special Function Registers (XFR)
The XFR is a group of registers allocated in the 8051 external RAM area F00h - FFFh. These registers are used for special functions. Programs can use "MOVX" instruction to access these registers.

2.4 Auxiliary RAM (AUXRAM)
There are total 256 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - 8F Fh. Programs can use "MOVX" instruction to access the AUXRAM.

2.5 Dual Port RAM (DDCRAM1 & DDCRAM2)
There are 2x256 bytes Dual Port RAM allocated in the 8051 external RAM area 900h - 9FFh & E00h - EFFh for H/W auto transfer DDC. The external DDC1/2 Host can access the RAM as if two 24LC02 EEPROMs are connected onto the interface. The HSCL1, HSDA1 pins can access DDCRAM1 directly. And the HSCL2, HSDA2 pins can access DDCRAM2 directly. Programs can also use "MOVX" instruction to access these RAM.



3. Chip Configuration

The Chip Configuration registers define configuration of the chip and function of the pins.

Reg name	addr	bit7	bit6 bi	t5	Bit4	bit3 bi	t2 bi	t1	bit0
PADMOD	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	F51h(w)		P56E P55E		P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	HIIC1E	IIICE	HIIC2E	CKOE	HCLPE	P42E	P41E	P40E
PADMOD	F53h(w)		P56oe	P55oe	P54oe P53oe		P52oe P51oe		P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w) PW	MF	DIV253	FclkE		ENSCL	Msel	MIICF1	MIICF0
PADMOD	F5Eh(w)				P74E	P73E	P72E	P71E	P70E
PADMOD	F5Fh(w)	P77oe	P76oe	P75oe	P74oe	P73oe	P72oe	P71oe	P70oe

PADMOD (w) : Pad mode control registers. (All are "0" in Chip Reset, except for HIIC1E bit)

D A13E = 1 → Pin “P6.7/DA13” is DA13.
= 0 → Pin “P6.7/DA13” is P6.7.
D A12E = 1 → Pin “P6.6/DA12” is DA12.
= 0 → Pin “P6.6/DA12” is P6.6.
D A11E = 1 → Pin “P6.5/DA11” is DA11.
= 0 → Pin “P6.5/DA11” is P6.5.
D A10E = 1 → Pin “P6.4/DA10” is DA10.
= 0 → Pin “P6.4/DA10” is P6.4.
A D3E = 1 → Pin “P6.3/AD3” is AD3.
= 0 → Pin “P6.3/AD3” is P6.3.
A D2E = 1 → Pin “P6.2/AD2” is AD2.
= 0 → Pin “P6.2/AD2” is P6.2.
A D1E = 1 → Pin “P6.1/AD1” is AD1.
= 0 → Pin “P6.1/AD1” is P6.1.
A D0E = 1 → Pin “P6.0/AD0” is AD0.
= 0 → Pin “P6.0/AD0” is P6.0.
P56E = 1 → Pin “DA6/P5.6/CKO” is P5.6.
= 0 → Pin “DA6/P5.6/CKO” is DA6/CKO selected by CKOE bit.
P55E = 1 → Pin “DA5/P5.5” is P5.5.
= 0 → Pin “DA5/P5.5” is DA5.
P54E = 1 → Pin “DA4/P5.4” is P5.4.
= 0 → Pin “DA4/P5.4” is DA4.
P53E = 1 → Pin “DA3/P5.3” is P5.3.
= 0 → Pin “DA3/P5.3” is DA3.
P52E = 1 → Pin “DA2/P5.2” is P5.2.
= 0 → Pin “DA2/P5.2” is DA2.
P51E = 1 → Pin “DA1/P5.1” is P5.1.
= 0 → Pin “DA1/P5.1” is DA1.
P50E = 1 → Pin “DA0/P5.0” is P5.0.
= 0 → Pin “DA0/P5.0” is DA0.
HI IC1E = 1 → Pin “HSCL1/P3.0/Rxd” is HSCL1; pin “HSDA1/P3.1/Txd” is HSDA1.
= 0 → Pin “HSCL1/P3.0/Rxd” is P3.0/Rxd; pin “HSDA1/P3.1/Txd” is P3.1/Txd.
II ICE = 1 → Pin “ISDA/P3.4/T0” is ISDA; pin “ISCL/P7.7” is ISCL.
= 0 → Pin “ISDA/P3.4/T0” is P3.4/T0; pin “ISCL/P7.7” is P7.7.
HIIC2E = 1 → Pin “HSCL2/P7.5” is HSCL2. Pin “HSDA2/P7.6” is HSDA6.
= 0 → Pin “HSCL2/P7.5” is P7.5. Pin “HSDA2/P7.6” is P7.6.

	CKOE = 1	→ Pin “DA6/P5.6/CKO is CKO if P56E = 0.
	= 0	→ Pin “DA6/P5.6/CKO” is DA6 if P56E = 0.
	HCLPE = 1	→ Pin “DA7/P7.0/HCLAMP” is HCLAMP if P70E = 0.
	= 0	→ Pin “DA7/P7.0/HCLAMP” is DA7 if P70E = 0.
	P42E = 1	→ Pin “P4.2” is P4.2.
	= 0	→ Reserved
	P41E = 1	→ Pin “HBLANK/P4.1” is P4.1.
	= 0	→ Pin “HBLANK/P4.1” is HBLANK.
	P40E = 1	→ Pin “VBLANK/P4.0” is P4.0.
	= 0	→ Pin “VBLANK/P4.0” is VBLANK.
P56oe	= 1	→ P5.6 is output pin.
	= 0	→ P5.6 is input pin.
P55oe	= 1	→ P5.5 is output pin.
	= 0	→ P5.5 is input pin.
P54oe	= 1	→ P5.4 is output pin.
	= 0	→ P5.4 is input pin.
P53oe	= 1	→ P5.3 is output pin.
	= 0	→ P5.3 is input pin.
P52oe	= 1	→ P5.2 is output pin.
	= 0	→ P5.2 is input pin.
P51oe	= 1	→ P5.1 is output pin.
	= 0	→ P5.1 is input pin.
P50oe	= 1	→ P5.0 is output pin.
	= 0	→ P5.0 is input pin.
P67oe	= 1	→ P6.7 is output pin.
	= 0	→ P6.7 is input pin.
P66o e	= 1	→ P6.6 is output pin.
	= 0	→ P6.6 is input pin.
P65oe	= 1	→ P6.5 is output pin.
	= 0	→ P6.5 is input pin.
P64oe	= 1	→ P6.4 is output pin.
	= 0	→ P6.4 is input pin.
P63oe	= 1	→ P6.3 is output pin.
	= 0	→ P6.3 is input pin.
P62oe	= 1	→ P6.2 is output pin.
	= 0	→ P6.2 is input pin.
P61oe	= 1	→ P6.1 is output pin.
	= 0	→ P6.1 is input pin.
P60oe	= 1	→ P6.0 is output pin.
	= 0	→ P6.0 is input pin.
	COP17 = 1	→ Pin “P1.7” is CMOS Output.
	= 0	→ Pin “P1.7” is 8051 standard I/O.
	COP16 = 1	→ Pin “P1.6” is CMOS Output.
	= 0	→ Pin “P1.6” is 8051 standard I/O.
	COP15 = 1	→ Pin “P1.5” is CMOS Output.
	= 0	→ Pin “P1.5” is 8051 standard I/O.
	COP14 = 1	→ Pin “P1.4” is CMOS Output.
	= 0	→ Pin “P1.4” is 8051 standard I/O.
	COP13 = 1	→ Pin “P1.3” is CMOS Output.
	= 0	→ Pin “P1.3” is 8051 standard I/O.
	COP12 = 1	→ Pin “P1.2” is CMOS Output.
	= 0	→ Pin “P1.2” is 8051 standard I/O.

COP11 = 1 → Pin “P1.1” is CMOS Output.
= 0 → Pin “P1.1” is 8051 standard I/O.
COP10 = 1 → Pin “P1.0” is CMOS Output.
= 0 → Pin “P1.0” is 8051 standard I/O.
P74E = 1 → Pin “VSYNC/P7.4” is P7.4.
= 0 → Pin “VSYNC/P7.4” is VSYNC.
P73E = 1 → Pin “HSYNC/P7.3” is P7.3.
= 0 → Pin “HSYNC/P7.3” is HSYNC.
P72E = 1 → Pin “DA9/P7.2” is P7.2.
= 0 → Pin “DA9/P7.2” is DA9.
P71E = 1 → Pin “DA8/P7.1” is P7.1.
= 0 → Pin “DA8/P7.1” is DA8.
P70E = 1 → Pin “DA7/P7.0/HCLAMP” is P7.0.
= 0 → Pin “DA7/P7.0/HCLAMP" is DA7/HCLAMP selected by HCLPE bit.
P77oe = 1 → P7.7 is output pin.
= 0 → P7.7 is input pin.
P76oe = 1 → P7.6 is output pin.
= 0 → P7.6 is input pin.
P75oe = 1 → P7.5 is output pin.
= 0 → P7.5 is input pin.
P74oe = 1 → P7.4 is output pin.
= 0 → P7.4 is input pin.
P73oe = 1 → P7.3 is output pin.
= 0 → P7.3 is input pin.
P72oe = 1 → P7.2 is output pin.
= 0 → P7.2 is input pin.
P71oe = 1 → P7.1 is output pin.
= 0 → P7.1 is input pin.
P70oe = 1 → P7.0 is output pin.
= 0 → P7.0 is input pin.

OPTION (w) : Chip option configuration (All are "0" in Chip Reset).
PWMF = 1 → Selects 94KHz PWM frequency.
= 0 → Selects 47KHz PWM frequency.
DIV253 = 1 → PWM pulse width is 253-step resolution.
= 0 → PWM pulse width is 256-step resolution.
Fcl kE = 1 → CPU is running at double rate
= 0 → CPU is running at normal rate
ENSCL = 1 → Enable slave IIC block to hold HSCL pin low while MTV412M is unable to catch-up with the external master's speed.
Msel = 1 → Master IIC block connect to HSCL1/HSDA1 pins.
= 0 → Master IIC block connect to ISCL/ISDA pins.
MIICF1,MIICF0 = 1,1 → Selects 400KHz Master IIC frequency.
= 1,0 → Selects 200KHz Master IIC frequency.
= 0,1 → Selects 50KHz Master IIC frequency.
= 0,0 → Selects 100KHz Master IIC frequency.

4. I/O Ports

4.1 Port1
Port1 is a group of pseudo open drain pins or CMOS output pins. It can be used as general purpose I/O. Behavior of Port1 is the same as standard 8051.

4.2 P3.0-2, P3.4
If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Behavior of Port3 is the same as standard 8051.

4.3 Port4, Port5, Port6 and Port7
Port5, Port6 and Port7 are used as general purpose I/O. S/W needs to set the corresponding P5(n)oe, P6(n)oe and P7(n)oe to define whether these pins are input or output. Port4 is pure output.

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42
PORT7	F70h(r/w)								P70
PORT7	F71h(r/w)								P71
PORT7	F72h(r/w)								P72
PORT7	F73h(r/w)								P73
PORT7	F74h(r/w)								P74
PORT7	F75h(r/w)								P75
PORT7	F76h(r/w)								P76
PORT7	F77h(r/w)								P77

PORT5 (r/w) : Port 5 data input/output value.

PORT6 (r/w) : Port 6 data input/output value.

PORT4 (w) : Port 4 data output value.

PORT7 (r/w) : Port 7 data input/output value.

5. PWM DAC

Each output pulse width of PWM DAC converter is controlled by an 8-bit register in XFR. The frequency of

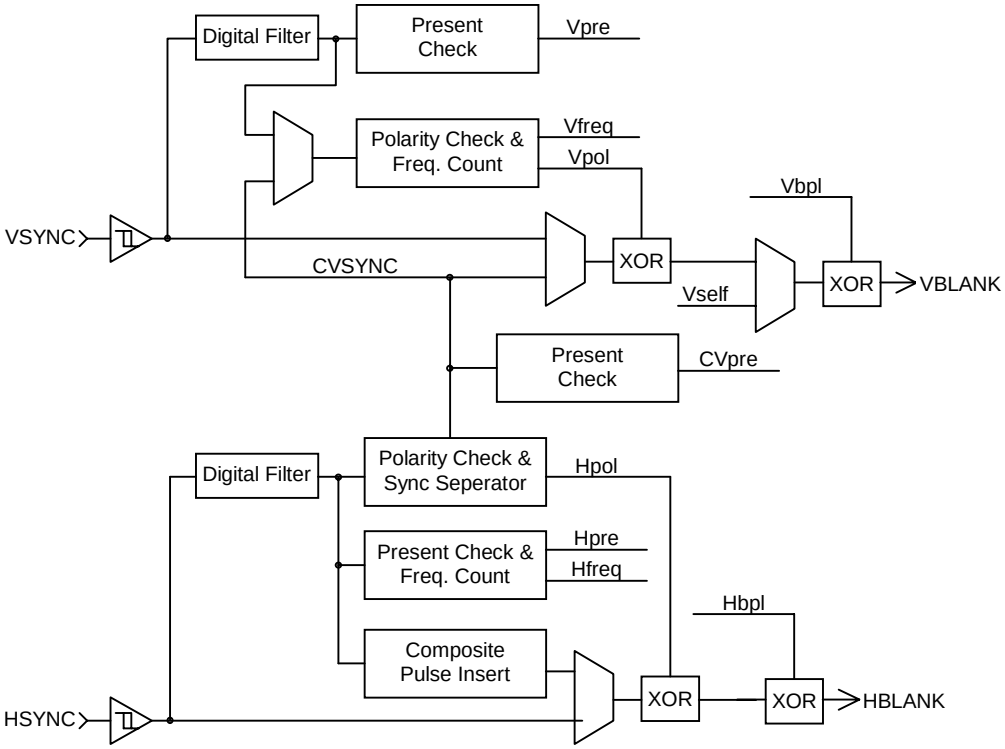
PWM clock is 47KHz or 94KHz, selected by PWMF. And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to DAC register generates stable high output. If DIV253=0, the output pulses low at least once even if the DAC register's content is FFH. Writing 00H to DAC register generates stable low output.

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							
DA6	F26h(r/w)	Pulse width of PWM DAC 6							
DA7	F27h(r/w)	Pulse width of PWM DAC 7							
DA8	F28h(r/w)	Pulse width of PWM DAC 8							
DA9	F29h(r/w)	Pulse width of PWM DAC 9							
DA10	F2Ah(r/w)	Pulse width of PWM DAC 10							
DA11	F2Bh(r/w)	Pulse width of PWM DAC 11							
DA12	F2Ch(r/w)	Pulse width of PWM DAC 12							
DA13	F2Dh(r/w)	Pulse width of PWM DAC 13							

DA0-13 (r/w) : The output pulse width control for DA0-13.
* All of PWM DAC converters are centered with value 80h after power on.

6. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation/insertion. SYNC inputs presence check, frequency counting, polarity detection and control, as well as the protection of VBLANK output while VSYNC speeds up in high DDC communication clock rate.
Based on the digital filter, the HSYNC present and frequency function block treat any pulse longer than the specified time period as pulse, and the specified time period is controlled by (DF1,DF0) bits. The VSYNC digital filter has no control bit. It works as (DF1,DF0) = (0, 0) of HSYNC.



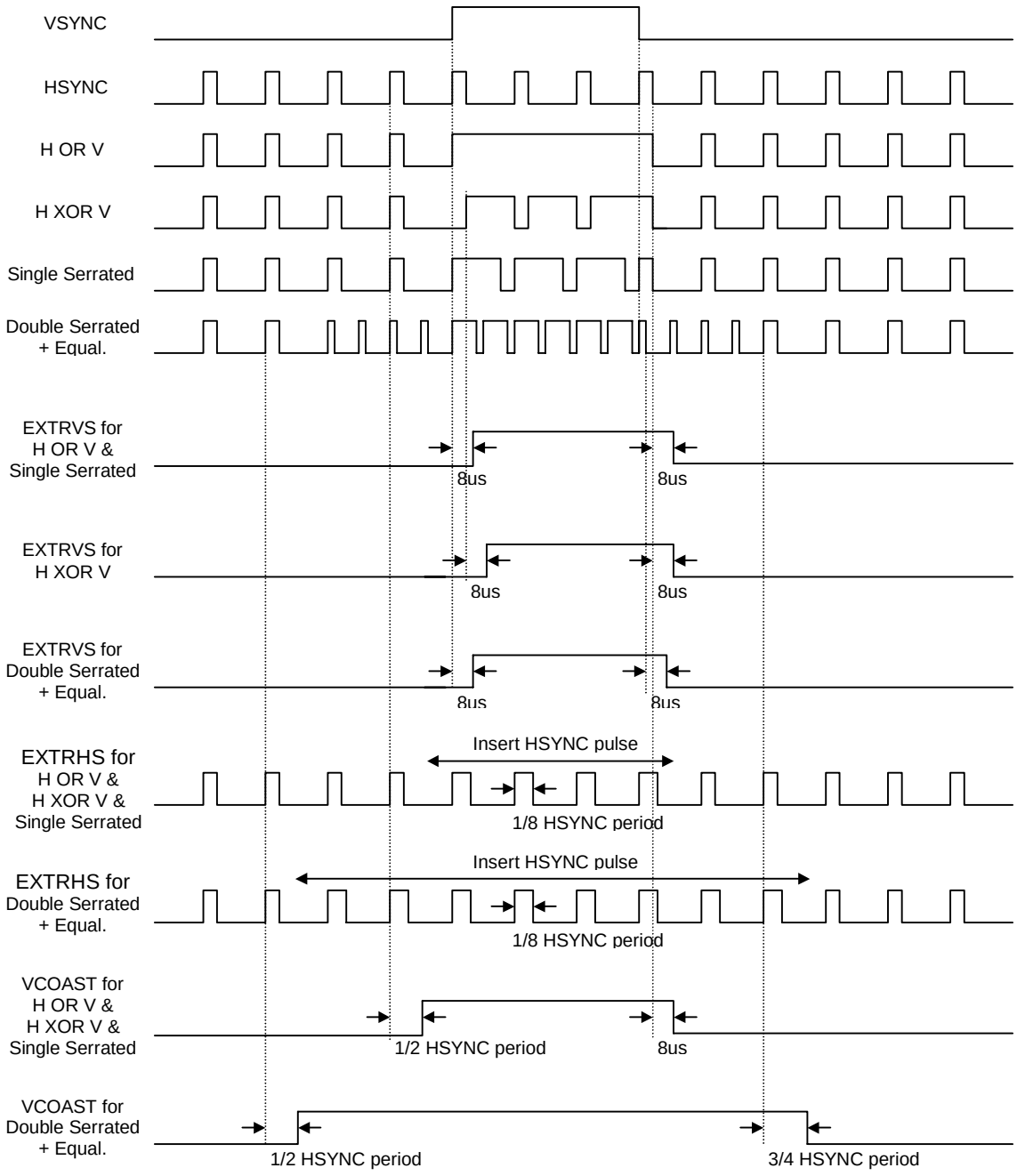
H/V SYNC Processor Block Diagram

6.1 Composite SYNC separation/insertion

The MTV412M continuously monitors the input HSYNC. If the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and users can select the extracted "CVSYNC" for the source of polarity check, frequency count, and VBLANK output. The CVSYNC then has 8us delay compared to the original signal. The MTV412M can also insert pulse to HBLANK output during composite VSYNC's active time. The width of insert pulse is 1/8 HSYNC period and the insertion frequency can adapt to original HSYNC. The insert pulse of HBLANK can be disabled or enabled by setting "NoHins" control bit. If "NoHins" bit is set to "1", HBLANK output will be same as HSYNC input (of course, polarity can be controlled by HBpl bit).

6.2 H/V Frequency Counter

MTV412M can discriminate HSYNC/VSYNC frequency and save the information in XFRs. The 14-bit Hcounter counts the time of 64xHSYNC period, then loads the result into the HCNTH/HCNTL latch. The output value is then [(128000000/H-Freq) - 1], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present. The 12-bit Vcounter counts the time between two VSYNC pulses, then loads the result into the VCNTH/VCNTL latch. The output value is then (62500/V-Freq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is set when VCNT/HCNT value changes or overflows. Table 6.2.1 and Table 6.2.2 show the HCNT/VCNT value under the operations of 12MHz.



Timing Relationship of Composite SYNC signal Separation/Insertion when "NoHins" = 0

6.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (14 bits)
		12MHz OSC (hex / dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

6.2.2 V-Freq Table

V-Freq(Hz)		Output value (12bits)
		12MHz OSC (hex / dec)
1	56	45Ch / 1116
2	60	411h / 1041
3	70	37Ch / 892
4	72	364h / 868
5	75	341h / 833
6	85	2DFh / 735

6.3 H/V Present Check

The Hpresent function checks the input HSYNC pulse, and the Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse, and the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value change.

6.4 H/V Polarity Detect

The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

6.5 Output HBLANK/VBLANK Control and Polarity Adjust

The HBLANK is the mux output of HSYNC and composite Hpulse. The VBLANK is the mux output of VSYNC and CVSYNC. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 250Hz. The HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

6.6 VSYNC Coast Pulse Output

This output pin define the period of ADC PLL which is needed to disable locking for composite sync. The output polarity of VCOAST are S/W controllable.

6.7 HSYNC Clamp Pulse Output

The HCLAMP output is activated by setting “HCLPE” control bit. The leading edge position, pulse width and polarity of HCLAMP are S/W controllable.

6.8 VSYNC Interrupt

The MTV412M checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC flag is set each time when MTV412M detects a VSYNC pulse. he flag is cleared by S/W writing a "0".

6.9 H/V SYNC Processor Register

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
HVSTUS	F40h(r) C	Vpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12 H	F11 H	F10	HF9	HF8
HCNTL	F42h(r)	HF7 H	F6 H	F5 H	F4 H	F3	HF2 H	F1 H	F0
VCNTH	F43h(r) V	ov f				VF11 VF	10	VF9	VF8
VCNTL	F44h(r)	VF7 VF	6 VF	5	VF4 VF	3 VF	2 VF	1 VF	0
HVCTR0	F40h(w)	C1	C0	NoHins				HBpl	VBpl
HVCTR2	F42h(w)								
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2 CL	PW1 CL	PW0		
HVCTR4	F44h(w)							DF1	DF0
INTFLG	F48h(r/w) H	PRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h(w) EH	PR	EVPR	EHPL	EVPL	EHF	EVF		EVsync

HVSTUS (r) : The status of polarity, present and static level for HSYNC and VSYNC.

C Vpre = 1 → The extracted CVSYNC is present.
= 0 → The extracted CVSYNC is not present.

H pol = 1 → HSYNC input is positive polarity.
= 0 → HSYNC input is negative polarity.

V pol = 1 → VSYNC (CVSYNC) is positive polarity.
= 0 → VSYNC (CVSYNC) is negative polarity.

H pre = 1 → HSYNC input is present.
= 0 → HSYNC input is not present.

V pre = 1 → VSYNC input is present.
= 0 → VSYNC input is not present.

H off* = 1 → Off level of HSYNC input is high.
= 0 → Off level of HSYNC input is low.

V off* = 1 → Off level of VSYNC input is high.
= 0 → Off level of VSYNC input is low.

*H off and V_{off} are valid when $H_{pre=0}$ or $V_{pre=0}$.

HCNTH (r) : H-Freq counter's high bits.

Ho vf = 1 → H-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
HF13 - HF8 : 6 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low byte.

VCNTH (r) : V-Freq counter's high bits.

Vov f = 1 → V-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
VF11 - 8 : 4 high bits of V-Freq counter.

VCNTL (r) : V-Freq counter's low byte.

HVCTR0 (w) : H/V SYNC processor control register 0.

C1 , C0 = 1,1 → Selects CVSYNC as the polarity, freq and VBLANK source.
= 1,0 → Selects VSYNC as the polarity, freq and VBLANK source.
= 0,0 → Disables composite function.
= 0,1 → H/W automatically switches to CVSYNC when CVpre=1 and VSpre=0.

NoHins = 1 → HBLANK has no insert pulse in composite mode.
= 0 → HBLANK has insert pulse in composite mode.

HB pl = 1 → Negative polarity HBLANK output.
= 0 → Positive polarity HBLANK output.

VB pl = 1 → Negative polarity VBLANK output.
= 0 → Positive polarity VBLANK output.

HVCTR3 (w) : HSYNC clamp pulse control register.
CL PEG = 1 → Clamp pulse follows HSYNC leading edge.
= 0 → Clamp pulse follows HSYNC trailing edge.
CL PPO = 1 → Positive polarity clamp pulse output.
= 0 → Negative polarity clamp pulse output.
CLPW2 : CLPW0 : Pulse width of clamp pulse is
[(CLPW2:CLPW0) + 1] x 0.167 μs for 12MHz X'tal selection.

HVCTR4 (w) :
DF1, DF0 :
= 0,0 → The digital filter will treat any HSYNC pulse shorter than one OSC period (83.33ns) as noise, between one and two OSC period (83.33ns to 166.67ns) as unknown region, and longer than two OSC period (166.67ns) as pulse.
= 0,1 → The digital filter will treat any HSYNC pulse shorter than half OSC period (41.66ns) as noise, between half and one OSC period (41.66ns to 83.33ns) as unknown region, and longer than one OSC period (83.33ns) as pulse.
= 1,x → Disable the digital filter for HSYNC.

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the INT1 source of 8051 core will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.
HP Rchg = 1 → No action.
= 0 → Clears HSYNC presence change flag.
VP Rchg = 1 → No action.
= 0 → Clears VSYNC presence change flag.
H PLchg = 1 → No action.
= 0 → Clears HSYNC polarity change flag.
VP Lchg = 1 → No action.
= 0 → Clears VSYNC polarity change flag.
HFc hg = 1 → No action.
= 0 → Clears HSYNC frequency change flag.
V Fchg = 1 → No action.
= 0 → Clears VSYNC frequency change flag.
Vs ync = 1 → No action.
= 0 → Clears VSYNC interrupt flag.

INTFLG (r) : Interrupt flag.
HP Rchg = 1 → Indicates a HSYNC presence change.
VP Rchg = 1 → Indicates a VSYNC presence change.
H PLchg = 1 → Indicates a HSYNC polarity change.
VP Lchg = 1 → Indicates a VSYNC polarity change.
HFc hg = 1 → Indicates a HSYNC frequency change or counter overflow.
V Fchg = 1 → Indicates a VSYNC frequency change or counter overflow.
Vs ync = 1 → Indicates a VSYNC interrupt.

INTEN (w) : Interrupt enable.
EH PR = 1 → Enables HSYNC presence change interrupt.
EV PR = 1 → Enables VSYNC presence change interrupt.
EH PL = 1 → Enables HSYNC polarity change interrupt.
EV PL = 1 → Enables VSYNC polarity change interrupt.
EH F = 1 → Enables HSYNC frequency change / counter overflow interrupt.

EV F = 1 → Enables VSYNC frequency change / counter overflow interrupt.
E Vsync = 1 → Enables VSYNC interrupt.

7. DDC & IIC Interface

7.1 DDC1/DDC2x Mode, DDCRAM1/DDCRAM2 and SlaveA1/SlaveA2 block

The MTV412M supports VESA DDC for both D-sub and DVI interfaces through HSCL1/HSDA1 and HSCL2/HSDA2 pins. The HSCL1/HSDA1 pins access DDCRAM1 by SlaveA1, and the HSCL2/HSDA2 pins access DDCRAM2 by SlaveA2. The MTV412M enters DDC1 mode for both DDC channels after Reset. In this mode, VSYNC is used as data clock. The HSCL1/HSCL2 pin should remain at high. The data output to the HSDA1/HSDA2 pin is taken from a shift register in MTV412M. The shift register automatically fetches EDID data from the lower 128 bytes of the Dual Port RAM (DDCRAM1/DDCRAM2), then sends it in 9-bit packet formats inclusive of a null bit (=1) as packet separator. S/W may enable/disable the DDC1 function by setting/clearing the DDC1en control bit.
The MTV412M switches to DDC2x mode when it detects a high to low transition on the HSCL1/HSCL2 pin. In this mode, the SlaveA1/SlaveA2 IIC block automatically transmits/receives data to/from the IIC Master. The transmitted/received data is taken-from/saved-to the DDC RAM1/DDCRAM2. In simple words, MTV412M can behaves as two 24LC02 EEPROMs. The only thing S/W needs to do is to write the EDID data to DDCRAM1/DDCRAM2. These slave address of SlaveA1/SlaveA2 block can be chosen by S/W as 5-bit, 6-bit or 7-bit. For example, if S/W chooses 5-bit slave address as 10100b, the SlaveA1 IIC block then responds to slave address 10100xxb. The SlaveA1/SlaveA2 can be enabled/disabled by setting/clearing the EnslvA1/EnslvA2 bit. The lower/upper DDCRAM1/DDCRAM2 can/cannot be written by the IIC Master by setting/clearing the EN128w/En256w bit. Besides, if the Only128 control bit is set, the SlaveA1/SlaveA2 only accesses the lower 128 bytes of the DDCRAM1/DDCRAM2.
The MTV412M returns to DDC1 mode if HSCL1 is kept high for 128 VSYNC clock period. However, it locks in DDC2B mode if a valid IIC address (1010xxxb) has been detected on HSCL1/HSDA1 buses. The DDC2 flag reflects the current DDC status, S/W may clear it by writing a "0" to it.

7.2 SlaveB Block
The SlaveB IIC block is connected to HSDA1 and HSCL1 pins only. This block can receive/transmit data using IIC protocols. S/W may write the SLVBADR register to determine the slave addresses.
In receive mode, the block first detects IIC slave address matching the condition then issues a SlvBMI interrupt. The data from HSDA1 is shifted into shift register then written to RCBBUF register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCBI (receives buffer full interrupt) every time when the RCBBUF is loaded. If S/W is not able to read out the RCBBUF in time, the next byte in shift register is not written to RCBBUF and the slave block returns NACK to the master. This feature guarantees the data integrity of communication. The WadrB flag can tell S/W whether the data in RCBBUF is a word address or not.
In transmit mode, the block first detects IIC slave address matching the condition, then issues a SlvBMI interrupt. In the meantime, the data pre-stored in the TXBBUF is loaded into shift register, resulting in TXBBUF emptying and generates a TXBI (transmit buffer empty interrupt). S/W should write the TXBBUF a new byte for the next transfer before shift register empties. A failure of this process causes data corrupt. The TXBI occurs every time when shift register reads out the data from TXBBUF.
The SlvBMI is cleared by writing "0" to corresponding bit in INTFLG register. The RCBI is cleared by reading out RCBBUF. The TXBI is cleared by writing TXBBUF.

*Please refer to the attachments about "Slave IIC Block Timing".

7.3 Master Mode IIC Function Block
The master mode IIC block can be connected to the ISDA /ISCL pins or the HSDA1/HSCL1 pins, selected by Msel control bit. Its speed can be selected within the range of 50KHz-400KHz by S/W setting the MIICF1/MIICF0 control bit. The software program can access the external IIC device through this interface. A summary of master IIC access is illustrated as follows.

7.3.1. To write IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV412M transmits this byte, a MbufI interrupt is triggered.
4. Programs can write MBUF to transfer next byte or set P bit to stop.

* Please refer to the attachments about "Master IIC Transmit Timing".

7.3.2. To read IIC Device
1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV412M transmits this byte, a MbufI interrupt is triggered.
4. Set or reset the MAckO flag according to the IIC protocol.
5. Read out MBUF the useless byte to continue the data transfer.
6. After the MTV412M receives a new byte, the MbufI interrupt is triggered again.
7. Read MBUF also trigger the next receive operation, but set P bit before read can terminate the operation.

* Please refer to the attachments about "Master IIC Receive Timing".

Reg name	addr	bit7 bi	t6	bit5	bit4 bi	t3	bit2	bit1	bit0
IICCTR	F00h (r/w)	DDC2A1	DDC2A2				MAckO	P	S
IICSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MAckIn
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	STOPI	ReStaI	WslvA1I	WslvA2I	MbufI
INTFLG	F03h (w)			SlvBMI	STOPI	ReStaI	WslvA1I	WslvA2I	MbufI
INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ESTOPI	EReStaI	EWSlvA1I	EWSlvA2I	EMbufI
MBUF	F05h (r/w)	Master IIC receive/transmit data buffer							
DDCCTRA1	F06h (w)	DDC1en	En128W	En256W	Only128		Sl	vA1bs1	SlvA1bs0
SLVA1ADR	F07h (w)	ENSlvA1	Slave A1 IIC address						
RCBBUF	F08h (r)	Slave B IIC receive buffer							
TXBBUF	F08h (w)	Slave B IIC transmit buffer							
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address						
DDCCTRA2	F86h (w)	DDC1en	En128W	En256W	Only128		Sl	vA2bs1	SlvA2bs0
SLVA2ADR	F87h (w)	ENSlvA2	Slave A2 IIC address						

IICCTR (r/w) : IIC interface status/control register.

DDC2A1 = 1 → DDC2 is active for HSCL1/HSDA1 pins.
= 0 → MTV412M remains in DDC1 mode for HSCL1/HSDA1 pins.
DDC2A2 = 1 → DDC2 is active for HSCL2/HSDA2 pins.
= 0 → MTV412M remains in DDC1 mode for HSCL2/HSDA2 pins.
M AckO = 1 → In master receive mode, NACK is returned by MTV412M.
= 0 → In master receive mode, ACK is returned by MTV412M.
S, P = ↑, 0 → Start condition when Master IIC is not during transfer.
= X, ↑ → Stop condition when Master IIC is not during transfer.
= 1, X → Resume transfer after a read/write MBUF operation.

IICSTUS (r) : IIC interface status register.

Wa drB = 1 → The data in RCBBUF is word address.
SlvRWB = 1 → Current transfer is slave transmit
= 0 → Current transfer is slave receive
SA ckIn = 1 → The external IIC host respond NACK.
SLV S = 1 → The slave block has detected a START, cleared when STOP detected.
MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.
= 0 → ACK received from the slave IIC device.

INTFLG (w) : Interrupt flag. A interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

Sl	vBMI	= 1	→ No action.
		= 0	→ Clears SlvBMI flag.
ST	OPI	= 1	→ No action.
		= 0	→ Clears STOPI flag.
	ReStaI	= 1	→ No action.
		= 0	→ Clears ReStaI flag.
	WslvA1I	= 1	→ No action.
		= 0	→ Clears WslvA1I flag.
	WslvA2I	= 1	→ No action.
		= 0	→ Clears WslvA2I flag.
M	bufI	= 1	→ No action.
		= 0	→ Clears Master IIC bus interrupt flag (MbufI).

INTFLG (r) : Interrupt flag.

T	XBI	= 1	→ Indicates the TXBBUF need a new data byte, cleared by writing TXBBUF.
RC	BI	= 1	→ Indicates the RCBBUF has received a new data byte, cleared by reading RCBBUF.
Sl	vBMI	= 1	→ Indicates the slave IIC address B match condition.
ST	OPI	= 1	→ Indicates the slave IIC has detected a STOP condition for HSCL1/HSDA1 pins.
	ReStaI	= 1	→ Indicates the slave IIC has detected a repeat START condition for HSCL1/HSDA1 pins.
	WslvA1I	= 1	→ Indicates the slave A1 IIC has detected a STOP condition of write mode.
	WslvA2I	= 1	→ Indicates the slave A2 IIC has detected a STOP condition of write mode.
Mb	ufI	= 1	→ Indicates a byte is sent/received to/from the master IIC bus.

INTEN (w) : Interrupt enable.

ET	XBI	= 1	→ Enables TXBBUF interrupt.
ER	CBI	= 1	→ Enables RCBBUF interrupt.
	ESlvBMI	= 1	→ Enables slave address B match interrupt.
	ESTOPI	= 1	→ Enables IIC bus STOP interrupt.
	EReStaI	= 1	→ Enables IIC bus repeat START interrupt.
	EWSlvA1I	= 1	→ Enables slave A1 IIC bus STOP of write mode interrupt.
	EWSlvA2I	= 1	→ Enables slave A2 IIC bus STOP of write mode interrupt.
EM	bufI	= 1	→ Enables Master IIC bus interrupt.

Mbuf (w) : Master IIC data shift register, after START and before STOP condition, write this register resumes MTV412M's transmission to the IIC bus.

Mbuf (r) : Master IIC data shift register, after START and before STOP condition, read this register resumes MTV412M's reception from the IIC bus.

DDCCTRA1 (w) : DDC interface control register for HSCL1, HSDA1 pins.

DDC1en	= 1	→ Enables DDC1 data transfer in DDC1 mode.
	= 0	→ Disables DDC1 data transfer in DDC1 mode.
En128W	= 1	→ The lower 128 bytes (00-7F) of DDCRAM1 can be written by IIC master.
	= 0	→ The lower 128 bytes (00-7F) of DDCRAM1 cannot be written by IIC master.
En256W	= 1	→ The higher 128 bytes (80-FF) of DDCRAM1 can be written by IIC master.
	= 0	→ The higher 128 bytes (80-FF) of DDCRAM1 cannot be written by IIC master.
Only128	= 1	→ The SlaveA1 always accesses EDID data from the lower 128 bytes of DDCRAM1.
	= 0	→ The SlaveA1 accesses EDID data from the whole 256 bytes DDCRAM1.

SlvA1bs1,SlvA1bs0 : Slave IIC block A1's slave address length.

= 1,0 → 5-bit slave address.
= 0,1 → 6-bit slave address.
= 0,0 → 7-bit slave address.

SLVA1ADR (w) : Slave IIC block A1's enable and address.
E nslvA1= 1 → Enables slave IIC block A1.
= 0 → Disables slave IIC block A1.
bit6-0 : Slave IIC address A1 to which the slave block should respond.

RCBBUF (r) : Slave IIC block B receives data buffer.

TXBBUF (w) : Slave IIC block B transmits data buffer.

SLVBADR (w) : Slave IIC block B's enable and address.
E NslvB = 1 → Enables slave IIC block B.
= 0 → Disables slave IIC block B.
bit6-0 : Slave IIC address B to which the slave block should respond.

DDCCTRA2 (w) : DDC interface control register for HSCL2, HSDA2 pins.
DDC1en = 1 → Enables DDC1 data transfer in DDC1 mode.
= 0 → Disables DDC1 data transfer in DDC1 mode.
En128W = 1 → The lower 128 bytes (00-7F) of DDCRAM2 can be written by IIC master.
= 0 → The lower 128 bytes (00-7F) of DDCRAM2 cannot be written by IIC master.
En256W = 1 → The higher 128 bytes (80-FF) of DDCRAM2 can be written by IIC master.
= 0 → The higher 128 bytes (80-FF) of DDCRAM2 cannot be written by IIC master.
Only128 = 1 → The SlaveA2 always accesses EDID data from the lower 128 bytes of DDCRAM2.
= 0 → The SlaveA2 accesses EDID data from the whole 256 bytes DDCRAM2.
SlvA2bs1,SlvA2bs0 : Slave IIC block A2's slave address length.
= 1,0 → 5-bit slave address.
= 0,1 → 6-bit slave address.
= 0,0 → 7-bit slave address.

SLVA2ADR (w) : Slave IIC block A2's enable and address.
E nslvA2= 1 → Enables slave IIC block A2.
= 0 → Disables slave IIC block A2.
bit6-0 : Slave IIC address A2 to which the slave block should respond.

8. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of power supply is below 3.8V(+/-0.2V) / 2.5V(+/-0.15V) in 5V / 3.3V applications for a specific period of time, the LVR generates a chip reset signal. After the power supply is above 3.8V(+/-0.2V) / 2.5V(+/-0.15V) in 5V / 3.3V applications, LVR maintains in reset state for 144 X'tal cycle to guarantee the chip exit reset condition with a stable X'tal oscillation.
The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is 0.25 sec x N, where N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power on reset, users can activate this function by setting WEN, and clear the timer by setting WCLR.

9. A/D converter

The MTV312M is equipped with four VDD range 8-bit A/D converters. So if the VDD = 5V/3.3V, and then the ADC conversion range is 5V/3.3V, S/W can select the current convert channel by setting the SADC1/SADC0 bit. The refresh rate for the ADC is OSC freq./1536 (128us for 12MHz X'tal).

The ADC compares the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 255). The ADC output value is N when pin voltage is greater than VDD*N/255 and smaller than VDD*(N+1)/255.

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
ADC	F10h (w)	ENADC				SADC3 $	ADC2 $	ADC1	SADC0
ADC	F10h (r)	ADC convert result							
WDT	F18h (w)	WE N	WCLR				WDT2	WD T1	WDT0

WDT (w) : Watchdog Timer control register.

WE N = 1 → Enables Watchdog Timer.
W CLR = 1 → Clears Watchdog Timer.
WDT2: WDT0 = 0 → Overflow interval = 8 x 0.25 sec.
= 1 → Overflow interval = 1 x 0.25 sec.
= 2 → Overflow interval = 2 x 0.25 sec.
= 3 → Overflow interval = 3 x 0.25 sec.
= 4 → Overflow interval = 4 x 0.25 sec.
= 5 → Overflow interval = 5 x 0.25 sec.
= 6 → Overflow interval = 6 x 0.25 sec.
= 7 → Overflow interval = 7 x 0.25 sec.

ADC (w) : ADC control.

EN ADC = 1 → Enables ADC.
S ADC0 = 1 → Selects ADC0 pin input.
S ADC1 = 1 → Selects ADC1 pin input.
S ADC2 = 1 → Selects ADC2 pin input.
S ADC3 = 1 → Selects ADC3 pin input.

ADC (r) : ADC convert result.

11. In System Programming function (ISP)

The Flash memory can be programmed by a specific WRITER in parallel mode, or by IIC Host in serial mode while the system is working. The features of ISP are outlined as below:

1. Single 3.3V power supply for Program/Erase/Verify.
2. Block Erase: 1024 bytes for Program Code, 10mS
3. Whole Flash erase (Blank): 10mS
4. Byte/Word programming Cycle time: 60uS per byte
5. Read access time: 50ns
6. Only one two-pin IIC bus (shared with DDC2) is needed for ISP in user/factory mode.
7. IIC Bus clock rates up to 140KHz.
8. Whole 128K-byte Flash programming within 12 Sec.
9. CRC check provides 100% coverage for all single/double bit errors.

There are two methods to enter the ISP mode which are described as below:
Method 1). The Valid ISP Slave Address and Compared data are transmitted
Method 2). Write 93h to ISP enable register (ISPEN)

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							

ISPSLV (w) : ISP Slave IIC's address.
bit7-2 : ISP Slave IIC's address to which the ISP block should respond. The default value is 100101.
ISPEN(w) : Write 93h to enable ISP Mode for ISP enable method 2.

Memory Map of XFR

Reg name	addr	bit7	bit6 bi	t5	bit4 bi	t3 bi	t2 bi	t1	bit0
IICCTR	F00h (r/w)	DDC2					MAckO	P	S
IICSTUS	F01h (r)	WadrB		SlvRWB	SAckIn	SLVS			MAckIn
INTFLG	F03h (r)	TXBI	RCBI	SlvBMI	STOPI	ReStaI	WSlvAI		MbufI
INTFLG	F03h (w)			SlvBMI	STOPI	ReStaI	WSlvAI		MbufI
INTEN	F04h (w)	ETXBI	ERCBI	ESlvBMI	ESTOPI	EReStaI	EWSlvAI		EMbufI
MBUF	F05h (r/w)	Master IIC receives/transmits data buffer							
DDCCTR	F06h (w)	DDC1en	En128W	En256W	Only128			SlvAbs1	SlvAbs0
SLVAADR	F07h (w)	ENSlvA	Slave A IIC address						
RCBBUF	F08h (r)	Slave B IIC receives buffer							
TXBBUF	F08h (w)	Slave B IIC transmits buffer							
SLVBADR	F09h (w)	ENSlvB	Slave B IIC address						
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							
ISPCMP1	F0Dh(w)	ISP compared data 1 [7:0]							
ISPCMP2	F0Eh(w)	ISP compared data 2 [7:0]							
ISPCMP3	F0Fh(w)	ISP compared data 3 [7:0]							
ADC	F10h (w)	ENADC				SADC3 $	ADC2 $	ADC1	SADC0
ADC	F10h (r)			ADC convert Result					
WDT	F18h (w)	WE N	WCLR				WDT2	WD T1	WDT0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA4	F24h(r/w)	Pulse width of PWM DAC 4							
DA5	F25h(r/w)	Pulse width of PWM DAC 5							
DA6	F26h(r/w)	Pulse width of PWM DAC 6							
DA7	F27h(r/w)	Pulse width of PWM DAC 7							
DA8	F28h(r/w)	Pulse width of PWM DAC 8							
DA9	F29h(r/w)	Pulse width of PWM DAC 9							
DA10	F2Ah(r/w)	Pulse width of PWM DAC 10							
DA11	F2Bh(r/w)	Pulse width of PWM DAC 11							
DA12	F2Ch(r/w)	Pulse width of PWM DAC 12							
DA13	F2Dh(r/w)	Pulse width of PWM DAC 13							
PORT5	F30h(r/w)								P50
PORT5	F31h(r/w)								P51
PORT5	F32h(r/w)								P52
PORT5	F33h(r/w)								P53
PORT5	F34h(r/w)								P54
PORT5	F35h(r/w)								P55
PORT5	F36h(r/w)								P56
PORT6	F38h(r/w)								P60
PORT6	F39h(r/w)								P61
PORT6	F3Ah(r/w)								P62
PORT6	F3Bh(r/w)								P63
PORT6	F3Ch(r/w)								P64
PORT6	F3Dh(r/w)								P65
PORT6	F3Eh(r/w)								P66
PORT6	F3Fh(r/w)								P67
HVSTUS	F40h(r) C	Vpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12	HF11 H	F10	HF9	HF8

HCNTL	F42h(r)	HF7 H	F6 H	F5 H	F4 H	F3	HF2 H	F1 H	F0
VCNTH	F43h(r) Vov	f				VF11 VF	10	VF9	VF8
VCNTL	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h(w)	C1	C0	NoHins				HBpl	VBpl
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2	CL PW1	CL PW0		
HVCTR4	F44h(w)	VCpol						DF1	DF0
INTFLG	F48h(r/w) H	PRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg		Vsync
INTEN	F49h(w) EH	PR	EVPR	EHPL	EVPL	EHF	EVF		EVsync
PADMOD	F50h(w)	DA13E	DA12E	DA11E	DA10E	AD3E	AD2E	AD1E	AD0E
PADMOD	F51h(w)		P56E	P55E	P54E	P53E	P52E	P51E	P50E
PADMOD	F52h(w)	HIIC1E	IIICE	HIIC2E	CKOE	HCLPE	P42E	P41E	P40E
PADMOD	F53h(w)		P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD	F55h(w)	COP17	COP16	COP15	COP14	COP13	COP12	COP11	COP10
OPTION	F56h(w) PW	MF	DIV253	FclkE		ENSCL	Msel	MIICF1	MIICF0
PORT4	F58h(w)								P40
PORT4	F59h(w)								P41
PORT4	F5Ah(w)								P42
PADMOD	F5Eh(w)				P74E	P73E	P72E	P71 E	P70E
PADMOD	F5Fh(w)	P77oe	P76oe	P75oe	P74oe	P73oe	P72oe	P71oe	P70oe
PORT7	F70h(r/w)								P70
PORT7	F71h(r/w)								P71
PORT7	F72h(r/w)								P72
PORT7	F73h(r/w)								P73
PORT7	F74h(r/w)								P74
PORT7	F75h(r/w)								P75
PORT7	F76h(r/w)								P76
PORT7	F77h(r/w)								P77
EPADRH	FF1h(w)						EADR10	EADR9	EADR8
EPADRL	FF2h(w)	EADR7	EADR6	EADR5	EADR4	EADR3	EADR2	EADR1	EADR0
EPDATA	FF3h(r/w)	EDATA [7:0]							
INTFLG	FF4h(r/w)								EPbpf
INTEN	FF5h(w)								EEPbpf

ELECTRICAL PARAMETERS

1. Absolute Maximum Ratings

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name Sy	mbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +6.0	V
Maximum Input Voltage (HSYNC, VSYNC & open-drain pins)	Vin1	-0.3 to 5V+0.3	V
Maximum Input Voltage (other pins)	Vin2	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	^{o}C
Maximum Storage Temperature	Tstg	-25 to +125	^{o}C

2. Allowable Operating Conditions

at: Ta= 0 to 70 ^{o}C, VSS=0V

Name Sy	mbol	Condition	Min.	Max.	Unit
Supply Voltage	VDD	5V applications	4.5	5.5	V
		3.3V applications	3.0	3.6	V
Input "H" Voltage	Vih1	5V applications	0.4 x VDD	VDD +0.3	V
	Vih2	3.3V applications	0.6 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	5V applications	-0.3	0.2 x VDD	V
	Vil2	3.3V applications	-0.3	0.3 x VDD	V
Operating Freq.	Fopg		-	15	MHz

3. DC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=5.0V/3.3V, VSS=0V

Name S	ymbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage, open drain pin	Voh1	VDD=5V, Ioh=0uA	4			V
	Voh2	VDD=3.3V, Ioh=0uA	2.65			V
Output "H" Voltage, 8051 I/O port pin	Voh3	VDD=5V, Ioh=-50uA	4			V
	Voh4	VDD=3.3V, Ioh=-50uA	2.65			V
Output "H" Voltage, CMOS output	Voh5	VDD=5V, Ioh=-4mA	4			V
	Voh6	VDD=3.3V, Ioh=-4mA	2.65			V
Output "L" Voltage	Vol	Iol=5mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	150		250	Kohm
Pin Capacitance	Cio				15	pF

4. AC Characteristics

at: Ta=0 to 70 ^{o}C, VDD=5.0V/3.3V, VSS=0V

Name S	ymbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			12		MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		7.5	uS
VS input pulse Width	tVIPW	fXtal=12MHz	3			uS
HSYNC to Hblank output jitter	tHHBJ				5	nS
H+V to Vblank output delay	tVVBD	fXtal=12MHz		8		uS
VS pulse width in H+V signal	tVCPW	FXtal=12MHz	20			uS

Test Mode Condition

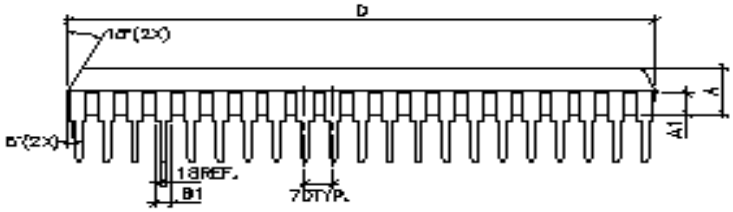
In normal application, users should avoid the MTV412M entering its test mode or writer mode, outlined as follows, adding pull-up resistor to DA8 and DA9 pins is recommended.

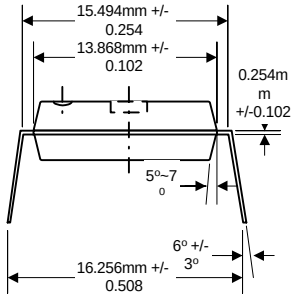
Test Mode A: RESET=1 & DA9=1 & DA8=0 & P4.2=0
Test Mode B: RESET's falling edge & DA9=1 & DA8=0 & P4.2=1
Writer Mode: RESET=1 & DA9=0 & DA8=1

PACKAGE DIMENSION

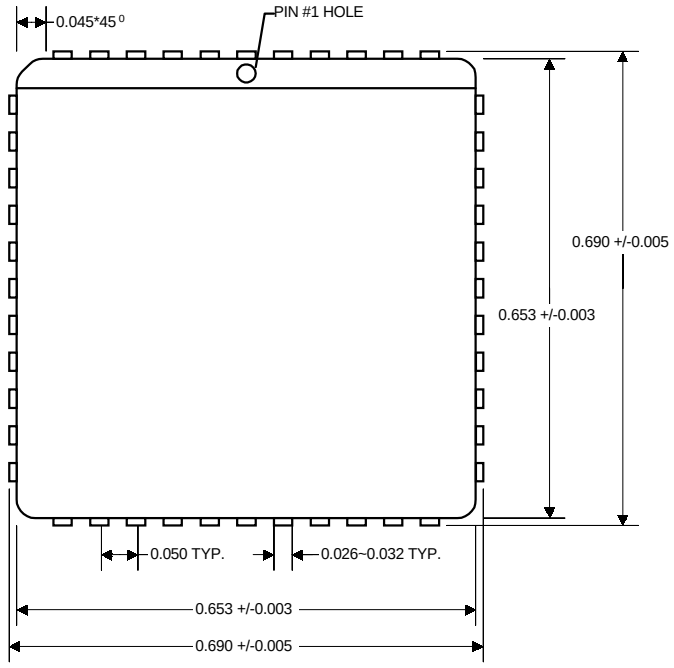
1. 42 pin SDIP Unit: mm

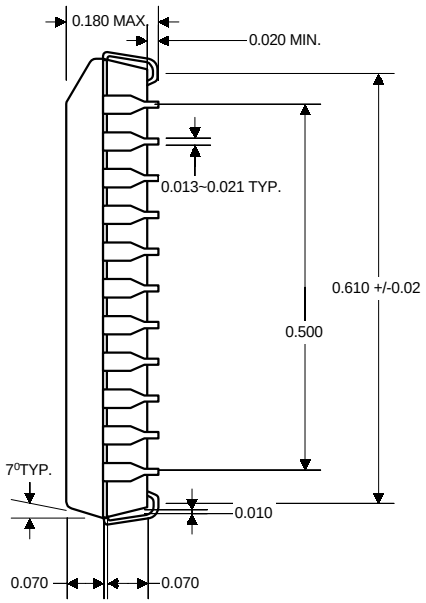
Symbol	Dimension in mm		
	Min	Nom	Max
A 3.	937	4.064	4.2
A1 1.	78	1.842	1.88
B1	0.914 1.	270 1.	118
D	36.78 36	.83 36	.88
E1 13	.945	13.970	13.995
F 15	.19	15.240	15.29
eB 15	.24	16.510	17.78
θ	0°	7.5°	15°





2. 44 pin PLCC Unit:





Ordering Information

Standard Configurations:

Prefix	Part Type	Package Type	ROM Size (K)
MTV	412M	S: SDIP V: PLCC F: PQFP	128