8051 Embedded Micro-Controller with 128K Flash ROM

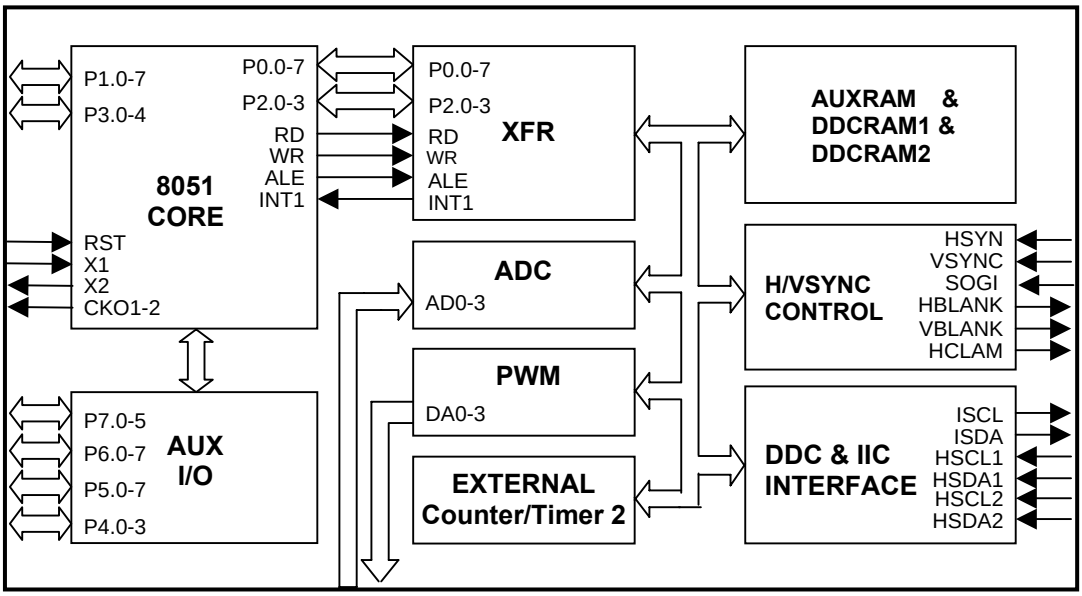
GENERAL DESCRIPTION

The MTV416M micro-controller is an 8051 CPU core embedded device targeted for LCD Monitor or LCD TV application. It includes an 8051 CPU core, a 128K-byte internal program Flash-ROM, a 768-byte SRAM, 4 channels of PWM DAC, 4 channels of 6-bit ADC, and a built-in sync-processor. It also includes two IIC Slave B ports, supporting VESA DDC/CI for both D-sub and DVI interfaces, and a Boot-Code-Free ISP (In System Programming).

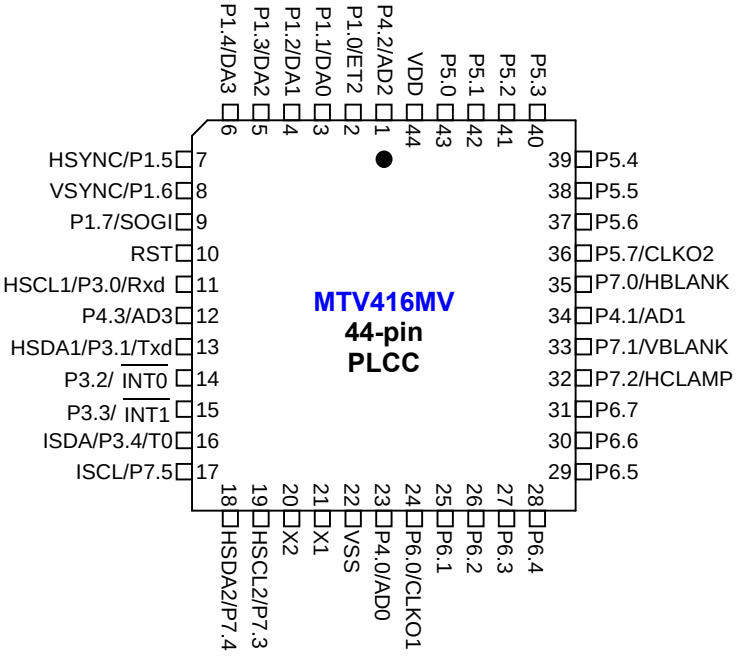
FEATURES

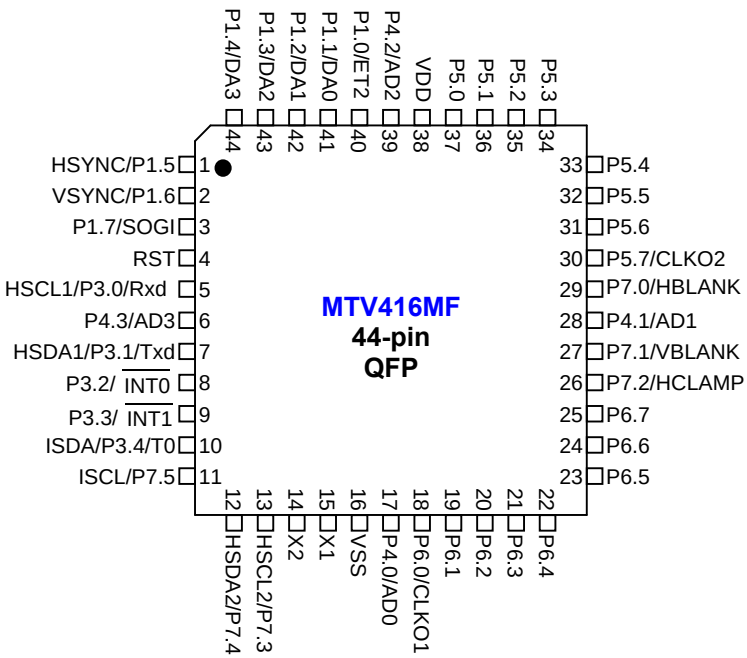
- 8051 core, 24MHz operating frequency
- + 3.3V power supply
- 768-bytes RAM; 128K-byte program Flash-ROM
  - 256 bytes Internal RAM
  - 256 bytes Auxiliary RAM
  - 128 x 2 bytes DDC RAM
- 4 channels of PWM DAC
  - Sink current up to 10 mA (DA0 ~ DA3)
  - Programmable PWM output frequency (100 Hz ~ 100KHz)
  - 14-bit PWM out for VCT application (DA2 and DA3)
- Maximum 39 I/O pins
- Maximum 10 channels of +3.3V/+5.0V tolerant I/O
  - Hsync, Vsync, HSCL1, HSDA1, HSCL2, HSDA2, and General I/O x 4
- SYNC processor for composite separation / insertion, H/V polarity/frequency check and polarity adjustment
  - Programmable hysteretic window for built-in Schmitt Trigger
- Built-in analog filter for Hsync, Vsync, and IIC input pins
- Support SOG (Sync On Green) input
- Two clock output ports to drive other devices
  - Programmable output driving current for EMI repression (CLKO1)
- Built-in dual DDC RAMs, H/W auto transfer DDC1/DDC2x data for both D-sub and DVI interfaces
- Built-in two IIC Slave B ports, supporting VESA DDC1/2B/2Bi/2B+/CI standards
- Single master IIC interface for peripheral device communication
- Maximum 4-channel 6-bit A/D converter with Flag indication
  - Conversion time: 16 uS
  - Input voltage level: 0 ~ +VDD
- ISP (In System Programming)
  - Support H/W ISP, no Boot Code required
- Programmable Watch Dog Timer
- Flash-ROM program code protection
- 44-pin PLCC or QFP package
- Green packages available
- Main application fields: LCD Monitor, LCD TV

BLOCK DIAGRAM



PIN CONNECTION DIAGRAMS





PIN DESCRIPTION

NAME	PIN NO.		PIN TYPE		DEFAULT FUNCTION	INTERNAL PULL UP/DOWN	PIN CONFIGURATION		FUNCTION DESCRIPTION
	PLCC	QFP	TYPE	DEFAULT			TYPE④	DEFAULT	
P4.2/AD2	1	39	I/O	I	P4.2	Up	C	C	General purpose I/O / Analog to Digital Converter 2 input
P1.0/ET2	2	40	I/O	I	P1.0	Up	5/C	5	General purpose I/O (8051 standard) / External Counter or Timer 2 Adding a pull-up resistor is recommended.
P1.1/DA0 ①	3	41	I/O	I	P1.1	-	O	O	General purpose I/O (8051standard) / PWM Digital to Analog Converter 0 output. It is a +3.3V/+5V tolerant I/O pin while configured as P1.1.
P1.2/DA1	4	42	I/O	I	P1.2	-	O	O	General purpose I/O (8051 standard) / PWM Digital to Analog Converter 1 output. It is a +3.3V/+5V tolerant I/O pin while configured as P1.2.
P1.3/DA2 ②	5	43	I/O	I	P1.3	-	O	O	General purpose I/O (8051 standard) / PWM Digital to Analog Converter 2 output. It is a +3.3V/+5V tolerant I/O pin while configured as P1.3.
P1.4/DA3	6	44	I/O	I	P1.4	-	O	O	General purpose I/O (8051 standard) / PWM Digital to Analog Converter 3 output. It is a +3.3V/+5V tolerant I/O pin while configured as P1.4.
HSYNC/P1.5	7	1	I/O	I	HSYNC	-	O	O	General purpose I/O (8051 standard) / Horizontal Sync or Composite Sync Input. It is a +3.3V/+5V tolerant I/O pin while configured as HSYNC.
VSYNC/P1.6	8	2	I/O	I	VSYNC	-	O	O	General purpose I/O(8051 standard) / Vertical Sync input. It is a 3.3V/5V tolerant I/O pin while configured as VSYNC.
P1.7/SOGI	9	3	I/O	I	P1.7	Up	5/C	5	General purpose I/O(8051 standard) / Sync On Green input
RST	10	4	I	I	RST	Down	I	I	Active high reset
HSCL1/P3.0/Rxd	11	5	I/O	I	HSCL1	-	O	O	Slave IIC 1 clock / General purpose I/O or Rxd (8051 standard). It is a +3.3V/+5V tolerant I/O pin while configured as HSCL1.
P4.3/AD3	12	6	I/O	I	P4.3	Up	C	C	General purpose I/O / Analog to Digital Converter 3 input
HSDA1/P3.1/Txd	13	7	I/O	I	HSDA1	-	O	O	Slave IIC 1 data / General purpose I/O or Txd (8051 standard). It is a +3.3V/+5V tolerant I/O pin while configured as HSDA1.
P3.2/INT0	14	8	I/O	I	P3.2	Up	5	5	General purpose I/O / INT0 (8051 standard)
P3.3/INT1	15	9	I/O	I	P3.3	Up	5	5	General purpose I/O / INT1 (8051 standard)
ISDA/P3.4/T0	16	10	I/O	I	ISDA	-	O	O	Master IIC data / General purpose I/O or T0 (8051 standard)
ISCL/P7.5	17	11	I/O	I	ISCL	-	O	O	Master IIC clock / General purpose I/O
HSDA2/P7.4	18	12	I/O	I	HSDA2	-	O	O	Slave IIC 2 data / General purpose I/O. It is a +3.3V/+5V tolerant I/O pin while configured as HSDA2.

NAME	PIN NO.		PIN TYPE		DEFAULT FUNCTION	INTERNAL PULL UP/DOWN	PIN CONFIGURATION		FUNCTION DESCRIPTION
	PLCC	QFP	TYPE	DEFAULT			TYPE④	DEFAULT	
HSCL2/P7.3	19	13	I/O	I	HSCL2	-	O	O	Slave IIC 2 clock / General purpose I/O. It is a +3.3V/+5V tolerant I/O pin while configured as HSCL2.
X2	20	14	O	O	X2	-	-	-	Oscillator output
X1	21	15	I	I	X1	-	-	-	Oscillator input
VSS	22	16	-	-	VSS	-	-	-	Ground
P4.0/AD0	23	17	I/O	I	P4.0	Up	C	C	General purpose I/O / Analog to Digital Converter 0 input
P6.0/CLKO1 ③	24	18	I/O	I	P6.0	Up	C	C	General purpose I/O / Oscillator Freq. clock output 1
P6.1	25	19	I/O	I	P6.1	Up	C	C	General purpose I/O
P6.2	26	20	I/O	I	P6.2	Up	C	C	General purpose I/O
P6.3	27	21	I/O	I	P6.3	Up	C	C	General purpose I/O
P6.4	28	22	I/O	I	P6.4	Up	C	C	General purpose I/O
P6.5	29	23	I/O	I	P6.5	Up	C	C	General purpose I/O
P6.6	30	24	I/O	I	P6.6	Up	C	C	General purpose I/O
P6.7	31	25	I/O	I	P6.7	Up	C	C	General purpose I/O
P7.2/HCLAMP	32	26	I/O	I	P7.2	Up	C	C	General purpose I/O / Hsync clamp pulse output
P7.1/VBLANK	33	27	I/O	I	P7.1	Up	C	C	General purpose I/O / Vertical blank output
P4.1/AD1	34	28	I/O	I	P4.1	Up	C	C	General purpose I/O / Analog to Digital Converter 1 input
P7.0/HBLANK	35	29	I/O	I	P7.0	Up	C	C	General purpose I/O / Horizontal blank output
P5.7/CLKO2	36	30	I/O	I	P5.7	Up	C	C	General purpose I/O / Oscillator Freq. clock output 2
P5.6	37	31	I/O	I	P5.6	Up	C	C	General purpose I/O
P5.5	38	32	I/O	I	P5.5	Up	C	C	General purpose I/O
P5.4	39	33	I/O	I	P5.4	Up	C	C	General purpose I/O
P5.3	40	34	I/O	I	P5.3	Up	C	C	General purpose I/O
P5.2	41	35	I/O	I	P5.2	Up	C	C	General purpose I/O
P5.1	42	36	I/O	I	P5.1	Up	C	C	General purpose I/O
P5.0	43	37	I/O	I	P5.0	Up	C	C	General purpose I/O
VDD	44	38	-	-	VDD	-	-	-	Positive power supply

Notes: ***① The sink current is up to 10 mA for DA0 ~ DA3 pins.***

② DA2 and DA3 ports support 14-bit PWM output.

③ Output driving current is programmable on CLKO1 port.

④ Pin configuration description

C - CMOS
O - Open Drain
I - Input
5 - Standard 8051

PIN CONFIGURATION

A “CMOS output pin” (Figure 1-2) means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

An “open drain pin” (Figure 1-3) means it can sink at least 4mA current. It can be used as input or output function and needs an external pull up resistor.

An “8051 standard pin” (Figure 1-1) is a pseudo open drain pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 160nS when output transits from low to high, then keeps driving at 100uA to maintain the pin at high level. It can be used as input or output function. It needs an external pull up resistor when driving heavy load device.

There is an internal-pull down resistance on each CMOS PAD and an internal pull-down resistance on each input PAD. It is recommended to add a pull high resistance on each open drain pin.

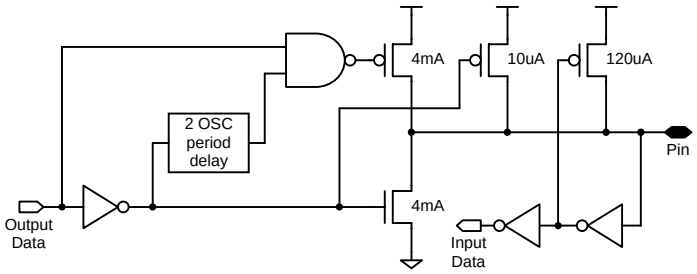


Figure 1-1 8051 Standard Pin

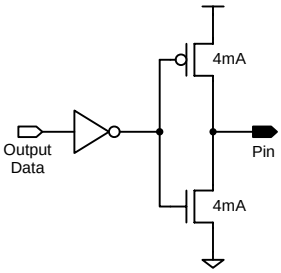


Figure 1-2 CMOS Output Pin

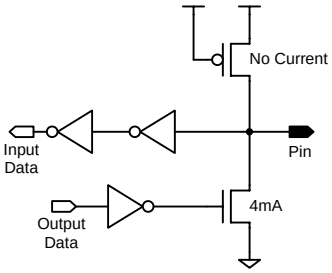


Figure 1-3 Open Drain Pin

FUNCTIONAL DESCRIPTIONS

8051 CPU CORE

The CPU core of MTV416M is compatible with the in standard 8051, which includes 256 bytes RAM, Special Function Registers (SFR), two timers (T0 and ET2), five interrupt sources and a serial interface (UART). The CPU core fetches its program code from the 128K bytes Flash memory in MTV416M. It uses Port0 and Port2 to access the “external special function register” (XFR) and external auxiliary RAM (AUXRAM).

Note: All registers listed in this document reside in 8051’s external RAM area (XFR). For internal RAM memory map, please refer to 8051 specifications.

Memory Allocation

Internal Special Function Registers (SFR)

The SFR is a group of registers that are the same as standard 8051.

Internal RAM

There are total 256 bytes internal RAM in MTV416M, the same as standard 8052.

External Special Function Registers (XFR)

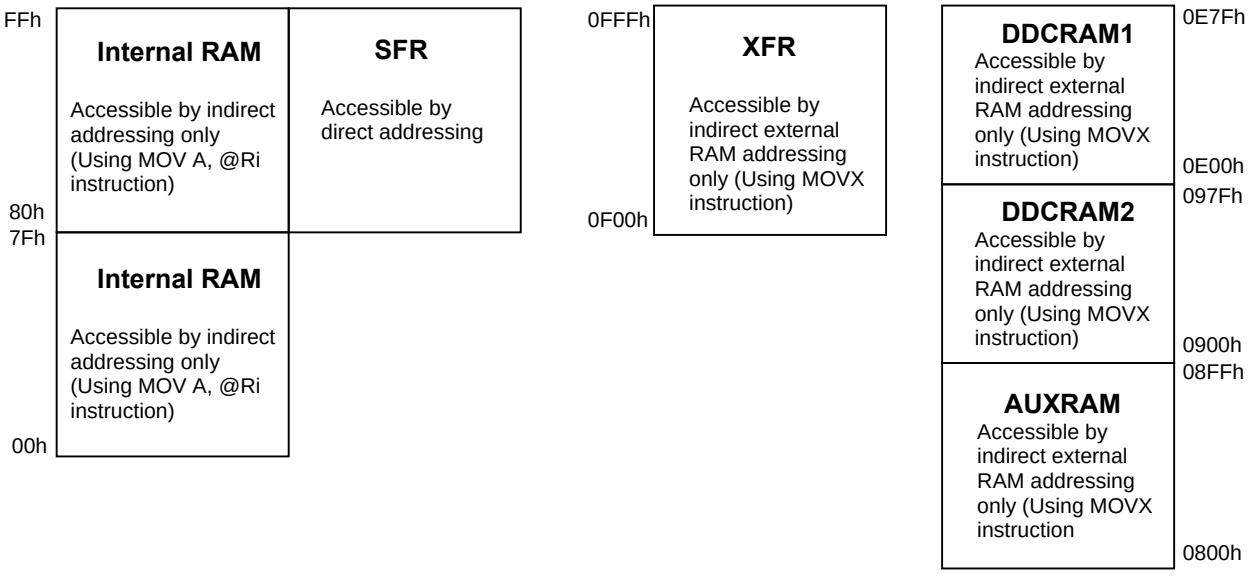
The XFR is a group of registers allocated in the 8051 external RAM areas F00h – FFFh. These registers are used for special functions. Programs can use "MOVX" instruction to access these registers.

Auxiliary RAM (AUXRAM)

There are total 256 bytes auxiliary RAM allocated in the 8051 external RAM area 800h - 8FFh. Programs can use "MOVX" instruction to access the AUXRAM.

Dual Port RAM (DDCRAM)

There are two 128 bytes Dual Port RAM allocated in the 8051 external RAM area 0900h-097Fh and 0E00h - 0E7Fh. Programs can use "MOVX" instruction to access the RAM. The external IIC Host can access the RAM by IIC protocol. The addresses from 0800h to 0FFFh are occupied by MTV416M XFR and on-chip memory (DDCRAMs and AUXRAM). External Access should use 0000h to 07FF and 1000h to FFFFh.



Chip Configuration

The Chip Configuration registers define configuration of the chip and function of the pins. Except HIIC1E, PADMOD5D, and PADMODE5E, all registers are "0" after chip reset.

REG NAME	ADDRESS	bit7	bit6	bit5	Bit4	bit3	bit2	bit1	bit0
PADMOD50	F50h(w)					AD3E	AD2E	AD1E	AD0E
PADMOD51	F51h(w)								ICE_T
PADMOD52	F52h(w)	HIIC1E	IIICE	HIIC2E	CKOE1	HCLPE	CKOE2		
PADMOD53	F53h(w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD54	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD55	F55h(w)	COP17							COP10
OPTION56	F56h(w)	PWMF	DIV253	Rev5	Rev4	ENSCL	Msel	MIICF1	MIICF0
PADMOD57	F57h(w)					P43oe	P42oe	P41oe	P40oe
PADMOD5D	F5Dh(w)	P17E	P16E	P15E	P14E	P13E	P12E	P11E	P10E
PADMOD5E	F5Eh(w)			P75E	P74E	P73E	P72E	P71E	P70E
PADMOD5F	F5Fh(w)			P75oe	P74oe	P73oe	P72oe	P71oe	P70oe

PADMOD50 (w): Pad mode control registers.

AD3E = 1 → Pin "P4.3/AD0" is AD3.
= 0 → Pin "P4.3/AD0" is P4.3.
AD2E = 1 → Pin "P4.2/AD0" is AD2.
= 0 → Pin "P4.2/AD0" is P4.2.
AD1E = 1 → Pin "P4.1/AD0" is AD0.
= 0 → Pin "P4.1/AD0" is P4.1.
AD0E = 1 → Pin "P4.0/AD0" is AD0.
= 0 → Pin "P4.0/AD0" is P4.0.

PADMOD51 (w):

ICE_T = 1 → ICE mode setting
= 0 → Normal operation

PADMOD52 (w):

HIIC1E = 1 → Pin "HSCL1/P3.0/Rxd" is HSCL1; pin "HSDA1/P3.1/Txd" is HSDA1.
= 0 → Pin "HSCL1/P3.0/Rxd" is P3.0/Rxd; pin "HSDA1/P3.1/Txd" is P3.1/Txd.
IIICE = 1 → Pin "ISDA/P3.4/T0" is ISDA; pin "ISCL/P7.5" is ISCL.
= 0 → Pin "ISDA/P3.4/T0" is P3.4/T0; pin "ISCL/P7.5" is P7.5.
HIIC2E = 1 → Pin "HSCL2/P7.3" is HSCL2; pin "HSDA2/P7.4" is HSDA2.
= 0 → Pin "HSCL2/P7.3" is P7.3; pin "HSDA2/P7.4" is P7.4.
CKOE1 = 1 → Pin "P6.0/CLKO1 is P6.0
= 0 → Pin "P6.0/CLKO1 is CLKO1
HCLPE = 1 → Pin "P7.2/HCLAMP" is HCLAMP
= 0 → Pin "P7.2/HCLAMP" is P7.2
CKOE2 = 1 → Pin "P5.7/CLKO2 is P5.7
= 0 → Pin "P5.7/CLKO2" is CLKO2

PADMOD53 (w) : Port 5 output enable

P57oe = 1 → P5.7 is output pin.
= 0 → P5.7 is input pin.
P56oe = 1 → P5.6 is output pin.
= 0 → P5.6 is input pin.
P55oe = 1 → P5.5 is output pin.
= 0 → P5.5 is input pin.
P54oe = 1 → P5.4 is output pin.
= 0 → P5.4 is input pin.
P53oe = 1 → P5.3 is output pin.
= 0 → P5.3 is input pin.
P52oe = 1 → P5.2 is output pin.
= 0 → P5.2 is input pin.
P51oe = 1 → P5.1 is output pin.
= 0 → P5.1 is input pin.
P50oe = 1 → P5.0 is output pin.
= 0 → P5.0 is input pin.

PADMOD54 (w) : Port 6 output enable

P67oe = 1 → P6.7 is output pin.
= 0 → P6.7 is input pin.
P66oe = 1 → P6.6 is output pin.
= 0 → P6.6 is input pin.
P65oe = 1 → P6.5 is output pin.
= 0 → P6.5 is input pin.
P64oe = 1 → P6.4 is output pin.
= 0 → P6.4 is input pin.
P63oe = 1 → P6.3 is output pin.
= 0 → P6.3 is input pin.
P62oe = 1 → P6.2 is output pin.
= 0 → P6.2 is input pin.
P61oe = 1 → P6.1 is output pin.
= 0 → P6.1 is input pin.
P60oe = 1 → P6.0 is output pin.
= 0 → P6.0 is input pin.

PADMOD55 (w): Pin configuration type setting

COP17 = 1 → Pin “P1.7” is CMOS Output.
= 0 → Pin “P1.7” is 8051 standard I/O.
COP10 = 1 → Pin “P1.0” is CMOS Output.
= 0 → Pin “P1.0” is 8051 standard I/O.

OPTION56 (w) : Chip option configuration (All are "0" after Chip Reset).

PWMF = 1 → Selects 94KHz PWM frequency.
= 0 → Selects 47KHz PWM frequency.
DIV253 = 1 → PWM pulse width is 253-step resolution.
= 0 → PWM pulse width is 256-step resolution.
Rev5 = 1 → Reserve for testing
= 0 → Normal Application
Rev4 = 1 → Reserve for testing
= 0 → Normal Application
ENSCL = 1 → Enable slave IIC block to hold HSCL pin low while MTV416M is unable to catch up with the external master's speed.
Msel = 1 → Master IIC block connect to HSCL1/HSDA1 pins.
= 0 → Master IIC block connect to ISCL/ISDA pins.
MIICF1, MIICF0= 1,1 → Master IIC bus operates at 400KHZ
= 1,0 → Master IIC bus operates at 200KHZ
= 0,1 → Master IIC bus operates at 50KHZ
= 0,0 → Master IIC bus operates at 100KHZ

PADMOD57 (w) : Port 4 output enable

P43oe = 1 → P4.3 is output pin.
= 0 → P4.3 is input pin.
P42oe = 1 → P4.2 is output pin.
= 0 → P4.2 is input pin.
P41oe = 1 → P4.1 is output pin.
= 0 → P4.1 is input pin.
P40oe = 1 → P4.0 is output pin.
= 0 → P4.0 is input pin.

PADMOD5D (w): Port 1 pin definition setting

P17E = 1 → Pin “P1.7/SOGI” is P1.7.
= 0 → Pin “P1.7/SOGI” is SOGI.
P16E = 1 → Pin “P1.6/VSYNC” is P1.6.
= 0 → Pin “P1.6/VSYNC” is VSYNC.
P15E = 1 → Pin “P1.5/HSYNC” is P1.5.
= 0 → Pin “P1.5/HSYNC” is HSYNC.
P14E = 1 → Pin “P1.4/DA3” is P1.4.
= 0 → Pin “P1.4/DA3” is DA3.
P13E = 1 → Pin “P1.3/DA2” is P1.3.
= 0 → Pin “P1.3/DA2” is DA2.
P12E = 1 → Pin “P1.2/DA1” is P1.2.
= 0 → Pin “P1.2/DA1” is DA1.
P11E = 1 → Pin “P1.1/DA0” is P1.1.
= 0 → Pin “P1.1/DA0” is DA0.

P10E = 1 → Pin "P1.0/ ET2" is P1.0.
= 0 → Pin "P1.0/ET2" is ET2.

PADMOD5E (w): Port 7 pin definition setting

P75E = 1 → Pin "ISCL/P7.5" is P7.5.
= 0 → Pin "ISCL/P7.5" is ISCL.
P74E = 1 → Pin "HSDA2/P7.4" is P7.4.
= 0 → Pin "HSDA2/P7.4" is HSDA2.
P73E = 1 → Pin "HSCL2/P7.3" is P7.3.
= 0 → Pin "HSCL2/P7.3" is HSCL2.
P72E = 1 → Pin "P7.2/HCLAMP" is P7.2.
= 0 → Pin "P7.2/HCLAMP" is HCLAMP.
P71E = 1 → Pin "P7.1/ VBLANK" is P7.1.
= 0 → Pin "P7.1/VBLANK" is VBLANK.
P70E = 1 → Pin "P7.0/ HBLANK" is P7.0.
= 0 → Pin "P7.0/HBLANK" is HBLANK.

PADMOD5F (w) : Port 7 output enable

P75oe = 1 → P7.5 is output pin.
= 0 → P7.5 is input pin.
P74oe = 1 → P7.4 is output pin.
= 0 → P7.4 is input pin.
P73oe = 1 → P7.3 is output pin.
= 0 → P7.3 is input pin.
P72oe = 1 → P7.2 is output pin.
= 0 → P7.2 is input pin.
P71oe = 1 → P7.1 is output pin.
= 0 → P7.1 is input pin.
P70oe = 1 → P7.0 is output pin.
= 0 → P7.0 is input pin.

I/O Ports

Port 1

Port1 is a group of pseudo open-drain pins or CMOS output pins. It can be used as general purpose I/O. Behavior of Port1 is the same as standard 8051.

P3.0-3.4

If these pins are not set as IIC pins, Port3 can be used as general purpose I/O, interrupt, UART and Timer pins. Behavior of Port3 is the same as standard 8051.

Port 4, Port 5, Port 6 and Port 7

When Port 4, Port 5, Port 6 and Port 7 are used as general purpose I/O, S/W needs to set the corresponding P4(n)oe, P5(n)oe, P6(n)oe, and P7(n)oe to define whether these pins are input or output. These ports can be accessed in bit or byte mode.

REG NAME	ADDRESS	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
P5B0	F30h(w)								P50
P5B1	F31h(w)							P51	
P5B2	F32h(w)						P52		
P5B3	F33h(w)					P53			
P5B4	F34h(w)				P54				
P5B5	F35h(w)			P55					
P5B6	F36h(w)		P56						
P5B7	F37h(w)	**P57**							
P6B0	F38h(w)								P60
P6B1	F39h(w)							P61	
P6B2	F3Ah(w)						P62		
P6B3	F3Bh(w)					P63			
P6B4	F3Ch(w)				P64				
P6B5	F3Dh(w)			P65					
P6B6	F3Eh(w)		P66						
P6B7	F3Fh(w)	**P67**							
P4B0	F58h(w)								P40
P4B1	F59h(w)							P41	
P4B2	F5Ah(w)						P42		
P4B3	F5Bh(w)					P43			
P7B0	F70h(w)								P70
P7B1	F71h(w)							P71	
P7B2	F72h(w)						P72		
P7B3	F73h(w)					P73			
P7B4	F74h(w)				P74				
P7B5	F75h(w)			P75					
PORT 5	F80h(r/w)	P57	P56	P55	P54	P53	P52	P51	P50
PORT 6	F81h(r/w)	P67	P66	P65	P64	P63	P62	P61	P60
PORT 4	F82h(r/w)					P43	P42	P41	P40
PORT 7	F83h(r/w)			P75	P74	P73	P72	P71	P70

Note: MTV416M supports bit/byte write and byte read functions on Port4, Port5, Port6, and Port7.

P4B0 – P4B3 (w) : Port 4 bit access data output.
P5B0 – P5B7 (w) : Port 5 bit access data output
P6B0 – P6B7 (w) : Port 6 bit access data output.
P7B0 – P7B7 (w) : Port 7 bit access data output.

PORT 4 (r/w) : Port 4 4-bit input/output data.

PORT 5 (r/w) : Port 5 data input/output value.

PORT 6 (r/w) : Port 6 data input/output value.

PORT 7 (r/w) : Port 7 6-bit input/output value.

PWM DAC

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	F20h(r/w)	Pulse width of PWM DAC 0 *							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA2FC	F2Dh(r/w)			D2B5	D2B4	D2B3	D2B2	D2B1	D2B0
DA3FC	F2Eh(r/w)			D3B5	D3B4	D3B3	D3B2	D3B1	D3B0

Note : All of PWM DACs are centered with value 80h after power on.

DA0 – DA3 (r/w) : The output pulse width control for DA0-3.

DA2FC (r/w) : The control signals to fine-tune the pulse width of PWM channel 2 output.
DA3FC (r/w) : The control signals to fine-tune the pulse width of PWM channel 3 output.

Each output pulse width of PWM DACs is controlled by an 8-bit register in XFR. The frequency of PWM is 47KHz or 94KHz, selected by PWMF(See **OPTION56**). And the total duty cycle step of these DAC outputs is 253 or 256, selected by DIV253(See **OPTION56**). If DIV253=1, writing FDH/FEH/FFH to DAC register generates a stable high output, while writing 00H generates a stable low output. If DIV253=0, the output pulses low at least once even if the DAC register's content is FFH.

For channel 2 and 3, there are other 6-bit registers used to fine-tune the duty. To control the 6-bit registers, user can generate an additional pulse(1/256 * cycle time) in the certain cycles. If the 6-bit data is m in decimal, the additional pulse is generated in each m period of 64 periods. The relationship between the 6-bit and the modified wider pulse cycle is shown below. (Table 1 & Figure 2)

Bit position of the 6-bit data	Relative cycles where to fine-tune the pulse
Bit0 (D2B0 or D3B0)	32
Bit1 (D2B1 or D3B1)	16,48
Bit2 (D2B2 or D3B2)	8,24,40,56
Bit3 (D2B3 or D3B3)	4,12,20,28,36,44,52,60
Bit4 (D2B4 or D3B4)	2,6,10,14,18,22,26,30,…,58,62
Bit5 (D2B5 or D3B5)	1,3,5,7,9,11,13,15,17,…,59,61,63

Table 1

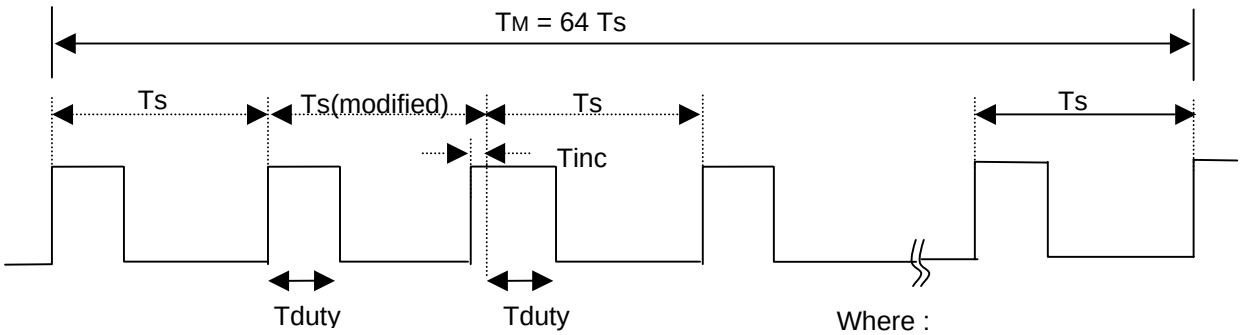


Figure 2

H/V SYNC Processing

The H/V SYNC processing block (Figure 3) performs the functions of composite signal separation/insertion. SYNC inputs presence check, frequency counting, polarity detection and control, as well as the protection of VBLANK output while VSYNC speeds up in high DDC communication clock rate. Based on the digital filter, the HSYNC present and frequency function block treat any pulse longer than the specified time period as pulse, and the specified time period is controlled by (DF1,DF0) bits. The VSYNC digital filter has no control bit. It works as (DF1, DF0) = (0, 0) of HSYNC.

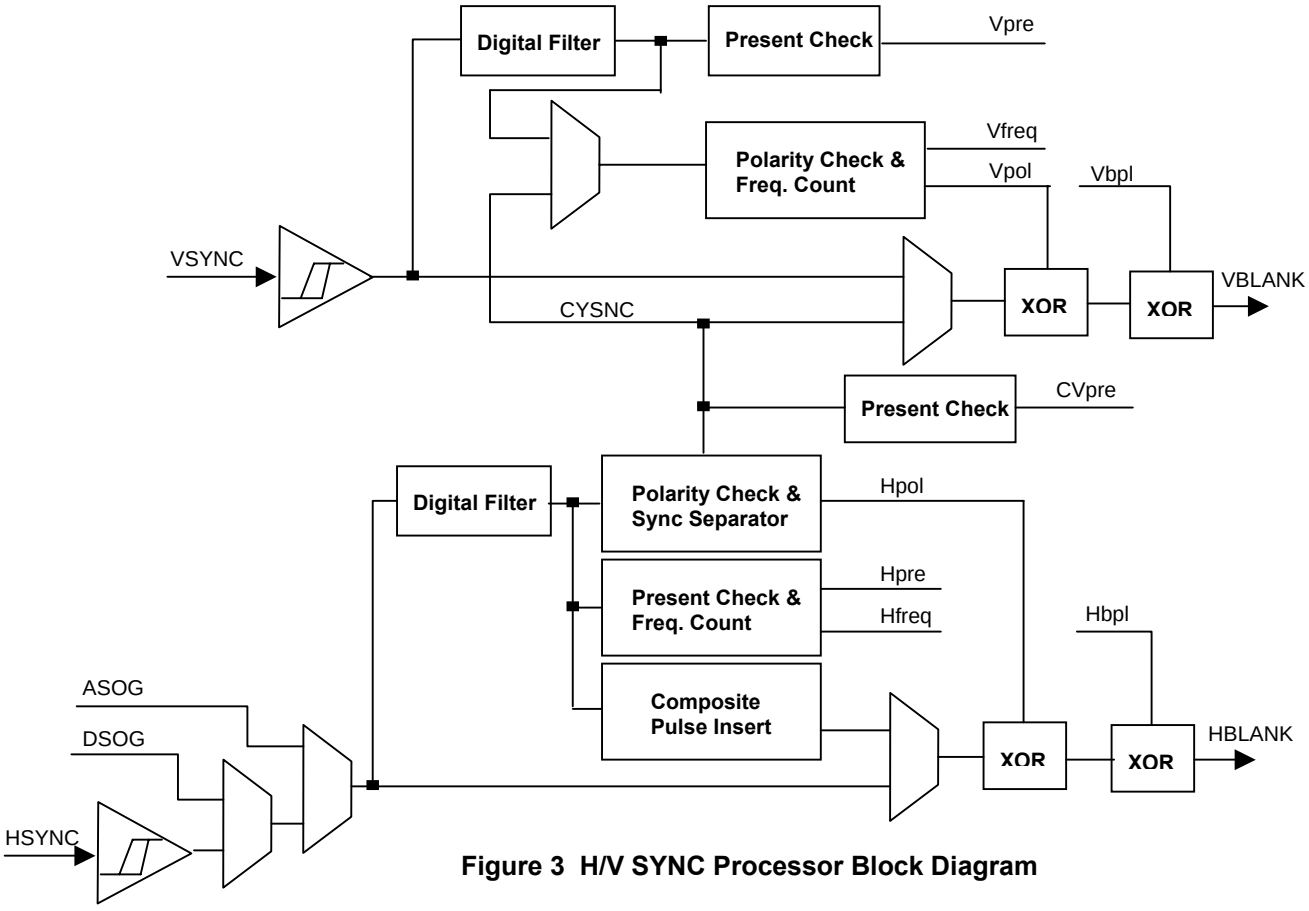


Figure 3 H/V SYNC Processor Block Diagram

Composite SYNC separation/insertion

The MTV416M continuously monitors the input HSYNC. If the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and users can select the extracted "CVSYNC" for the source of polarity check, frequency count, and VBLANK output. The CVSYNC then has 8us delay compared to the original signal. The MTV416M can also insert pulse to HBLANK output during composite VSYNC's active time. The width of insert pulse is 1/8 HSYNC period and the insertion frequency can adapt to original HSYNC. The insert pulse of HBLANK can be disabled or enabled by setting "NoHins" control bit. If "NoHins" bit is set to "1", HBLANK output will be same as HSYNC input (of course, polarity can be controlled by HBpl bit).

H/V Frequency Counter

MTV416M can discriminate HSYNC/VSYNC frequency and save the information in XFRs. The 14-bit Hcounter counts the time of 64xHSYNC period, then loads the result into the HCNTH/HCNTL latch. The output value is then [(128000000/H-Freq) - 1], updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present or continuously updated when VSYNC/CVSYNC is non-present. The 12-bit Vcounter counts the time between two VSYNC pulses, and then loads the result into the VCNTH/VCNTL latch. The output value is then (62500/V-Freq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is set when VCNT/HCNT value changes or overflows. Table 6.2.1 and Table 6.2.2 show the HCNT/VCNT value under the operations of 12MHz.

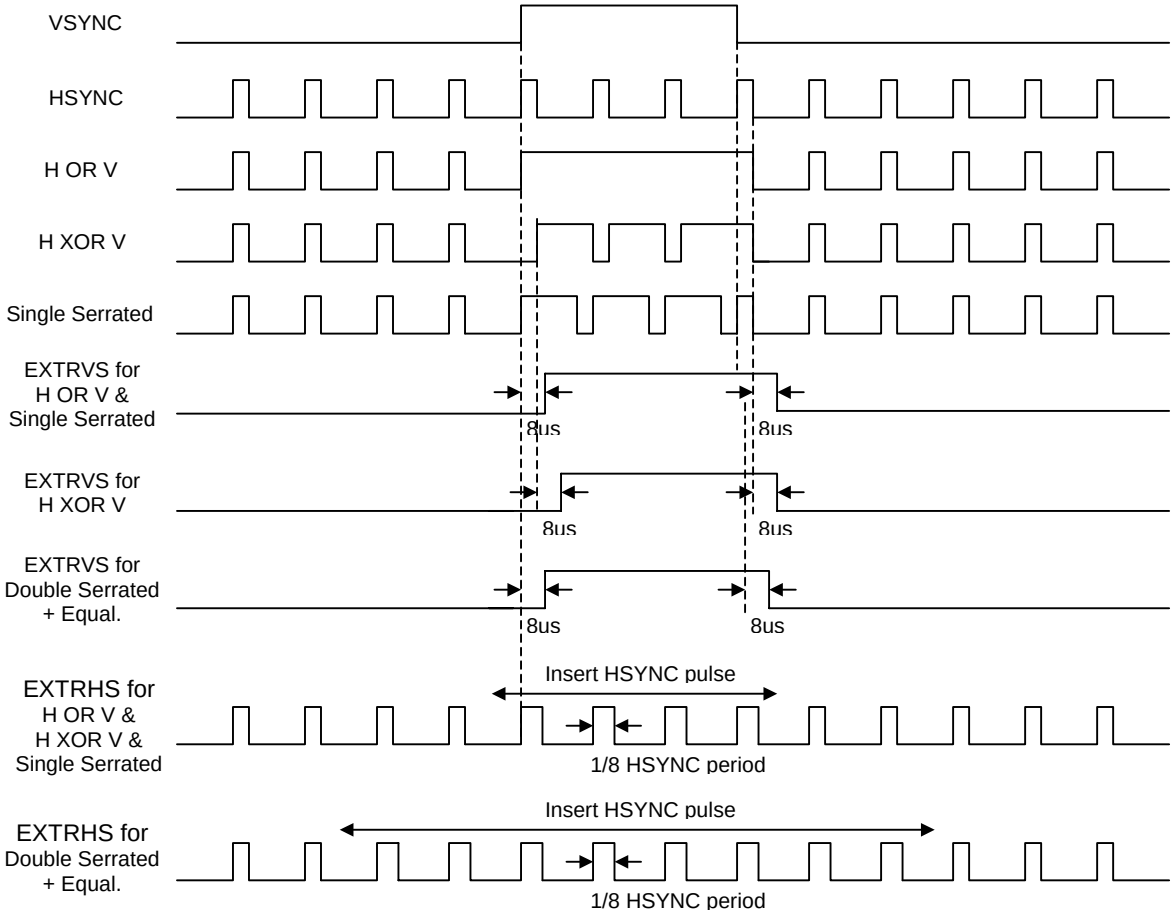


Figure 4 Timing Relationship of Composite SYNC Signal Separation/Insertion when "NoHins" = 0

H-Freq(KHZ)		OUTPUT VALUE (14 bits) 12MHz OSC (hex / dec)
1	31.5	0FDEh / 4062
2	37.5	0D54h / 3412
3	43.3	0B8Bh / 2955
4	46.9	0AA8h / 2728
5	53.7	094Fh / 2383
6	60.0	0854h / 2132
7	68.7	0746h / 1862
8	75.0	06AAh / 1706
9	80.0	063Fh / 1599
10	85.9	05D1h / 1489
11	93.8	0554h / 1364
12	106.3	04B3h / 1203

Table 2-1 H Frequency Counter Table

V-Freq(Hz)		OUTPUT VALUE (12bits) 12MHz OSC (hex / dec)
1	56	45Ch / 1116
2	60	411h / 1041
3	70	37Ch / 892
4	72	364h / 868
5	75	341h / 833
6	85	2DFh / 735

Table 2-2 V Frequency Counter Table

H/V Present Check

The Hpresent function checks the input HSYNC pulse, and the Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The Vpresent function checks the input VSYNC pulse, and the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre value change.

H/V Polarity Detect

The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

Output HBLANK/VBLANK Control and Polarity Adjust

The HBLANK is the mux output of HSYNC and composite Hpulse. The VBLANK is the mux output of VSYNC and CVSYNC. The mux selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 250Hz. The HBLANK/VBLANK shares the output pin with P7.1/ P7.0.

HSYNC Clamp Pulse Output

The HCLAMP output is activated by setting “HCLPE” control bit. The leading edge position, pulse width and polarity of HCLAMP are S/W controllable.

VSYNC Interrupt

The MTV416M checks the VSYNC input pulse and generates an interrupt at its leading edge. The VSYNC flag is set each time when MTV416M detects a VSYNC pulse. The flag is cleared by S/W writing a "0".

SOG (Sync On Green)

The MTV416M supports SOG separation. User should input the SOG signal in an AC coupled method. The separated Hsync will be sent to Sync processor as an Hsync input if ENSOG is set to high. If ENSOG is 0 and ENDSOG is 1, the digital pulse from P1.5 is directly sent to Sync processor without the separation process.

H/V SYNC Processor Register

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	F43h(r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h(w)	C1	C0	NoHins	ENSOG	ENSOGD		HBpl	VBpl
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
HVCTR4	F44h(w)							DF1	DF0
HVFILT	F46h(w)	VPF1	VPF0	VNMW	VAW	HPF1	HPF0	HNMW	HAW
INTFLG	F48h(r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	Hsync	Vsync
INTEN	F49h(w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EHsync	EVsync
SOGCTL	F4Ah(w)	SPF1	SPF0	SSEL[4:0]					

HVSTUS (r) : The status of polarity, present and static level for HSYNC and VSYNC.

- CVpre = 1 → The extracted CVSYNC is present.
  = 0 → The extracted CVSYNC is not present.
- Hpol = 1 → HSYNC input is positive polarity.
  = 0 → HSYNC input is negative polarity.
- Vpol = 1 → VSYNC (CVSYNC) is positive polarity.
  = 0 → VSYNC (CVSYNC) is negative polarity.
- Hpre = 1 → HSYNC input is present.
  = 0 → HSYNC input is not present.
- Vpre = 1 → VSYNC input is present.
  = 0 → VSYNC input is not present.
- Hoff* = 1 → Off level of HSYNC input is high.
  = 0 → Off level of HSYNC input is low.
- Voff* = 1 → Off level of VSYNC input is high.
  = 0 → Off level of VSYNC input is low.

*** H_{off} and V_{off} are valid when $H_{pre=0}$ or $V_{pre=0}$.**

HCNTH (r) : H-Freq counter's high bits.

- Hovf = 1 → H-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
- HF13 - HF8 : → 6 high bits of H-Freq counter.

HCNTL (r) : H-Freq counter's low byte.

VCNTH (r) : V-Freq counter's high bits.

- Vovf = 1 → V-Freq counter is overflowed, this bit is cleared by H/W when condition removed.
- VF11 - 8 : → 4 high bits of V-Freq counter.

VCNTL (r) : V-Freq counter's low byte.

HVCTR0 (w) : H/V SYNC processor control register 0.

C1, C0 = 1,1 → Selects CVSYNC as the polarity, freq and VBLANK source.
= 1,0 → Selects VSYNC as the polarity, freq and VBLANK source.
= 0,0 → Disables composite function.
= 0,1 → H/W automatically switches to CVSYNC when CVpre=1 and VSpre=0.
NoHins = 1 → HBLANK has no insert pulse in composite mode.
= 0 → HBLANK has insert pulse in composite mode.
ENSOG= 1 → enable analog SOG input function.
= 0 → disable analog SOG input function.
ENSOGD= 1 → enable digital SOG input function.
= 0 → disable digital SOG input function.
HBpl = 1 → Negative polarity HBLANK output.
= 0 → Positive polarity HBLANK output.
VBpl = 1 → Negative polarity VBLANK output.
= 0 → Positive polarity VBLANK output.

HVCTR3 (w) : HSYNC clamp pulse control register.

CLPEG = 1 → Clamp pulse follows HSYNC leading edge.
= 0 → Clamp pulse follows HSYNC trailing edge.
CLPPO = 1 → Positive polarity clamp pulse output.
= 0 → Negative polarity clamp pulse output.
CLPW2 : CLPW0 : Pulse width of clamp pulse is
[(CLPW2:CLPW0) + 1] x 0.167 μs for 12MHz X'tal selection.

HVCTR4 (w) :

DF1, DF0 :
= 0,0 → The digital filter will treat any HSYNC pulse shorter than one OSC period (83.33ns) as noise, between one and two OSC period (83.33ns to 166.67ns) as unknown region, and longer than two OSC period (166.67ns) as pulse.
= 0,1 → The digital filter will treat any HSYNC pulse shorter than half OSC period (41.66ns) as noise, between half and one OSC period (41.66ns to 83.33ns) as unknown region, and longer than one OSC period (83.33ns) as pulse.
= 1,x → Disable the digital filter for HSYNC.

HVFILT (w) :

VPF1, VPF0 : Pulse filter length control
= 0,0 → By pass pulse filter
= 0,1 → 50ns
= 1,0 → 100ns
= 1,1 → 150ns

VNMW, VAW: Adjust the Schmitt trigger's voltage level
= 0,0 → 1.1/1.8
= 0.1 → 0.7/2.0
= 1.0 → 1.3/1.6
= 1.1 → 1.3/1.6

HPF1, HPF0 : Pulse filter length control
= 0,0 → By pass pulse filter
= 0,1 → 50ns
= 1,0 → 100ns
= 1,1 → 150ns

HNMW, HAW: Adjust the Schmitt trigger's voltage level
= 0,0 → 1.1/1.8
= 0.1 → 0.7/2.0

= 1.0 → 1.3/1.6
= 1.1 → 1.3/1.6

INTFLG (w) : Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the INT1 source of 8051 core will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

HPRchg= 1 → No action
= 0 → Clears HSYNC presence change flag
VPRchg= 1 → No action
= 0 → Clears VSYNC presence change flag
HPLchg= 1 → No action
= 0 → Clears HSYNC polarity change flag
VPLchg= 1 → No action
= 0 → Clears VSYNC polarity change flag
HFchg = 1 → No action
= 0 → Clears HSYNC frequency change flag
VFchg = 1 → No action
= 0 → Clears VSYNC frequency change flag
Hsync = 1 → No action
= 0 → Clears HSYNC interrupt flag
Vsync = 1 → No action
= 0 → Clears VSYNC interrupt flag

INTFLG (r) : Interrupt flag

HPRchg= 1 → Indicates a HSYNC presence change
VPRchg= 1 → Indicates a VSYNC presence change
HPLchg= 1 → Indicates a HSYNC polarity change
VPLchg= 1 → Indicates a VSYNC polarity change
HFchg = 1 → Indicates a HSYNC frequency change or counter overflow
VFchg = 1 → Indicates a VSYNC frequency change or counter overflow
Hsync = 1 → Indicates a HSYNC interrupt
Vsync = 1 → Indicates a VSYNC interrupt

INTEN (w) : Interrupt enable.

EHPR = 1 → Enables HSYNC presence change interrupt
EVPR = 1 → Enables VSYNC presence change interrupt
EHPL = 1 → Enables HSYNC polarity change interrupt
EVPL = 1 → Enables VSYNC polarity change interrupt
EHF = 1 → Enables HSYNC frequency change / counter overflow interrupt
EVF = 1 → Enables VSYNC frequency change / counter overflow interrupt
EHsync = 1 → Enables HSYNC interrupt
EVsync = 1 → Enables VSYNC interrupt

SOGCTL (w) : Sync-on-green control

SPF0, SPF1: pulse filter length control
= 0,0 → By pass pulse filter
= 0,1 → 50ns
= 1,0 → 100ns
= 1,1 → 150ns

SSEL[4:0]: fine-tune the threshold of input SOG signal
= 16h → recommended value

DDC & IIC Interface

DDC1/DDC2x Mode, DDCRAM1/DDCRAM2 and SlaveA1/SlaveA2 block

The MTV416M supports VESA DDC for both D-sub and DVI interfaces through HSCL1/HSDA1 and HSCL2/HSDA2 pins. The HSCL1/HSDA1 pins access DDCRAM1 by SlaveA1, and the HSCL2/HSDA2 pins access DDCRAM2 by SlaveA2. The MTV416M enters DDC1 mode for both DDC channels after Reset. In this mode, VSYNC is used as data clock. The HSCL1/HSCL2 pin should remain at high. The data output to the HSDA1/HSDA2 pin is taken from a shift register in MTV416M. The shift register automatically fetches EDID data from the lower 128 bytes of the Dual Port RAM (DDCRAM1/DDCRAM2), then sends it in 9-bit packet formats inclusive of a null bit (=1) as packet separator. S/W may enable/disable the DDC1 function by setting/clearing the DDC1en control bit.

The MTV416M switches to DDC2x mode when it detects a high to low transition on the HSCL1/HSCL2 pin. In this mode, the SlaveA1/SlaveA2 IIC block automatically transmits/receives data to/from the IIC Master. The transmitted/received data is taken-from/saved-to the DDCRAM1/DDCRAM2. In simple words, MTV416M can behave as two 24LC02 EEPROMs. The only thing S/W needs to do is to write the EDID data to DDCRAM1/DDCRAM2. These slave addresses of SlaveA1/SlaveA2 block can be chosen by S/W as 5-bit, 6-bit or 7-bit. For example, if S/W chooses 5-bit slave address as 10100b, the SlaveA1 IIC block then responds to slave address 10100xxb. The SlaveA1/SlaveA2 can be enabled/disabled by setting/clearing the EnslvA1/EnslvA2 bit. The lower/upper DDCRAM1/DDCRAM2 can/cannot be written by the IIC Master by setting/clearing the EN128w/En256w bit. Besides, if the Only128 control bit is set, the SlaveA1/SlaveA2 only accesses the lower 128 bytes of the DDCRAM1/DDCRAM2.

The MTV416M returns to DDC1 mode if HSCL1 is kept high for 128 VSYNC clock period. However, it locks in DDC2B mode if a valid IIC address (1010xxxb) has been detected on HSCL1/HSDA1 buses. The DDC2 flag reflects the current DDC status, S/W may clear it by writing a "0" to it.

Slave B Block

There are 2 Slave B IIC blocks, which are connected to HSDA1/HSCL1 and HSDA2/HSCL2 pins separately. These blocks can receive/transmit data using IIC protocols. S/W may write the SLVBADR1/2 register to determine the slave addresses.

In receive mode, the block first detects IIC slave address matching the condition then issues a SlvBMI1/2 interrupt. The data from HSDA1/2 is shifted into shift register then written to RCBBUF1/2 register when a data byte is received. The first byte loaded is word address (slave address is dropped). This block also generates a RCBI1/2 (receives buffer full interrupt) every time when the RCBBUF1/2 is loaded. If S/W is not able to read out the RCBBUF1/2 in time, the next byte in shift register is not written to RCBBUF1/2 and the slave block returns NACK to the master. This feature guarantees the data integrity of communication. The WadrB1/2 flag can tell S/W whether the data in RCBBUF1/2 is a word address or not.

In transmit mode, the block first detects IIC slave address matching the condition, then issues a SlvBMI1/2 interrupt. In the meantime, the data pre-stored in the TXBBUF1/2 is loaded into shift register, resulting in TXBBUF1/2 emptying and generates a TXBI1/2 (transmit buffer empty interrupt). S/W should write the TXBBUF1/2 a new byte for the next transfer before shift register empties. A failure of this process causes data corruption. The TXBI1/2 occurs every time when shift register reads out the data from TXBBUF1/2.

The SlvBMI1/2 is cleared by writing "0" to corresponding bit in INTFLG1/2 register. The RCBI1/2 is cleared by reading out RCBBUF1/2. The TXBI1/2 is cleared by writing TXBBUF1/2.

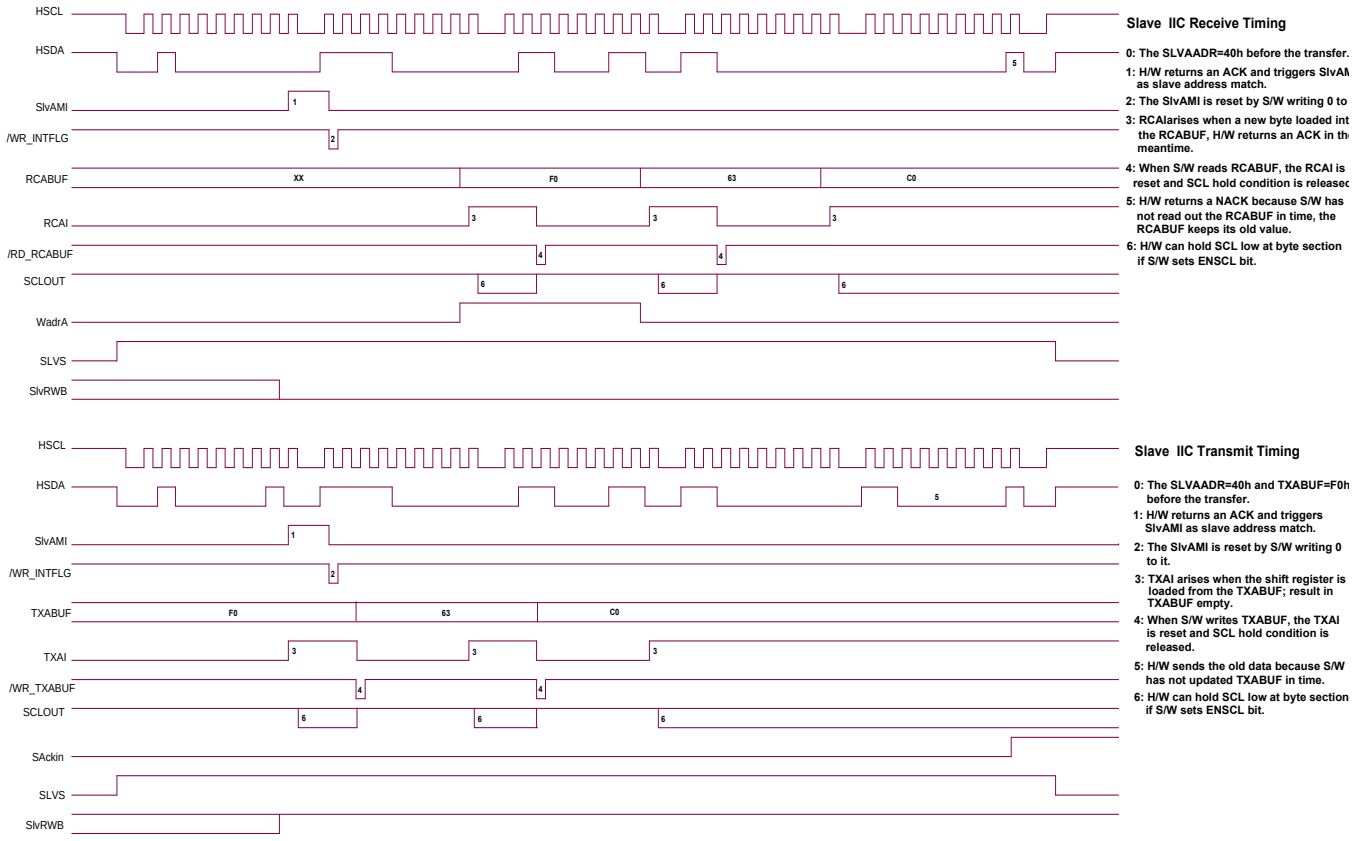


Figure 5 Slave IIC Timing Diagram (Transmit and Receive)

Master Mode IIC Function Block

The master mode IIC block can be connected to the ISDA /ISCL pins or the HSDA1/HSCL1 pins, selected by Msel control bit. Its speed can be selected within the range of 50KHz-400KHz by S/W setting the MIICF1/MIICF0 control bit. The software program can access the external IIC device through this interface. A summary of master IIC access is illustrated as follows.

1). To write IIC Device

1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV416M transmits this byte, a MbufI interrupt is triggered.
4. Programs can write MBUF to transfer next byte or set P bit to stop.

2). To read IIC Device

1. Write MBUF the Slave Address.
2. Set S bit to Start.
3. After the MTV416M transmits this byte, a MbufI interrupt is triggered.
4. Set or reset the MAckO flag according to the IIC protocol.
5. Read out MBUF the useless byte to continue the data transfer.
6. After the MTV416M receives a new byte, the MbufI interrupt is triggered again.

Read MBUF also trigger the next receive operation, but set P bit before read can terminate the operation.

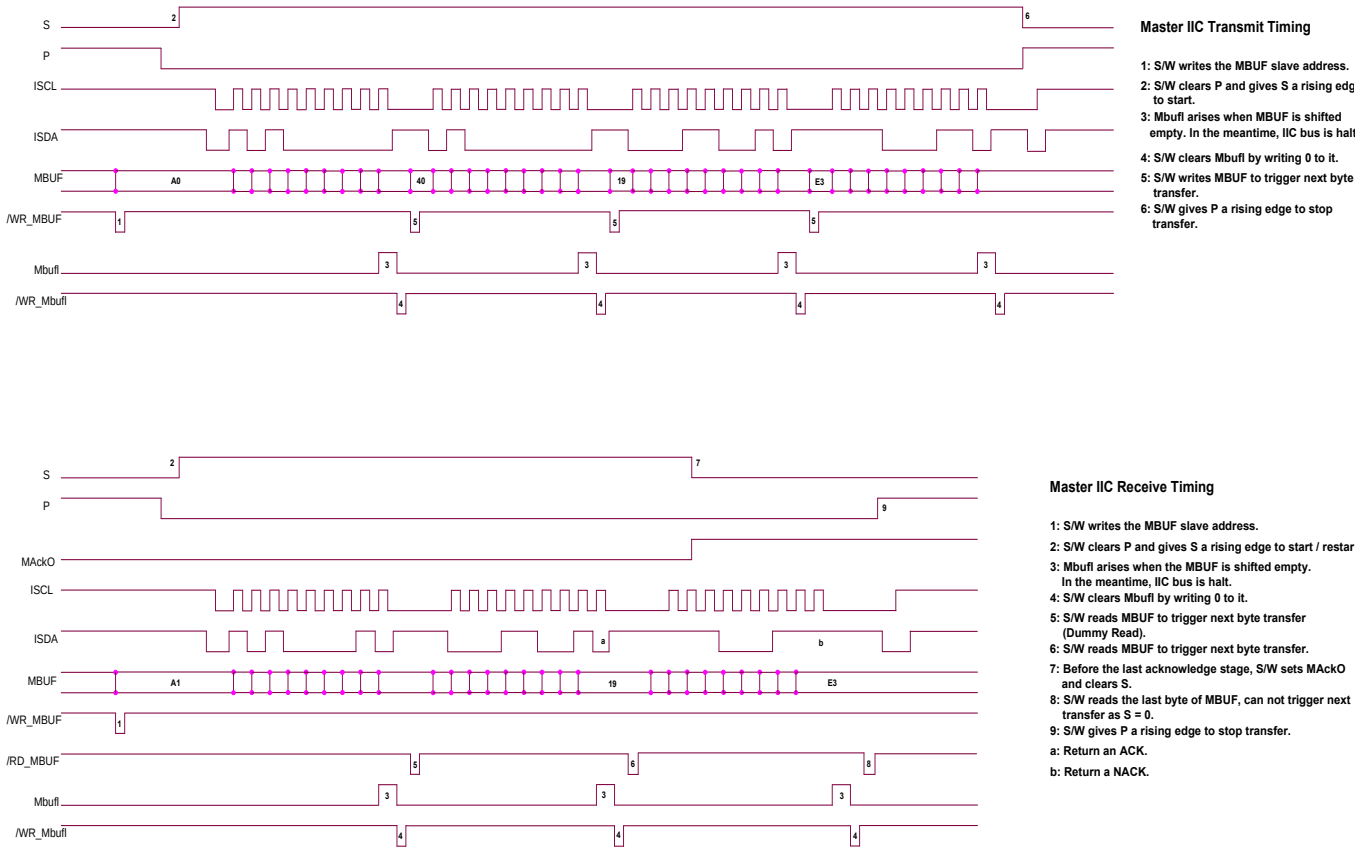


Figure 6 Master IIC Timing Diagram (Transmit and Receive)

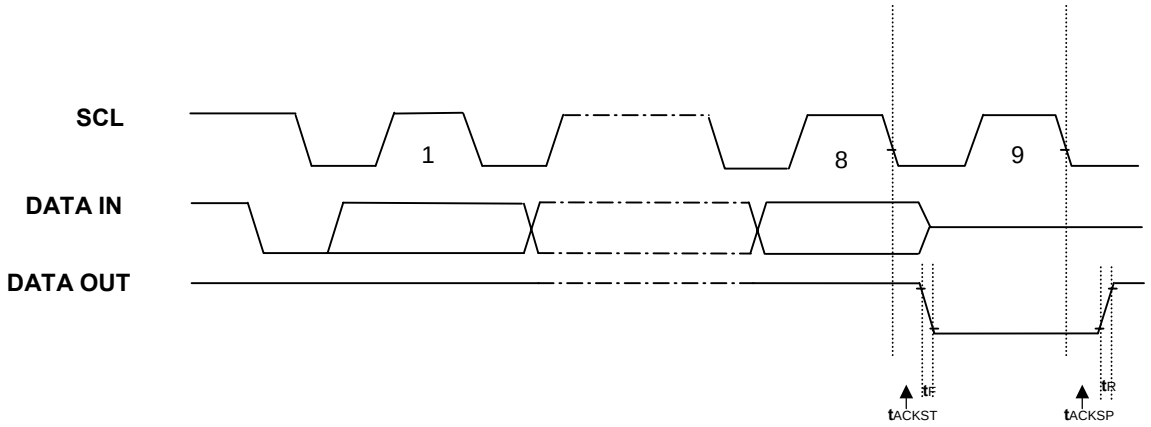


Figure 7 Slave Ack Timing in Write Mode

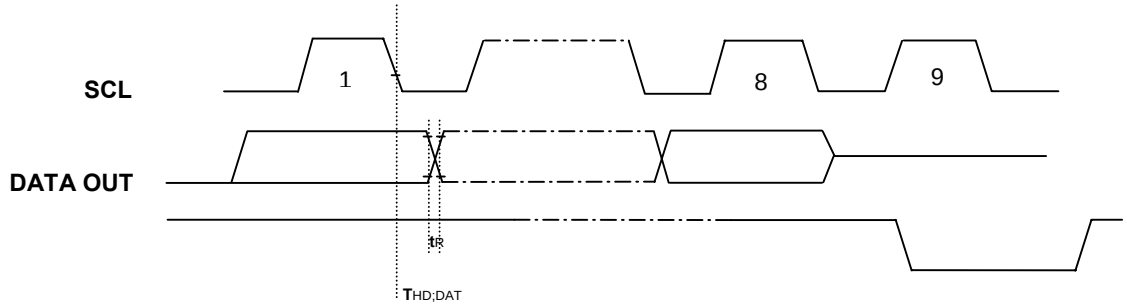


Figure 8 Slave Data Transmission Timing in Read Mode

PARAMETER	SYMBOL	TIME	
		MIN	MAX
Time interval from SCL falling** edge (under VIL) to data starting to update (10% or 90% swing)	THD;DAT	2 x sysclk*	3 x sysclk
Time interval from SCL falling edge (under VIL) to slave starting to update (10% swing)	tACKST	2 x sysclk	3 x sysclk
Time interval from SCL falling edge (under VIL) to slave starting to update (10% swing)	tACKSP	2 x sysclk	3 x sysclk
SDA rise time by slave IIC (10% to 90% swing)	tR	123.9ns	127.1nsns
SDA fall time by slave IIC (90% to 10% swing)	tF	0.85ns	2.79ns

Note: sysclk is the clock input on X1. It is 83ns for 12MHz crystal.
****Note: SCL falling means when SCL drop below VIL of IIC PAD, which is 1.0 volt in typical case.***

Table 3 Slave IIC Data Timing AC Characteristics

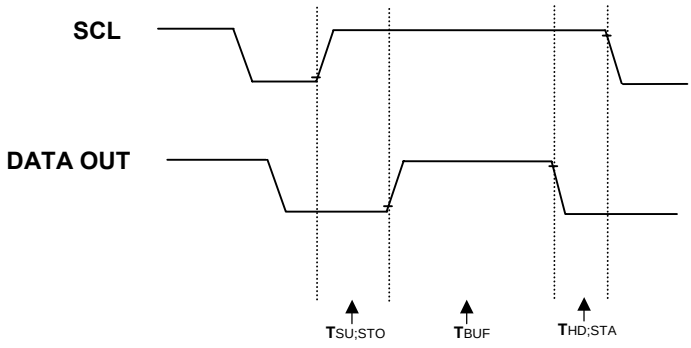


Figure 9 Acceptable IIC Start/Stop Timing

PARAMETER	SYMBOL	MIN	MAX
Time interval from SCL rising edge (over VIH) to SDA rising edge (10% swing)	tSU;STO	600ns	-
Time interval from SDA rising edge to SCL falling edge (90% swing)	THD;STA	600ns	-
Bus free time between stop and start (from 90% to 90% swing)	TBUF	1300ns	-

Table 4 Slave IIC Start/Stop Timing AC Characteristic

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)	DDC2A1	DDC2A2				MAckO	P	S
IICSTUS1	F01h (r)	WadrB1		SlvRWB1	SackIn1	SLVS1			MAckIn
INTFLG1	F03h (r)	TXBI1	RCBI1	SlvBMI1	STOPI1	ReStaI1	WslvA1I	WslvA2I	MbufI
INTFLG1	F03h (w)			SlvBMI1	STOPI1	ReStaI1	WslvA1I	WslvA2I	MbufI
INTEN1	F04h (w)	ETXBI1	ERCBI1	ESlvBMI1	ESTOPI1	EreStaI1	EWSlvA1I	EWSlvA2I	EMbufI
MBUF	F05h (r/w)	Master IIC receives/transmits data buffer							
DDCCTRA1	F06h (w)	Rev7	En128W1	Rev5	Rev4			SlvA1bs1	SlvA1bs0
SLVAADR1	F07h (w)	ENSlvA1	Slave A IIC address						
RCBBUF1	F08h (r)	Slave B IIC receives buffer							
TXBBUF1	F08h (w)	Slave B IIC transmits buffer							
SLVBADR1	F09h (w)	ENSlvB1	Slave B IIC address						
CTRSLVB1	F0Ah(r/w)							Rev1	Rev0
DDCCTRA2	F86h(w)	Rev7	En128W2	Rev5	Rev4			SlvA2bs1	SlvA2bs0
SLVAADR2	F87h(w)	ENSlvA2	Slave A2 IIC address						
IICSTUS2	F91h (r)	WadrB2		SlvRWB2	SackIn2	SLVS2			
INTFLG2	F93h (r)	TX2BI2	RCBI2	SlvBMI2	STOPI2	ReStaI2			
INTFLG2	F93h (w)			SlvBMI2	STOPI2	ReStaI2			
INTEN2	F94h (w)	ETXBI2	ERCBI2	ESlvBMI2	ESTOPI2	EreStaI2			
RCBBUF2	F98h (r)	Slave B IIC receives buffer							
TXBBUF2	F98h (w)	Slave B IIC transmits buffer							
SLVBADR2	F99h (w)	ENSlvB2	Slave B IIC address						
CTRSLVB2	F9Ah(r/w)							Rev1	Rev0

IICCTR (r/w) : IIC interface status/control register.

DDC2A1 = 1 → DDC2 is active for HSCL1/HSDA1 pins.
= 0 → MTV416M remains in DDC1 mode for HSCL1/HSDA1 pins.
DDC2A2 = 1 → DDC2 is active for HSCL2/HSDA2 pins.
= 0 → MTV416M remains in DDC1 mode for HSCL2/HSDA2 pins.
MAckO = 1 → In master receive mode, NACK is returned by MTV416M.
= 0 → In master receive mode, ACK is returned by MTV416M.
S, P = ↑, 0 → Start condition when Master IIC is not during transfer.
= X, ↑ → Stop condition when Master IIC is not during transfer.
= 1, X → Resume transfer after a read/write MBUF operation.

IICSTUS1 (r) : IIC interface status register for Slave B1

WadrB1 = 1 → The data in RCBBUF is word address.

SlvRWB1 = 1 → Current transfer is slave transmit
= 0 → Current transfer is slave receive

SackIn1 = 1 → The external IIC host respond NACK.
SLVS1 = 1 → The slave block has detected a START, cleared when STOP detected.
MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.
= 0 → ACK received from the slave IIC device.

INTFLG1 (r) : Interrupt flag of Slave B1

TXBI1 = 1 → Indicates the TXBBUF need a new data byte, cleared by writing TXBBUF.
RCBI1 = 1 → Indicates the RCBBUF has received a new data byte, cleared by reading RCBBUF.
SlvBMI1= 1 → Indicates the slave IIC address B match condition.
STOPI1= 1 → Indicates the slave IIC has detected a STOP condition for HSCL1/HSDA1 pins.
ReStaI1 = 1 → Indicates the slave IIC has detected a repeat START condition for HSCL1/HSDA1 pins.
WslvA1I = 1 → Indicates the slave A1 IIC has detected a STOP condition of write mode.
WslvA2I = 1 → Indicates the slave A2 IIC has detected a STOP condition of write mode.

INTFLG1 (w) : Interrupt flag of Slave B1. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

SlvBMI1 = 1 → No action
= 0 → Clears SlvBMI1 flag
STOPI1 = 1 → No action.
= 0 → Clears STOPI flag
ReStaI1 = 1 → No action.
= 0 → Clears ReStaI1 flag
WslvA1I = 1 → No action.
= 0 → Clears WslvA1I flag
WslvA2I = 1 → No action.
= 0 → Clears WslvA2I flag
MbufI = 1 → No action.
= 0 → Clears Master IIC bus interrupt flag (MbufI)

INTEN1 (w) : Interrupt enable of Slave B1

ETXBI1 = 1 → Enables TXBBUF interrupt.
ERCBI1 = 1 → Enables RCBBUF interrupt.
ESlvBMI1 = 1 → Enables slave address B match interrupt.
ESTOPI1 = 1 → Enables IIC bus STOP interrupt.
EreStaI1 = 1 → Enables IIC bus repeat START interrupt.
EWSlvA1I = 1 → Enables slave A1 IIC bus STOP of write mode interrupt.
EWSlvA2I = 1 → Enables slave A2 IIC bus STOP of write mode interrupt.
EMbufI = 1 → Enables Master IIC bus interrupt.

MBUF (r) : Master IIC data shift register, after START and before STOP condition, read this register resumes MTV416M's reception from the IIC bus.

MBUF(w) : Master IIC data shift register, after START and before STOP condition, write this register resumes MTV416M's transmission to the IIC bus.

DDCCTRA1 (w) : DDC interface control register for HSCL1, HSDA1 pins.

Rev7 = 1 → reserved
= 0 → Normal operation
En128W1 = 1 → The 128 bytes (00-7F) of DDCRAM1 can be written by IIC master.
= 0 → The 128 bytes (00-7F) of DDCRAM1 cannot be written by IIC master.
Rev5 = 1 → reserved
= 0 → Normal operation
Rev4 = 1 → Normal operation
= 0 → reserved
SlvA1bs1, SlvA1bs0 : Slave IIC block A1's slave address length
= 1,X → reserved
= 0,1 → reserved
= 0,0 → Normal operation

SLVAADR1 (w) : Slave IIC block A1's enable and address

EnslvA1= 1 → Enables slave IIC block A1
= 0 → Disables slave IIC block A1
Bit6-0 : Slave A1 IIC address to which the slave block should respond

RCBBUF1 (r) : Slave IIC block B receives data buffer of Slave B1

TXBBUF1 (w) : Slave IIC block B transmits data buffer of Slave B1.

SLVBADR1 (w) : Slave IIC block B's enable and address of Slave B1

EnslvB1= 1 → Enables slave IIC block B1
= 0 → Disables slave IIC block B1
Bit6-0 : Slave B1IIC address to which the slave block should respond

CTRSLVB1 (r/w) : reserved

DDCCTRA2 (w) : DDC interface control register for HSCL2, HSDA2 pins.

Rev7
En128W2 = 1 → The 128 bytes (00-7F) of DDCRAM2 can be written by IIC master.
= 0 → The 128 bytes (00-7F) of DDCRAM2 cannot be written by IIC master.
Rev5 = 1 → reserved
= 0 → Normal operation
Rev4 = 1 → Normal operation
= 0 → reserved
SlvA2bs1, SlvA2bs0 : Slave IIC block A2's slave address length
= 1,X → reserved
= 0,1 → reserved
= 0,0 → Normal operation

SLVAADR2 (w) : Slave IIC block A2's enable and address

EnslvA2= 1 → Enables slave IIC block A2
= 0 → Disables slave IIC block A2
Bit6-0 : Slave A2 IIC address to which the slave block should respond

IICSTUS2 (r) : IIC interface status register for Slave B2

WadrB2 = 1 → The data in RCBBUF is word address
SlvRWB2 = 1 → Current transfer is slave transmit
= 0 → Current transfer is slave receive
SackIn2 = 1 → The external IIC host respond NACK.
SLVS2 = 1 → The slave block has detected a START, cleared when STOP detected.
MAckIn = 1 → Master IIC bus error, no ACK received from the slave IIC device.
= 0 → ACK received from the slave IIC device.

INTFLG2 (r) : Interrupt flag of Slave B2.

TXBI2 = 1 → Indicates the TXBBUF need a new data byte, cleared by writing TXBBUF.
RCBI2 = 1 → Indicates the RCBBUF has received a new data byte, cleared by reading RCBBUF.
SlvBMI2= 1 → Indicates the slave IIC address B match condition.
STOPI2= 1 → Indicates the slave IIC has detected a STOP condition for HSCL2/HSDA2 pins.
ReStaI2 = 1 → Indicates the slave IIC has detected a repeat START condition for HSCL2/HSDA2 pins.
WslvA1I = 1 → Indicates the slave A1 IIC has detected a STOP condition of write mode.
WslvA2I = 1 → Indicates the slave A2 IIC has detected a STOP condition of write mode.

INTFLG2 (w) : Interrupt flag of Slave B2. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

SlvBMI2 = 1 → No action
= 0 → Clears SlvBMI flag
STOPI2 = 1 → No action.
= 0 → Clears STOPI flag
ReStaI2 = 1 → No action.
= 0 → Clears ReStaI flag
WslvA1I = 1 → No action.
= 0 → Clears WslvA1I flag
WslvA2I = 1 → No action.
= 0 → Clears WslvA2I flag
MbufI = 1 → No action

INTEN2 (w) : Interrupt enable of Slave B2

ETXBI2 = 1 → Enables TXBBUF interrupt
ERCBI2 = 1 → Enables RCBBUF interrupt
ESlvBMI2 = 1 → Enables slave address B match interrupt
ESTOPI2 = 1 → Enables IIC bus STOP interrupt
EreStaI2 = 1 → Enables IIC bus repeat START interrupt
EWSlvA1I = 1 → Enables slave A1 IIC bus STOP of write mode interrupt
EWSlvA2I = 1 → Enables slave A2 IIC bus STOP of write mode interrupt
EMbufI = 1 → Enables Master IIC bus interrupt

RCBBUF2 (r) : Slave IIC block B receives data buffer of Slave B2.

TXBBUF2 (w) : Slave IIC block B transmits data buffer of Slave B2.

SLVBADR2 (w) :Slave IIC block B's enable and address of Slave B2.

EnslvB2= 1 → Enables slave IIC block B2.

= 0 → Disables slave IIC block B2.

Bit6-0 : Slave B2 IIC address to which the slave block should respond

CTRSLVB2 (r/w) : reserved

A/D Converter

The MTV416M is equipped with 4 channels 6-bit Analog to Digital Converters (ADC). The ADC conversion range is from VSS to VDD, Programmers can select the current convert channel by setting the SADC1/SADC0 bit. The conversion rate for the ADC is 16us/4channels when the crystal/oscillator frequency is 12MHz.

The ADC compares the input pin voltage with internal VDD*N/64 voltage (where N = 0 - 63). The ADC output value is N when pin voltage is greater than VDD*N/64 and smaller than VDD*(N+1)/64.

Every time when users write a 1 to ENADC, ADC will start a sequence to do 4 channels' conversion. After the sequence completes, ADCF will be set automatically. Users can check this flag to read back the results. The results of the channels, which are not selected, will not be updated.

User should set AdxE as high (See PADMOD50) and set Port4 in input mode (See P4E) before use ADC.

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC0	F10h (r)	ADCF		ADC0 convert Result					
ADC1	F11h (r)			ADC1 convert Result					
ADC2	F12h (r)			ADC2 convert Result					
ADC3	F13h (r)			ADC3 convert Result					

ADC (w) : ADC control.

ENADC = 1 → Enables ADC conversion.

SADC0 = 1 → Selects ADC0 pin input.

SADC1 = 1 → Selects ADC1 pin input.

SADC2 = 1 → Selects ADC2 pin input.

SADC3 = 1 → Selects ADC3 pin input.

ADC0 ~ ADC3 (r) :

ADCF: ADC complete flag.

ADC converts result: the 6-bit result for each channel.

In System Programming Function (ISP)

The Flash memory can be programmed by a specific WRITER in parallel mode, or by IIC Host in serial mode while the system is working. ISP can be done through SlaveB1 or SlaveB2 IIC channels. (i.e. via HSCL1/HSDA1 pins or HSCL2/HSDA2 pins) User should let NEA be high before program embedded program flash memory. The features of ISP are outlined as follows:

1. Single 3.3V power supply for Program/Erase/Verify.
2. Block Erase: 1024 bytes for Program Code, 10mS
3. Whole Flash erase (Blank): 10mS
4. Byte/Word programming Cycle time: 60uS per byte
5. Read access time: 50ns
6. Only one two-pin IIC bus (shared with DDC2) is needed for ISP in user/factory mode.

7. IIC Bus clock rates up to 140KHz.
8. Whole 64K-byte Flash programming within 6 Sec. (It depends on the external IIC speed)
9. CRC check provides 100% coverage for all single/double bit errors.

There are two methods to enter the ISP mode, which are described below:

Method 1: The Valid ISP Slave Address and Compared data are transmitted.
After Power On/Reset, if the MTV416M receives the valid "ISP Enable Command" by IIC bus, the MTV416M will enter into ISP mode directly and force 8051 stop. User can disable this way to enter into ISP mode. If any one of the ISP compared data 1, 2, and 3 registers is cleared to "00000000" by S/W, this way to enter ISP mode will be disabled.

Method 2: Write 93h to ISP enable register (ISPEN).
After Power On/Reset, The MTV416M runs the original Program Code. Once the S/W detects an ISP request (by key or IIC), S/W can accept the request following the steps below:
1) Clear watchdog to prevent reset during ISP period.
2) Disable all interrupt to prevent CPU wake-up.
3) Write IIC address of ISP slave to ISPSLV for communication.
4) Write 93h to ISP enable register (ISPEN) to enable ISP.

Reg name	addr	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							
ISPCMP1	F0Dh(w)	ISP compared data 1 [7:0]							
ISPCMP2	F0Eh(w)	ISP compared data 2 [7:0]							
ISPCMP3	F0Fh(w)	ISP compared data 3 [7:0]							

ISPSLV (w) : ISP Slave IIC's address.
bit7-2 : ISP Slave IIC's address to which the ISP block should respond. The default value is 100101.

ISPEN (w) : Write 93h to enable ISP Mode for ISP enable method 2.

ISPCMP1 (w) : The ISP compared data 1 for ISP enable method 1. The default value is ACh.

ISPCMP2 (w) : The ISP compared data 2 for ISP enable method 1. The default value is CAh.

ISPCMP3 (w) : The ISP compared data 3 for ISP enable method 1. The default value is 53h.

High Driving Pads

MTV416M has 4 ports (P1.1 – P1.4), which can sink 10mA current each.

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DRCTRL	F5Ch(w)	DE2	DE1		EH14	EH13	EH12	EH11	

DRCTRL (w) : driving strength control signals

DE2 = 1 → Decrease the slew rate of clock out
= 0 → Normal operation

DE1 = 1 → Reserved.
= 0 → Normal operation

EH14 = 1 → Enlarge the sink current of P1.4 to 10mA.
= 0 → Normal operation
EH13 = 1 → Enlarge the sink current of P1.3 to 10mA.
= 0 → Normal operation
EH12 = 1 → Enlarge the sink current of P1.2 to 10mA.
= 0 → Normal operation
EH11 = 1 → Enlarge the sink current of P1.1 to 10mA.
= 0 → Normal operation

Etimer

The Etimer is a 16-bit Timer/Counter, which provides capture/reload functions like Timer 2 in 8052. The type is selected by C/T2 in the SFR ETCTR. Etimer has 2 modes, capture/auto-reload (up or down counting). The modes are selected by CP/RL2 in ETCTR. Etimer contains 2 8-bit registers, TLET and THET. When it is used in the timer mode, THET-TLET count rate is 1/12 of the crystal/oscillator frequency. In the counter mode, the counter is incremented when 1→0 transition at Port1.0,

1. Capture mode
   In the capture mode, if EXEN2 = 0, Etimer is a 16-bit timer or counter. When EXEN2 = 0, Etimer counters up to FFFFh and then set TF2 upon overflow. This bit will generate an interrupt (INT1) to 8051. If EXEN2 = 1, Etimer capture the current value in THET-TLET into RCAPETH-RCAPETL, respectively when 1→0 transition at Port1.1. This will also generate an interrupt.
2. Auto-reload mode
   Etimer can be programmed to count-up or down when in auto-reload mode. This feature is selected by DCEN in SFR ETMOD. Down Counting is possible only if RCLKEN = TCLKEN = CP/RL2 = 0 and DCEN = 1. This does not mean however that with these conditions down counting will begin. For the down counting to begin, DCEN has to be 1 and also P1.1 has to be 0. If EXEN2 = 0, Etimer counts up to 0FFFFh and then set TF2 (overflow). At this mode, the counter is reloaded the 16-bit value from RCAPETH-RCAPETL. If EXEN2 = 1, the reload function can be triggered by overflow or by 1→0 transition at Port 1.1.

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
ETCTR	F88h(r/w)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
ETMOD	F89h(r/w)								DCEN
THET	F8Ah(r/w)	Etimer high 8-bit register							
TLET	F8Bh(r/w)	Etimer low 8-bit register							
RCAPETH	F8Ch(r/w)	Etimer high 8-bit capture/reload register							
RCAPETL	F8Dh(r/w)	Etimer low 8-bit capture/reload register							
EINT1PEN	F8Eh (w)	EEINT	ETE	TSTP1	IP77E				

ETCTR (w) : Etimer control register
TF2 = 1 → No actions
= 0 → Clear Etimer overflow interrupt
EXF2 = 1 → No actions
= 0 → Clear Etimer external capture / reload interrupt
RCLK = 1 → Serial port mode 1 or 3 uses the timer2 overflow pulse as receive clock input.
= 0 → Serial port mode 1 or 3 uses the timer1 overflow pulse as receive clock input.
TCLK = 1 → Serial port mode 1 or 3 uses the timer2 overflow pulse as transmit clock input.
= 0 → Serial port mode 1 or 3 uses the timer1 overflow pulse as transmit clock input.
EXEN2 = 1 → Enable Port1.1 capture / reload trigger
= 0 → Disable Port1.1 capture / reload trigger
TR2 = 1 → Enable Etimer
= 0 → Disable Etimer
C/T2 = 1 → Etimer functions as a counter

= 0 → Etimer functions as a timer
CP/RL2 = 1 → Set Etimer in Capture mode
= 0 → Set Etimer in Auto-reload mode

ETCTR (r) : Etimer control register
TF2 = 1 → Indicates an overflow interrupt of Etimer.
EXF2 = 1 → Indicates the interrupt of a negative edge of on P1.1 when EXEN2=1
RCLK → RCLK state
TCLK → TCLK state
EXEN2 → Exen2 state
TR2 → TR2 state
C/T2 → C/T2 state
CP/RL2 → CP/RL2 state

ETMOD (w/r) : Etimer mode control
DCEN = 0 → Disable down counting function
= 1 → Enable down counting function

THET (w/r) : Etimer high 8-bit register

TLET (w/r) : Etimer low 8-bit register

RCAPETH (w/r) : Etimer high 8-bit capture/reload register

RCAPETL (w/r) : Etimer low 8-bit capture/reload register

EINT1PEN (w) : External interrupt control
ETINT1 = 1 Enable P3.3 as external interrupt1 trigger
= 0 Disable P3.3 as external interrupt1 trigger
ETE = 1 Enable Etimer interrupt
= 0 Disable Etimer interrupt
TSTP1 = 1 Reserved
= 0 Normal operation
IP77E = 1 Reserved
= 0 Normal operation

Watchdog Timer

The Watchdog Timer automatically generates a device reset when it is overflowed. The interval of overflow is 0.25 sec x N, where N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power on reset; users can activate this function by setting WEN, and clear the timer by setting WCLR.

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0

WDT (w) : Watchdog Timer control register.
WEN = 1 → Enable Watchdog Timer
WCLR = 1 → Clear Watchdog Timer
WDT2 ~ WDT0 = 0 → Overflow interval = 8 x 0.25 sec.
= 1 → Overflow interval = 1 x 0.25 sec.
= 2 → Overflow interval = 2 x 0.25 sec.
= 3 → Overflow interval = 3 x 0.25 sec.
= 4 → Overflow interval = 4 x 0.25 sec.
= 5 → Overflow interval = 5 x 0.25 sec.
= 6 → Overflow interval = 6 x 0.25 sec.
= 7 → Overflow interval = 7 x 0.25 sec.

Memory Map of XFR

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
IICCTR	F00h (r/w)	DDC2A1	DDC2A2				MAckO	P	S
IICSTUS1	F01h (r)	WadrB1		SlvRWB1	SackIn1	SLVS1			MAckIn
INTFLG1	F03h (r)	TXBI1	RCBI1	SlvBMI1	STOPI1	ReStaI1	WslvA1I	WslvA2I	MbufI
INTFLG1	F03h (w)			SlvBMI1	STOPI1	ReStaI1	WslvA1I	WslvA2I	MbufI
INTEN1	F04h (w)	ETXBI1	ERCBI1	ESlvBMI1	ESTOPI1	EreStaI1	EWSlvA1I	EWSlvA2I	EMbufI
MBUF	F05h (r/w)	Master IIC receives/transmits data buffer							
DDCCTRA1	F06h (w)	Rev7	En128W1	Rev5	Rev4			SlvA1bs1	SlvA1bs0
SLVAADR1	F07h (w)	ENSlvA1	Slave A IIC address						
RCBBUF1	F08h (r)	Slave B IIC receives buffer							
TXBBUF1	F08h (w)	Slave B IIC transmits buffer							
SLVBADR1	F09h (w)	ENSlvB1	Slave B IIC address						
CTRSLVB1	F0Ah(r/w)							Rev1	Rev0
ISPSLV	F0Bh(w)	ISP Slave address							
ISPEN	F0Ch(w)	Write 93h to enable ISP Mode							
ISPCMP1	F0Dh(w)	ISP compared data 1 [7:0]							
ISPCMP2	F0Eh(w)	ISP compared data 2 [7:0]							
ISPCMP3	F0Fh(w)	ISP compared data 3 [7:0]							
ADC	F10h (w)	ENADC				SADC3	SADC2	SADC1	SADC0
ADC0	F10h (r)	ADCF		ADC0 convert Result					
ADC1	F11h (r)			ADC1 convert Result					
ADC2	F12h (r)			ADC2 convert Result					
ADC3	F13h (r)			ADC3 convert Result					
WDT	F18h (w)	WEN	WCLR				WDT2	WDT1	WDT0
DA0	F20h(r/w)	Pulse width of PWM DAC 0							
DA1	F21h(r/w)	Pulse width of PWM DAC 1							
DA2	F22h(r/w)	Pulse width of PWM DAC 2							
DA3	F23h(r/w)	Pulse width of PWM DAC 3							
DA2FC	F2Dh(r/w)			D2B5	D2B4	D2B3	D2B2	D2B1	D2B0
DA3FC	F2Eh(r/w)			D3B5	D3B4	D3B3	D3B2	D3B1	D3B0
P5B0	F30h(w)								P50
P5B1	F31h(w)							P51	
P5B2	F32h(w)						P52		
P5B3	F33h(w)					P53			
P5B4	F34h(w)				P54				
P5B5	F35h(w)			P55					
P5B6	F36h(w)		P56						
P5B7	F37h(w)	P57							
P6B0	F38h(w)								P60
P6B1	F39h(w)							P61	
P6B2	F3Ah(w)						P62		
P6B3	F3Bh(w)					P63			
P6B4	F3Ch(w)				P64				
P6B5	F3Dh(w)			P65					
P6B6	F3Eh(w)		P66						
P6B7	F3Fh(w)	P67							
HVSTUS	F40h(r)	CVpre		Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	F41h(r)	Hovf		HF13	HF12	HF11	HF10	HF9	HF8
HCNTL	F42h(r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	F43h(r)	Vovf				VF11	VF10	VF9	VF8
VCNTL	F44h(r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
HVCTR0	F40h(w)	C1	C0	NoHins	ENSOG	ENSOGD		HBpl	VBpl
HVCTR3	F43h(w)		CLPEG	CLPPO	CLPW2	CLPW1	CLPW0		
HVCTR4	F44h(w)							DF1	DF0
HVFILT	F46h(w)	VPF1	VPF0	VNMW	VAW	HPF1	HPF0	HNMW	HAW

REG NAME	ADDR	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
INTFLG	F48h(r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	Hsync	Vsync
INTEN	F49h(w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EHsync	EVsync
SOGCTL	F4A(w)	SPF1	SPF0	SSEL[4:0]					
PADMOD50	F50h(w)					AD3E	AD2E	AD1E	AD0E
PADMOD51	F51h(w)								ICE_T
PADMOD52	F52h(w)	HIIC1E	IIICE	HIIC2E	CKOE1	HCLPE	CKOE2		
PADMOD53	F53h(w)	P57oe	P56oe	P55oe	P54oe	P53oe	P52oe	P51oe	P50oe
PADMOD54	F54h(w)	P67oe	P66oe	P65oe	P64oe	P63oe	P62oe	P61oe	P60oe
PADMOD55	F55h(w)	COP17							COP10
OPTION56	F56h(w)	PWMF	DIV253	Rev5	Rev4	ENSCL	Msel	MIICF1	MIICF0
PADMOD57	F57h(w)					P43oe	P42oe	P41oe	P40oe
P4B0	F58h(w)								P40
P4B1	F59h(w)							P41	
P4B2	F5Ah(w)						P42		
P4B3	F5Bh(w)					P43			
DRCTRL	F5Ch(w)	DE2	DE1		EH14	EH13	EH12	EH11	
PADMOD5D	F5Dh(w)	P17E	P16E	P15E	P14E	P13E	P12E	P11E	P10E
PADMOD5E	F5Eh(w)			P75E	P74E	P73E	P72E	P71E	P70E
PADMOD5F	F5Fh(w)			P75oe	P74oe	P73oe	P72oe	P71oe	P70oe
P7B0	F70h(w)								P70
P7B1	F71h(w)							P71	
P7B2	F72h(w)						P72		
P7B3	F73h(w)					P73			
P7B4	F74h(w)				P74				
P7B5	F75h(w)			P75					
PORT 5	F80h(r/w)	P57	P56	P55	P54	P53	P52	P51	P50
PORT 6	F81h(r/w)	P67	P66	P65	P64	P63	P62	P61	P60
PORT 4	F82h(r/w)					P43	P42	P41	P40
PORT 7	F83h(r/w)			P75	P74	P73	P72	P71	P70
DDCCTRA2	F86h(w)	Rev7	En128W2	Rev5	Rev4			SlvA2bs1	SlvA2bs0
SLVAADR2	F87h(w)	ENSlvA2	Slave A2 IIC address						
ETCTR	F88h(r/w)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2	CP/RL2
ETMOD	F89h(r/w)								DCEN
THET	F8Ah(r/w)	Etimer high 8-bit register							
TLET	F8Bh(r/w)	Etimer low 8-bit register							
RCAPETH	F8Ch(r/w)	Etimer high 8-bit capture/reload register							
RCAPETL	F8Dh(r/w)	Etimer low 8-bit capture/reload register							
EINT1PEN	F8Eh (w)	EEINT	ETE	TSTP1	IP77E				
IICSTUS2	F91h (r)	WadrB2		SlvRWB2	SackIn2	SLVS2			
INTFLG2	F93h (r)	TX2BI2	RCBI2	SlvBMI2	STOPI2	ReStaI2			
INTFLG2	F93h (w)			SlvBMI2	STOPI2	ReStaI2			
INTEN2	F94h (w)	ETXBI2	ERCBI2	ESlvBMI2	ESTOPI2	EreStaI2			
RCBBUF2	F98h (r)	Slave B IIC receives buffer							
TXBBUF2	F98h (w)	Slave B IIC transmits buffer							
SLVBADR2	F99h (w)	ENSlvB2	Slave B IIC address						
CTRSLVB2	F9Ah(r/w)							Rev1	Rev0

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

at: Ta= 0 to 70 ^{o}C, VSS=0V

NAME	SYMBOL	RANGE	UNIT
Maximum Supply Voltage	VDD	-0.3 to +3.6	V
Maximum Input Voltage (HSYNC, VSYNC & open-drain pins)	Vin1	-0.3 to 3.3+0.3	V
Maximum Input Voltage (other pins)	Vin2	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	^{o}C
Maximum Storage Temperature	Tstg	-25 to +125	^{o}C

Recommended Operating Conditions

at: Ta= 0 to 70 ^{o}C, VSS=0V

NAME	SYMBOL	CONDITION	MIN	MAX	UNIT
Supply Voltage	VDD	3.3V application	3.0	3.6	V
Input "H" Voltage	Vih	3.3V application	0.6 x VDD	VDD +0.3	V
Input "L" Voltage	Vil	3.3V application	-0.3	0.3 x VDD	V
Operating Freq.	Fopg	3.3V application	-	24	MHz

DC Characteristics

at: Ta=0 to 70 ^{O}C, VDD=3.3V, VSS=0V

NAME	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Output "H" Voltage, open drain pin	Voh1	VDD=3.3V, Ioh=0uA	2.65			V
Output "H" Voltage, 8051 I/O port pin	Voh2	VDD=3.3V, Ioh=-50uA	2.65			V
Output "H" Voltage, CMOS output	Voh3	VDD=3.3V, Ioh=-4mA	2.65			V
Output "L" Voltage	Vol	Iol=5mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=3.3V	150		250	Kohm
Pin Capacitance	Cio				15	pF

AC Characteristics

at: Ta=0 to 70 ^{O}C, VDD=3.3V, VSS=0V

NAME	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Crystal Frequency	fXtal			12	24	MHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		94.86	KHz
HS input pulse Width	tHIPW	fXtal=12MHz	0.3		7.5	uS
VS input pulse Width	tVIPW	fXtal=12MHz	3			uS
HSYNC to Hblank output jitter	tHHBJ				5	nS
H+V to Vblank output delay	tVVBD	fXtal=12MHz		8		uS
VS pulse width in H+V signal	tVCPW	FXtal=12MHz	20			uS

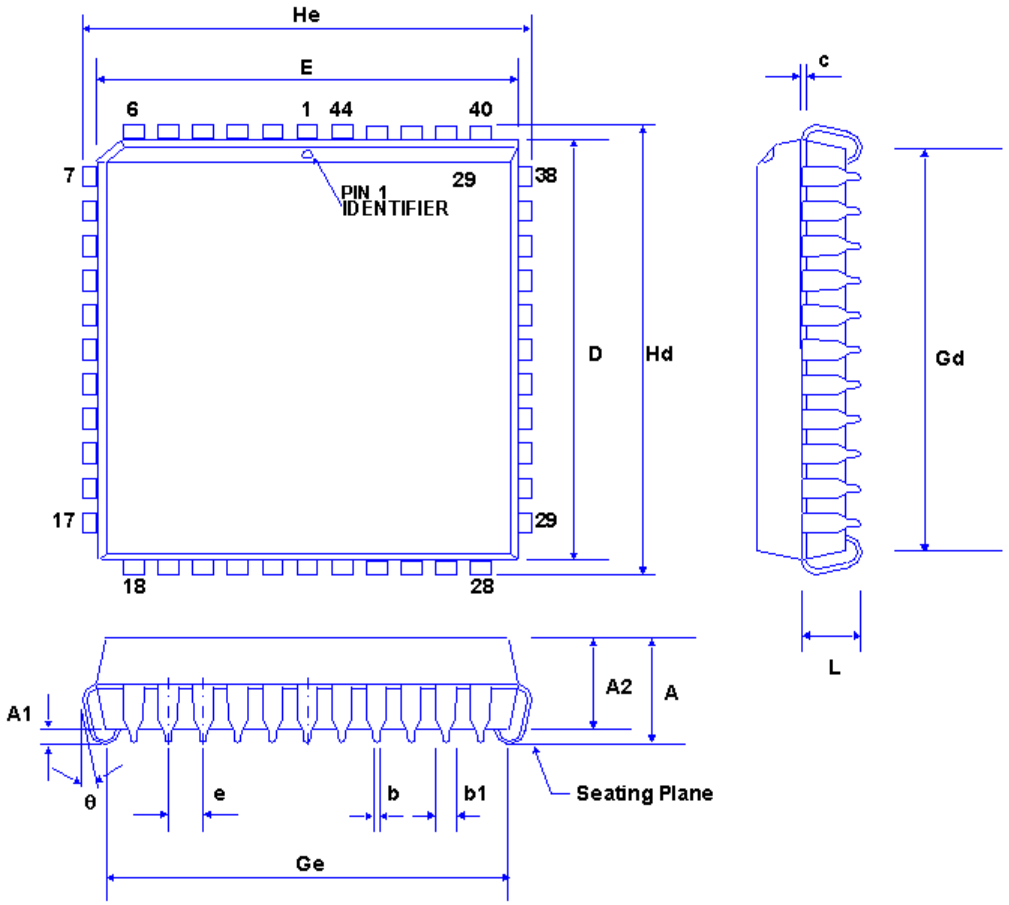
Test Mode Condition

In normal application, users should avoid the MTV416M entering its test mode or writer mode, outlined as follows: adding pull-up resistor to HSCL1/HSDA1/HSCL2/HSDA2 pins is recommended.

Test Mode: RESET's falling edge & HSCL1=0 & HSDA1 & HSCL2=0 & HSDA2 = 0

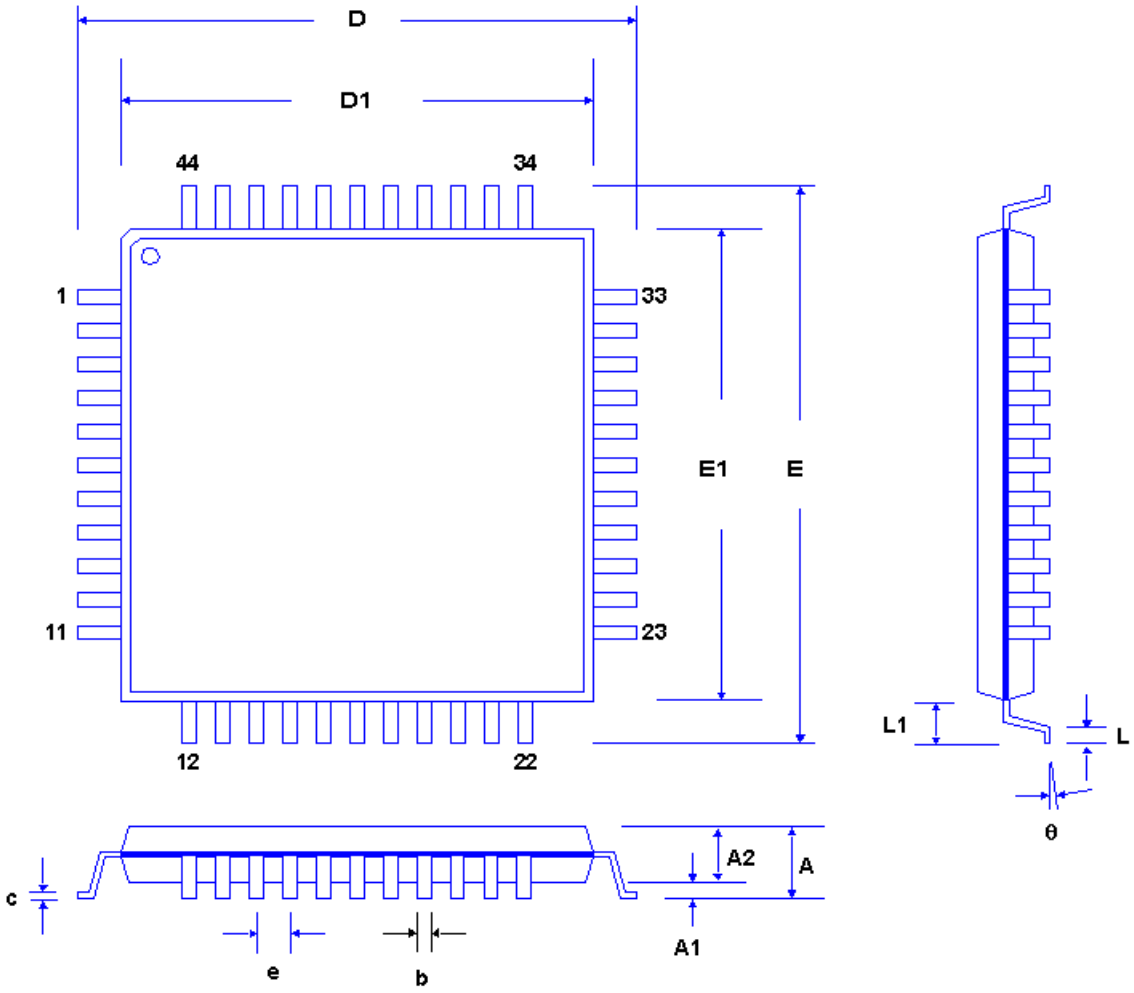
PACKAGE OUTLINE

44-pin PLCC



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	4.70	-	-	0.185
A1	0.51	-	-	0.020	-	-
A2	3.70	3.80	3.90	0.145	0.150	0.155
b	0.41	0.46	0.56	0.016	0.018	0.022
b1	0.65	0.70	0.80	0.026	0.028	0.032
c	0.18	0.25	0.33	0.007	0.010	0.013
D	16.46	16.60	16.71	0.648	0.653	0.658
E	16.46	16.60	16.71	0.648	0.653	0.658
e	1.27 (Typ)			0.050 (Typ)		
Gd	15.00	15.50	16.00	0.590	0.610	0.630
Ge	15.00	15.50	16.00	0.590	0.610	0.630
Hd	17.30	17.50	17.80	0.680	0.690	0.700
He	17.30	17.50	17.80	0.680	0.690	0.700
L	2.29	2.54	2.80	0.090	0.100	0.110
θ	0º	-	10º	0º	-	10º

44-PIN QFP



SYMBOL	DIMENSION IN MILLIMETERS			DIMENSION IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	2.70	-	-	0.105
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	1.90	2.00	2.20	0.075	0.079	0.087
b	0.3 (Typ)			0.012 (Typ)		
c	0.10	0.15	0.20	0.004	0.006	0.008
D	13.00	13.20	13.40	0.510	0.520	0.530
D1	9.90	10.00	10.10	0.390	0.040	0.041
E	13.00	13.20	13.40	0.510	0.520	0.530
E1	9.90	10.00	10.10	0.390	0.040	0.041
e	0.80 (Typ)			0.030 (Typ)		
L	0.73	0.88	0.93	0.029	0.035	0.037
L1	-	1.60	-	-	0.063	-
θ	0º	-	7º	0º	-	7º

ORDERING INFORMATION

PREFIX	NORMAL PART / GREEN PACKAGE PART			PACKAGE TYPE
	NORMAL	Pb-FREE	ALL GREEN	
MTV	416M	416PM	416GM	V: PLCC F: QFP

Example: **MTV 416PM V**