MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Advance Information

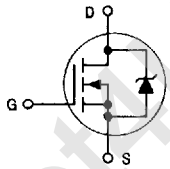
TMOS E-FET™
Power Field Effect Transistor
N-Channel Enhancement-Mode Silicon Gate

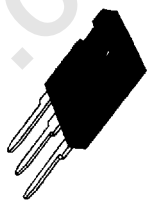
MTW10N40E
Motorola Preferred Device

TMOS POWER FET
10 AMPERES
$R_{DS(on)}$ = 0.55 OHM
400 VOLTS

This advanced TMOS E-FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain-to-source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





CASE 340F-03
TO-247AE

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	400	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	400	Vdc
Gate-Source Voltage — Continuous	V_{GS}	±20	Vdc
Drain Current — Continuous @ T_C = 25°C — Continuous @ T_C = 100°C — Single Pulse ($t_p \leq 10$ µs)	I_D I_D I_{DM}	10 7.0 40	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	150 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C
Single Pulse Drain-to-Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 10 Vpk, I_L = 10 Apk, L = 10.4 mH, R_G = 25 Ω)	E_{AS}	520	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 40	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	260	°C

This document contains information on a new product. Specifications and information are subject to change without notice.

E-FET is a trademark of Motorola, Inc.

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Preferred devices are Motorola recommended choices for future use and best overall value.

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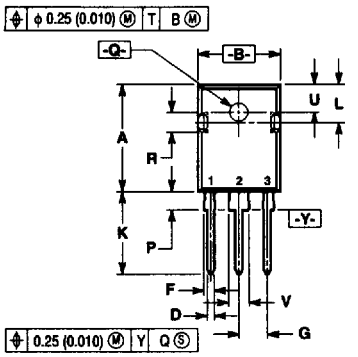
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

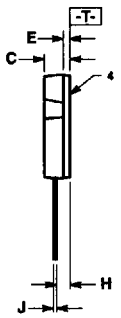
Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage (V_{GS} = 0 V, I_D = 250 µAdc) Temperature Coefficient (Positive)		BV_{DSS}	400 —	— 360	— —	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 400 Vdc, V_{GS} = 0) (V_{DS} = 400 Vdc, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	250 1000	µAdc
Gate-Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0)		I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 µAdc) Temperature Coefficient (Negative)		$V_{GS(th)}$	2.0 —	— 5 0	4.0 —	Vdc mV/°C
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 5 0 Adc)		$R_{DS(on)}$	—	—	0.55	Ohm
Drain-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 10 Adc) (I_D = 5.0 Adc, T_J = 125°C)		$V_{DS(on)}$	— —	— —	6 6 5.5	Vpk
Forward Transconductance (V_{DS} = 50 Vdc, I_D = 5 0 Adc)		g_{FS}	4.0	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	1570	2355	pF
Output Capacitance		C_{oss}	—	230	345	
Reverse Transfer Capacitance		C_{rss}	—	55	83	
SWITCHING CHARACTERISTICS*†						
Turn-On Delay Time	(V_{DD} = 200 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc, R_g = 9 1 Ω)	$t_{d(on)}$	—	25	50	ns
Rise Time		t_r	—	37	75	
Turn-Off Delay Time		$t_{d(off)}$	—	75	150	
Fall Time		t_f	—	31	65	
Gate Charge	(V_{DS} = 320 Vdc, I_D = 10 Adc, V_{GS} = 10 Vdc)	Q_T	—	75	110	nC
		Q_1	—	14	—	
		Q_2	—	41	—	
		Q_3	—	30	—	
SOURCE-DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 10 Adc, V_{GS} = 0) (I_S = 10 Adc, V_{GS} = 0, T_J = 125°C)	V_{SD}	— —	1 3 1 2	2 0 —	Vdc
Reverse Recovery Time	(I_S = 10 Adc, V_{GS} = 0, dI_S/dt = 100 A/µs)	t_{rr}	—	330	—	ns
		t_a	—	220	—	
		t_b	—	110	—	
Reverse Recovery Stored Charge		Q_{RR}	—	4 3	—	µC
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die)		L_D	— —	5.0 —	— —	nH
Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad)		L_S	—	13	—	nH

*Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

† Switching characteristics are independent of operating junction temperature.

PACKAGE OUTLINE DIMENSIONS AND FOOTPRINTS (continued)



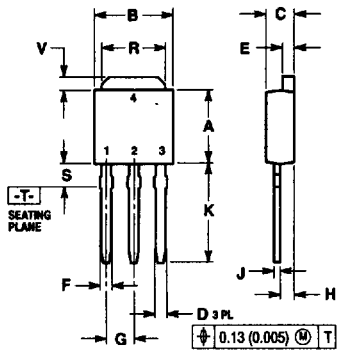


STYLE 1
PIN 1 GATE
2 DRAIN
3 SOURCE
4 DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION MILLIMETER
3 340F-01 AND -02 OBSOLETE, NEW STANDARD 340F-03

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.40	20.90	0.803	0.823
B	15.44	15.95	0.608	0.628
C	4.70	5.21	0.185	0.205
D	1.09	1.30	0.043	0.051
E	1.50	1.63	0.059	0.064
F	1.80	2.18	0.071	0.086
G	5.45 BSC		0.215 BSC	
H	2.56	2.87	0.101	0.113
J	0.48	0.68	0.019	0.027
K	15.57	16.08	0.613	0.633
L	7.26	7.50	0.286	0.295
P	3.10	3.38	0.122	0.133
Q	3.50	3.70	0.138	0.145
R	3.30	3.80	0.130	0.150
U	5.30 BSC		0.209 BSC	
V	3.05	3.40	0.120	0.134

CASE 340F-03
(TO-247)



STYLE 2:
PIN 1 GATE
2 DRAIN
3. SOURCE
4. DRAIN

NOTES
1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982
2 CONTROLLING DIMENSION: INCH
3 369-01 THRU -05 OBSOLETE, NEW STANDARD 369-06

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.22	0.235	0.245
B	6.35	6.73	0.250	0.265
C	2.19	2.38	0.086	0.094
D	0.69	0.88	0.027	0.035
E	0.84	1.01	0.033	0.040
F	0.94	1.19	0.037	0.047
G	2.29 BSC		0.090 BSC	
H	0.87	1.01	0.034	0.040
J	0.46	0.58	0.018	0.023
K	8.89	9.65	0.350	0.380
R	4.45	5.46	0.175	0.215
S	1.27	2.28	0.050	0.090
V	0.77	1.27	0.030	0.050

CASE 369-06
(TO-251)

5