

# MU1506 LDMOS TRANSISTOR

Document Number: MU1506  
Product Datasheet V3.0

## 1500MHz, 60W, 28V High Power RF LDMOS FETs

### Description

The MU1506 is a 60-watt, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz. It can be used in Class AB/B and Class C for all typical modulation formats.

- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$  Volts,  $I_{DQ} = 350$  mA, CW.

Frequency	Gp (dB)	$P_{-1dB}$ (W)	$\eta_D@P_{-1}$ (%)
1000 MHz	19	60	60

### MU1506



### Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

### Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+95	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+40	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$ , $T_J = 200^\circ\text{C}$ , DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### DC Characteristics

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Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$	95	——		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 75V, V_{GS} = 0 V)$	$I_{DSS}$	——	——	1	$\mu A$
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 28 V, V_{GS} = 0 V)$	$I_{DSS}$	——	——	1	$\mu A$
Gate--Source Leakage Current $(V_{GS} = 10 V, V_{DS} = 0 V)$	$I_{GSS}$	——	——	1	$\mu A$
Gate Threshold Voltage $(V_{DS} = 28V, I_D = 400 \mu A)$	$V_{GS(th)}$	——	2.2	——	V
Gate Quiescent Voltage $(V_{DD} = 28 V, I_D = 200 mA, \text{Measured in Functional Test})$	$V_{GS(Q)}$	——	3.1	——	V
Common Source Input Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	$C_{ISS}$		69.2		pF
Common Source Output Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	$C_{OSS}$		28.6		pF
Common Source Feedback Capacitance $(V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz)$	$C_{RSS}$		1.1		pF

**Functional Tests** (In Demo Test Fixture, 50 ohm system)  $V_{DD} = 28 Vdc, I_{DQ} = 350mA, f = 1000 MHz, CW$  Signal Measurements.

Power Gain	$G_p$	——	19	——	dB
Drain Efficiency@P1dB	$\eta_D$	——	60	——	%
1 dB Compression Point	$P_{-1dB}$	——	60	——	W
Input Return Loss	IRL	——	-7	——	dB

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):**  $V_{DD} = 28 Vdc, I_{DQ} = 350 mA, f = 1000 MHz$

VSWR 20:1 at 60W pulse CW Output Power	No Device Degradation
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## Package Outline

Flanged ceramic package; 2 leads

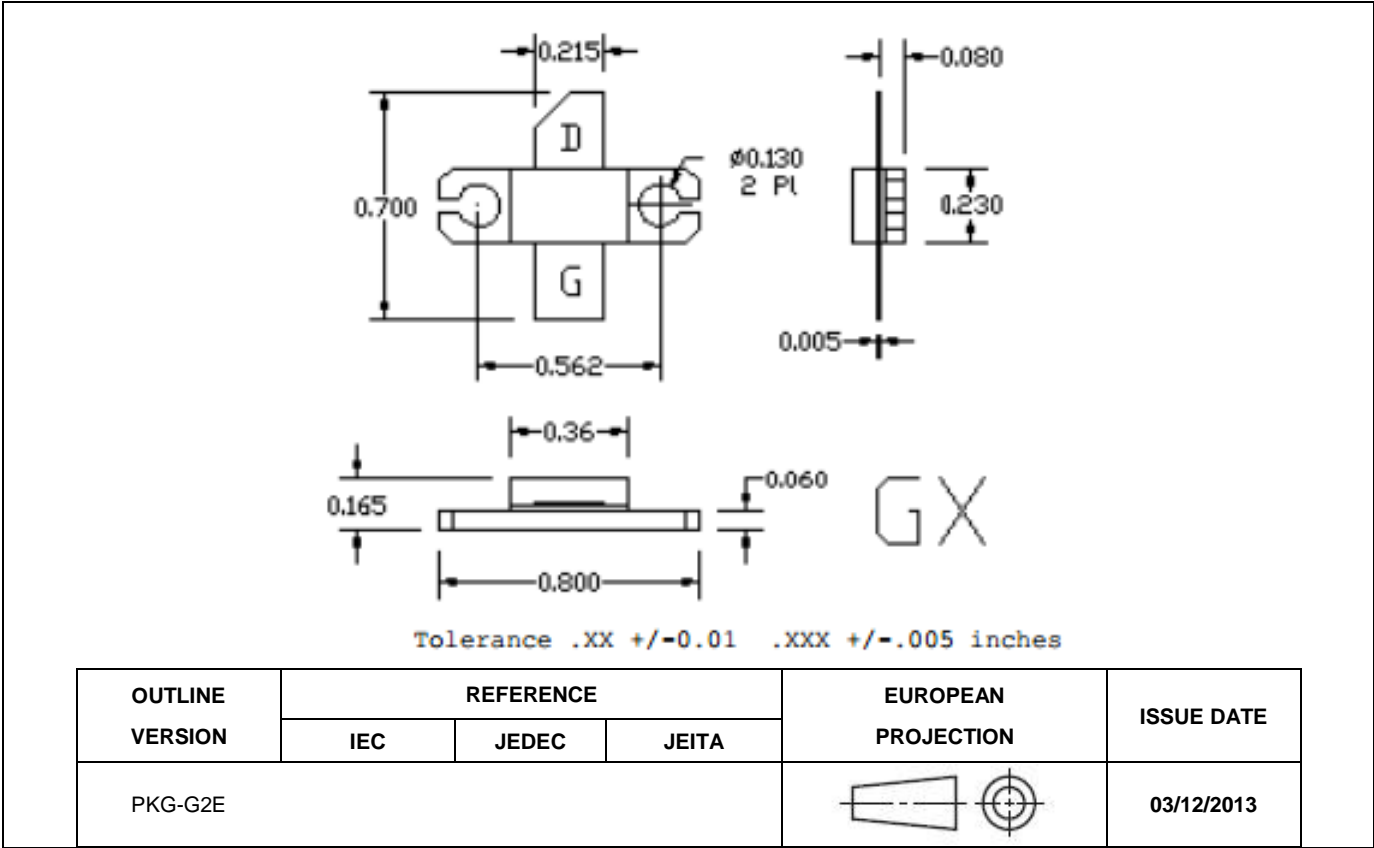


Figure 1. Package Outline PKG-G2E

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2014/2/11	Rev 1.0	Preliminary Datasheet
2016/8/8	Rev 2.0	Preliminary Datasheet
2016/12/27	Rev 2.1	Preliminary Datasheet
		Add Thermal Resistance
2017/2/22	Rev 3.0	Product Datasheet
		Add CV parameter

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