

MU1510C LDMOS TRANSISTOR

Document Number: MU1510C
Preliminary Datasheet V1.0

100W, 28V High Power RF LDMOS FETs

Description

The MU1510C is a 100-watt high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5 GHz.

MU1510C



- Typical Performance (On Innogration fixture with device soldered):

$V_{DD} = 28$ Volts, $I_{DQ} = 100$ mA, CW.

Frequency	Gp (dB)	P_{-1dB} (W)	$\eta_D @ P_{-1}$ (%)
1300 MHz	18	100	65

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DS}	+65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0, I_{DS}=1.0mA$	$V_{(BR)DSS}$	65	70		V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28 V, V_{GS} = 0 V$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10 V, V_{DS} = 0 V$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28V, I_D = 600 \mu A$)	$V_{GS(th)}$	—	1.98	—	V
Gate Quiescent Voltage ($V_{DD} = 28 V, I_D = 100 mA$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.53	—	V
Drain source on state resistance ($V_{DS} = 0.1V, V_{GS} = 10 V$)	$R_{ds(on)}$		100		m Ω
Common Source Input Capacitance ($V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz$)	C_{iss}		91		pF
Common Source Output Capacitance ($V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz$)	C_{oss}		38		pF
Common Source Feedback Capacitance ($V_{GS} = 0V, V_{DS} = 28 V, f = 1 MHz$)	C_{rss}		1.58		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 1300 MHz$, CW Signal Measurements.

Power Gain	G_p	—	18	—	dB
Drain Efficiency@P1dB	η_D	—	65	—	%
1 dB Compression Point	P_{-1dB}	—	100	—	W
Input Return Loss	IRL	—	-7	—	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28 Vdc, I_{DQ} = 100 mA, f = 1300 MHz$

VSWR 10:1 at 100W CW Output Power	No Device Degradation
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Package Outline

Flanged ceramic package; 2 leads

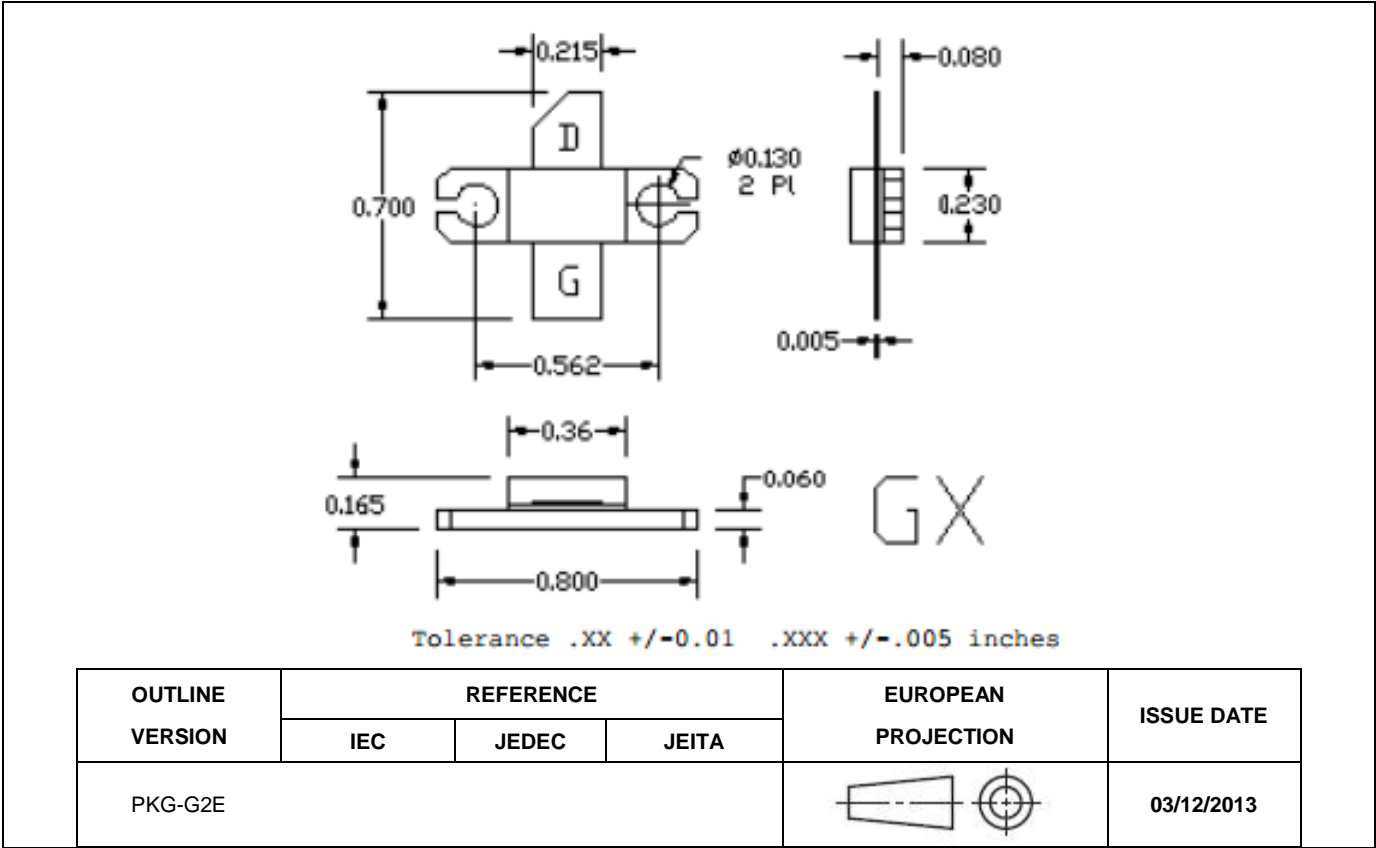


Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/8/2	Rev 1.0	Preliminary Datasheet Creation

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