MUSES100 series

600mA 5.5V Low Noise LDO Regulator For High Quality Audio

FEATURES

- Input Voltage Range (Maximum Rating): 2.5 V to 5.5 V (6.5 V)
- Output Voltage Range: 1.2 V to 5.0 V
- Output Current: 600 mA
- Output Noise Voltage: Typ. 3.0 μVrms (I_{OUT} = 50 mA, C_{NR} = 0.47 μF)
- Ripple Rejection: Typ. 90 dB (f = 1 kHz, 10 kHz) Typ. 80 dB (f = 100 kHz) (C_{NR} = 0.47 μF)
- Dropout Voltage: Typ. 0.15 V (I_{OUT} = 600 mA, V_{SET} = 3.3 V)
- Quiescent Current: Typ. 960 μA
- Operating Temperature Range: -40 ºC to 85 ºC
- Protection Function: Thermal Shutdown, Under Voltage Lockout(UVLO), Over Current Protection
- Film capacitors and Aluminum electrolytic capacitors can be used in.

Application

- Home audio equipment
- Professional audio equipment
- Portable audio equipment

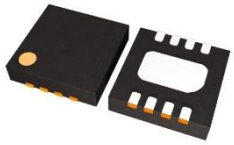
GENERAL DESCRIPTION

The MUSES100 series is a CMOS based 5.5 V, 600 mA low noise low dropout voltage regulator for high quality audio.

This series achieves high-quality sound featured sound quality conscious circuit, materials and packaging technologies.

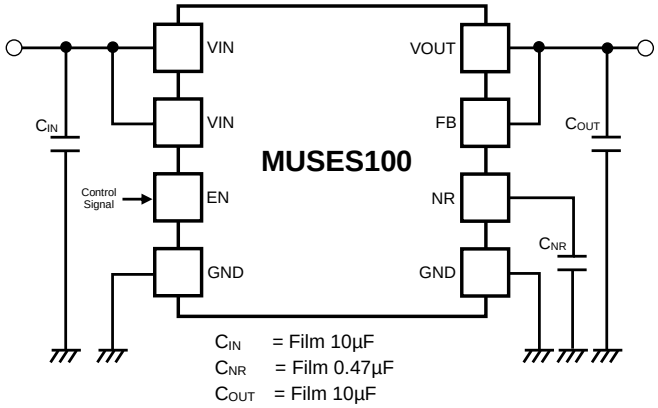
High ripple rejection ratio and low noise features make The MUSES100 series suitable for high-quality audio DAC.

Packages (unit: mm)

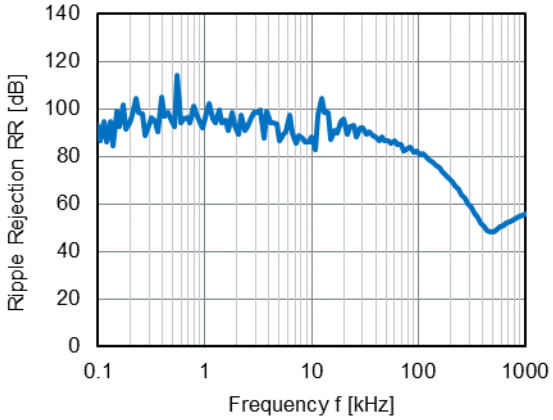


DFN3030-8-GQ
3.0×3.0×0.75mm

Typical Application Circuit



Ripple Rejection Ratio Characteristic



V_{IN} = 4.3 V, Ripple 0.2 Vp-p, V_{SET} = 3.3 V,
I_{OUT} = 100 mA, C_{NR} = 0.47 μF、C_{OUT} = 10 μF

■ PRODUCT NAME INFORMATION

MUSES100 aa bb c dd e

Description of configuration

Composition	Item	Description
aa	Package Code	Indicates the package. GQ: DFN3030-8-GQ
bb	Output Voltage	Output voltage (V_{SET}). The lineup ranges from 1.2 V (12) to 5.0 V (50).
c	Version	Only “A”
dd	Packing	Insert Direction. Refer to the packing specifications.
e	Grade	Indicates the quality grade. S: Consumer

Grade

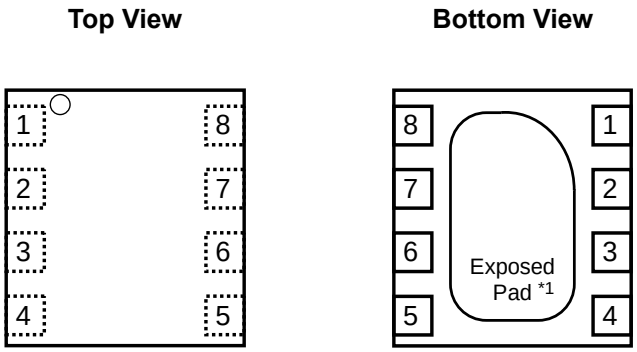
e	Applications	Operating Temperature Range	Test Temperature
S	Consumer	−40 °C to 85 °C	25 °C

■ ORDER INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN-FREE	PLATING COMPOSITION	WEIGHT (mg)	QUANTITY (pcs/reel)
MUSES100GQxxAxxS	DFN3030-8-GQ	✓	✓	Sn2Bi	17mg	1500

Refer to “MARKING SPECIFICATION” for details.
Please contact us if you require a voltage other than the existing fixed-output product.

■ PIN DESCRIPTIONS



DFN3030-8-GQ Pin Configuration

Pin No.	Pin Name	I/O	Description
1, 2	VIN	Power	Power Supply Input Pin Connect the input capacitor (C_{IN}) between the VIN pin and GND. The Pin #1 and #2 must be shorted.
3	EN	I	Enable Pin Input “Low” to this pin shuts down the IC. Input "High" to this pin enables the IC. This pin is pulled down with an internal constant current circuit.
4, 5	GND	-	Ground Pin
6	NR	-	Noise Reduction Capacitor Connection Pin Connect a capacitor between the NR pin and GND.
7	FB	I	Feedback Input Pin Connect to the VOUT pin.
8	VOUT	O	Output Pin Connect the output capacitor (C_{OUT}) between the VOUT pin and GND.

*1 The tab on the bottom of the package is the silicon substrate level. It is recommended to mount on the board and electrically floated from audio quality perspective.

■ ABSOLUTE MAXIMUM RATINGS

	Symbol	Ratings	Unit
VIN pin Voltage	V_{IN}	−0.3 to 6.5	V
VOUT pin Voltage	V_{OUT}	−0.3 to V_{IN} + 0.3 ≤ 6.5	V
EN pin Voltage	V_{EN}	−0.3 to 6.5	V
NR pin Voltage	V_{NR}	−0.3 to 6.5	V
FB pin Voltage	V_{FB}	−0.3 to V_{OUT} + 0.3 ≤ 6.5	V
Junction Temperature Range[*1]	T_j	−40 to 125	°C
Storage Temperature Range	T_{stg}	−50 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause permanent damage and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

[*1] Calculate the power consumption of the IC from the operating conditions and calculate the junction temperature with the thermal resistance.
Please refer to "THERMAL CHARACTERISTICS" below for thermal resistance under our measured substrate conditions.

■ THERMAL CHARACTERISTICS

Parameter	Measurement Result
Thermal Resistance (θja)	27 °C/W
Thermal Characterization Parameter (ψjt)	8 °C/W

θja: Junction-to-Ambient Thermal Resistance
ψjt: Junction-to-Top Thermal Characterization Parameter

■ ELECTROSTATIC DISCHARGE RATINGS

	Conditions	Protection Voltage
HBM	C = 100 pF, R = 1.5 kΩ	±2000 V
CDM		±1000 V

ELECTROSTATIC DISCHARGE RATINGS

The electrostatic discharge test is done based on JEDEC JS001, JS002.
In the HBM method, ESD is applied using the power supply pin and the GND pin as reference pins.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Ratings	Unit
Input Voltage	V_{IN}	2.5 to 5.5	V
EN Pin Input Voltage	V_{EN}	0 to 5.5	V
Output Current	I_{OUT}	0 to 600	mA
Operating Temperature Range	T_a	−40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

■ ELECTRICAL CHARACTERISTICS

V_{IN} = V_{SET} + 1 V (V_{IN} = 2.5 V for V_{SET} < 1.5 V, V_{IN} = 5.5 V for V_{SET} > 4.5 V), I_{OUT} = 1 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF and C_{NR} = 10 nF unless otherwise specified.
For items without temperature conditions, TYP values are at T_a = 25 °C and MIN/MAX values are applied to all the temperature range of −40 °C ≤ T_a ≤ 85 °C.

MUSES100

Parameter	Symbol	Conditions		MIN	TYP	MAX	Unit
Output Voltage Accuracy	V_{OUT}	T_a = 25 ºC V_{IN} = V_{SET} + 0.5 V to 5.5 V *1	1.2 V ≤ V_{SET} < 3.0 V	-1.5	-	+1.5	%
			3.0 V ≤ V_{SET} ≤ 5.0 V	-1.0	-	+1.0	%
		-40 ºC ≤ T_a ≤ 85 ºC V_{IN} = V_{SET} + 0.5 V to 5.5 V *1	1.2 V ≤ V_{SET} < 3.0 V	-2.0	-	+1.8	%
			3.0 V ≤ V_{SET} ≤ 5.0 V	-1.5	-	+1.3	%
Quiescent Current	I_Q	V_{EN} = V_{IN}, I_{OUT} = 0 A		-	960	1210	µA
Shutdown Current	I_{SD}	V_{IN} = 5.5 V, V_{EN} = 0 V, Ta = 25 ºC		-	0.05	0.30	µA
Line Regulation	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = V_{SET} + 0.5 V to 5.5 V *1 I_{OUT} = 1 mA	1.2 V ≤ V_{SET} < 3.0 V	-	0.08	-	%/V
			3.0 V ≤ V_{SET} ≤ 5.0 V	-	0.04	-	%/V
Load Regulation	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 600 mA		0.01	-	0.01	V
Dropout Voltage *2	V_{DO}	I_{OUT} = 600 mA	1.2 V ≤ V_{SET} < 2.2 V	- *3			V
			2.2 V ≤ V_{SET} < 2.8 V	-	0.18 *4	0.26 *4	V
			2.8 V ≤ V_{SET} < 3.3 V	-	0.15	0.21	V
			3.3 V ≤ V_{SET} ≤ 5.0 V	-	0.14	0.20	V
Output Current Limit	I_{LIM}	V_{OUT} = V_{SET} × 90 %		600	850	-	mA
Short-circuit Current	I_{SC}	V_{OUT} = 0 V		110	150	185	mA
Current Limit at Start-up	$I_{LIMRISE}$	V_{OUT} = 0 V		110	150	185	mA
Discharge FET On-resistance	R_{ONDIS}	V_{IN} = 5 V, V_{EN} = 0 V, V_{OUT} = 0.1 V		-	20	-	Ω
EN pin current	I_{EN}	V_{IN} = V_{EN} = 5.5 V		-	0.37	0.60	µA
EN pin High Input Voltage(enable device)	V_{ENH}			1.0	-	5.5	V
EN pin Low Input Voltage(disable device)	V_{ENL}			0	-	0.4	V
UVLO Detection Voltage *5	$V_{UVLODET}$	V_{IN} = Falling		2.15	-	-	V
UVLO Release Voltage *5	$V_{UVLOREL}$	V_{IN} = Rising		-	-	2.4	V
Thermal Shutdown Detection Temperature	T_{SDDET}	T_j = Rising		-	165	-	ºC
Thermal Shutdown Release Temperature	T_{SDREL}	T_j = Falling		-	135	-	ºC
Ripple Rejection	RR	Ripple 0.2 Vp-p, I_{OUT} = 100 mA, C_{NR} = 0.47 µF	f = 1 kHz	-	90	-	dB
			f = 10 kHz	-	90	-	dB
			f = 100 kHz	-	80	-	dB
Output Noise Voltage	V_{NOISE}	I_{OUT} = 50 mA, C_{NR} = 0.47 µF f = 10 Hz to 100 kHz		-	3.0	-	µVrms

All test parameters listed in Electrical Characteristics are tested under the condition of pulse load condition (T_j ≈ T_a = 25°C) expect for Ripple Rejection and Output Noise Voltage.

*1 1.2 V ≤ V_{SET} < 2.0 V: 2.5 V ≤ V_{IN} ≤ 5.5 V
4.7 V ≤ V_{SET} ≤ 5.0 V: V_{SET} + 0.2 V ≤ V_{IN} ≤ 5.5 V

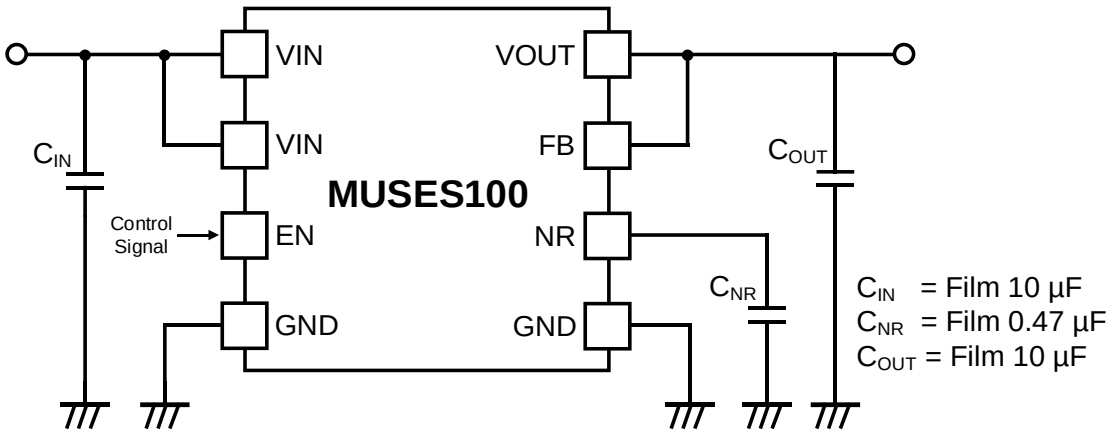
*2 Dropout Voltage (V_{DO}) is specified as the minimum voltage difference between Input Voltage (V_{IN}) and Output Voltage (V_{OUT}) required to obtain 95% at specified load current.

*3 Make sure to Input Voltage (V_{IN}) under the recommended condition (2.5 V or more).

*4 If V_{SET} + V_{DO} < 2.5 V, make sure to Input Voltage (V_{IN}) under the recommended condition (2.5 V or more).

*5 Due to the circuit configuration, $V_{UVLODET}$ ≥ $V_{UVLOREL}$ does not hold. The hysteresis is Typ. 0.08 V.

■ TYPICAL APPLICATION CIRCUIT



MUSES100 Typical Application Circuit

EXTERNAL COMPONENTS INFORMATION

This device requires three external capacitors: C_{IN}, C_{OUT} and C_{NR}. Select suitable parts to refer the following cautions.

Input Capacitor (C_{IN})

Connect a 10 µF or more the input capacitor (C_{IN}) between the VIN pin and the GND pin with shortest-distance wiring. We recommend using a Film capacitor or an Aluminum electrolytic capacitor with superior DC bias characteristics. Ceramic capacitors are not recommended due to the piezoelectric effect may induce noise.

Output Capacitor (C_{OUT})

Phase compensation with the Output Capacitor (C_{OUT}) is provided to secure stable operation even when the load current is varied. Therefore, connect a Film capacitor or an Aluminum electrolytic capacitor of 10µF or more and 2200µF or less between the VOUT pin and the GND pin with shortest-distance wiring.
If prioritize sound quality, recommend using a 100µF or more and superior DC bias characteristic Aluminum electrolytic capacitor. Besides, select for the output capacitor to ensure the following effective capacitance in consideration of the dependence of temperature, DC bias and package size.

Set Output Voltage vs. C_{OUT} Effective Capacitance

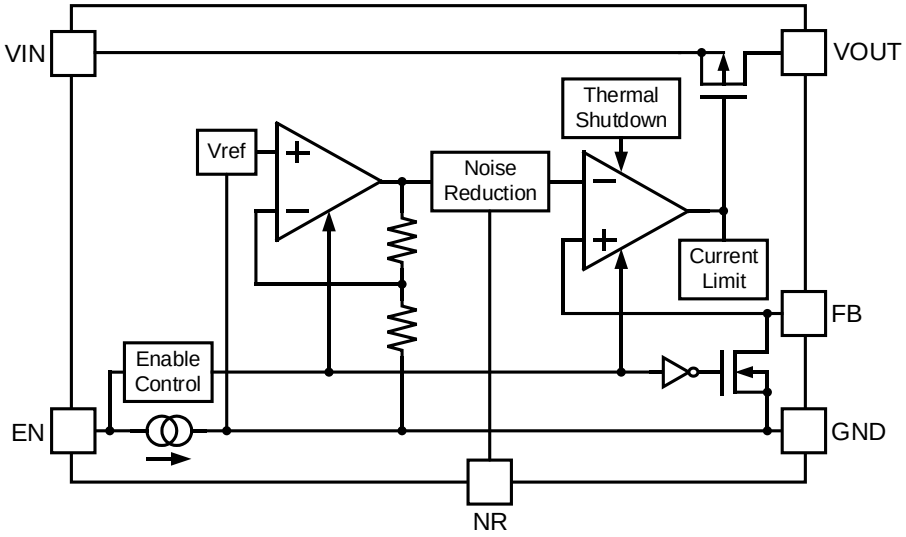
Set Output Voltage (V_{SET})	C_{OUT} Effective Capacitance	
	MIN	TYP
1.2 V ≤ V_{SET} ≤ 5.0 V	7 µF	10 µF

Furthermore, this device is designed for Film capacitor or Aluminum electrolytic capacitor. Do not use Ceramic capacitors to avoid unstable operation.

Noise Reduction Capacitor (C_{NR})

Connect the Noise Reduction Capacitor (C_{NR}) of 10 nF or more and 1 µF or less between the NR pin and the GND pins with shortest-distance wiring.
To secure Ripple Rejection Ratio and/or Output Noise Voltage that show on "ELECTRICAL CHARACTERISTICS", we recommend a Film Capacitor of 0.47µF or more and superior DC bias characteristic. Furthermore, not recommend Ceramic capacitors due to the piezoelectric effect may induce noise.

■ BLOCK DIAGRAM



MUSES100GQxxA Block Diagram

■ THEORY OF OPERATION

● Enable Function

Forcing above designated "High" voltage to the EN pin, the IC becomes active. Forcing below designated "Low" voltage to the EN pin shuts down the IC. The EN pin is pulled down with a constant current of Typ.0.37 µA inside the IC.
If control by the EN pin is not possible or is not required, connect the EN pin to the VIN pin, etc., so that "High" is input at start-up. If the EN pin is connected to the VIN pin, the normal effect of the built-in discharge FET cannot be expected.
Even if voltage is applied to the EN pin before the VIN pin, the IC will not fail.

● Discharge Function

This function turns on the FET connected between the VOUT pin and the GND pin to discharge the charge stored in the output capacitor (C_{OUT}) and quickly reduce the output voltage to near 0 V. This function is enabled when the EN pin is "Low" or when thermal shutdown is detected.
The FET on-resistance is Typ. 20 Ω (V_{IN} = 5.0 V). This function is effective when the input voltage (V_{IN}) is within the recommended operating conditions.
Please note that when the input voltage (V_{IN}) and the EN pin input voltage are used in common, the C_{OUT} charge cannot be discharged sufficiently when the input voltage (V_{IN}) drops.

● Thermal Shutdown

When the junction temperature (T_j) exceeds the thermal shutdown detection temperature (Typ.165 °C), this IC cuts off the output transistor and suppresses the self-heating. When the junction temperature falls below the thermal shutdown release temperature (Typ. 135 °C), this IC will restart with the Inrush Current Suppression Function.

● Under Voltage Lockout (UVLO) Circuit

The UVLO function is an auxiliary function that stops the operation of the IC when the input voltage is low, and the IC cannot operate normally. The VOUT pin is pulled down by the built-in discharge FET when this function works. To restart the operation, the input voltage (V_{IN}) must be higher than the recommended operating conditions (2.5 V).

● Inrush Current Suppression Function

The Inrush Current Suppression Function is that limits the inrush current at start-up (I_{RUSH}), which is the sum of the charge current (I_{CHG}) to the output capacitor (C_{OUT}) and the load current (I_{LOAD}), with the limit current value at start-up ($I_{LIMRISE}$, Typ. 150 mA).
Under the condition such as the output capacitor (C_{OUT}) or load current (I_{LOAD}) makes the start-up inrush current (I_{RUSH}) reaches the Start-up Inrush Current Limit ($I_{LIMRISE}$, Typ. 150 mA), it rises at a slower slope that determined by C_{OUT} and I_{LOAD}.
The rise time (t_{ON}) by the inrush current limiting function can be calculated by the following formula.

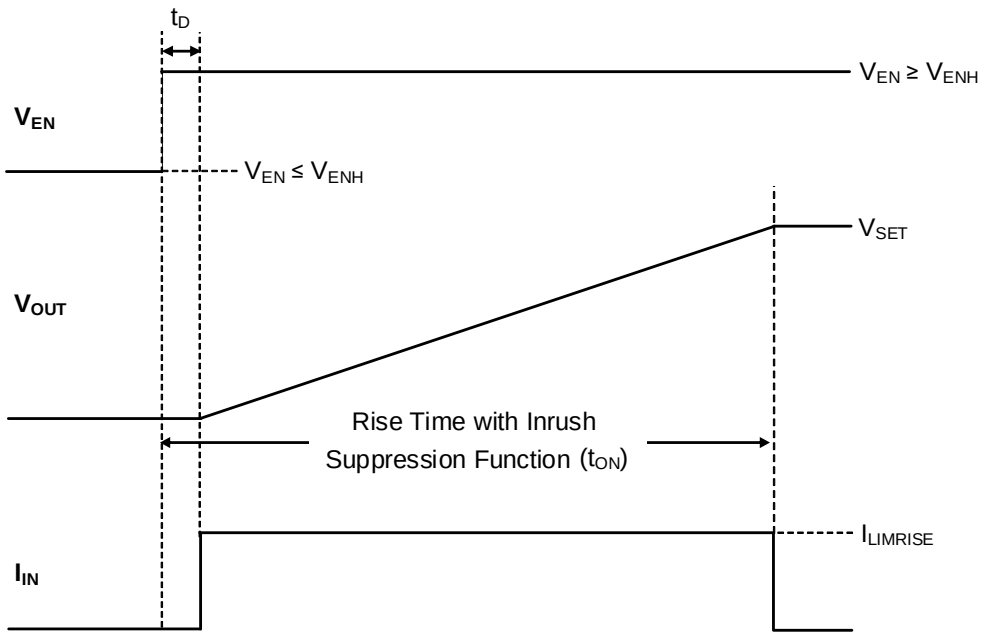
$$t_{ON} = t_D + C_{OUT} \times V_{SET} / (I_{LIMRISE} - I_{LOAD})$$

t_D:	Output Delay Time	Typ. 35 µs
C_{OUT}:	Effective Capacitance of Output Capacitor	
V_{SET}:	Set Output Voltage	
$I_{LIMRISE}$:	Start-up Inrush Current Limit	Typ. 150 mA
I_{LOAD}:	Load Current	

The Start-up Inrush Current Limit ($I_{LIMRISE}$) is effective until the output voltage (V_{OUT}) reaches the set output voltage (V_{SET}). It is then protected against overcurrent by the output current limit (I_{LIM}) and the short circuit current (I_{SC}).

To enable the inrush current limit function, start by inputting "High" to the EN pin after applying the recommended operating conditions (2.5 V or more) as the input voltage (V_{IN}).
If the input voltage (V_{IN}) does not meet the recommended operating conditions and the EN pin is set to "High", the IC may start up without inrush current limit function.
If the load current (I_{LOAD}) exceeds the Start-up Inrush Current Limit ($I_{LIMRISE}$) during start-up, the output voltage (V_{OUT}) will not reach the set output voltage (V_{SET}).

The UVLO function and the thermal shutdown function are valid even while the output voltage is starting. These protective functions may operate when starting with a load current or when a large output capacitor (C_{OUT}) is connected. In such cases, adjust the output capacitor (C_{OUT}) and start-up timing to suppress inrush current and heat generation.



Timing Chart: Start-up inrush current is larger than the start-up inrush current limit

■ THERMAL CHARACTERISTICS (DFN3030-8-GQ)

Thermal characteristics depend on the mounting conditions.
The following measurement conditions are based on JEDEC STD. 51.

Measurement Result

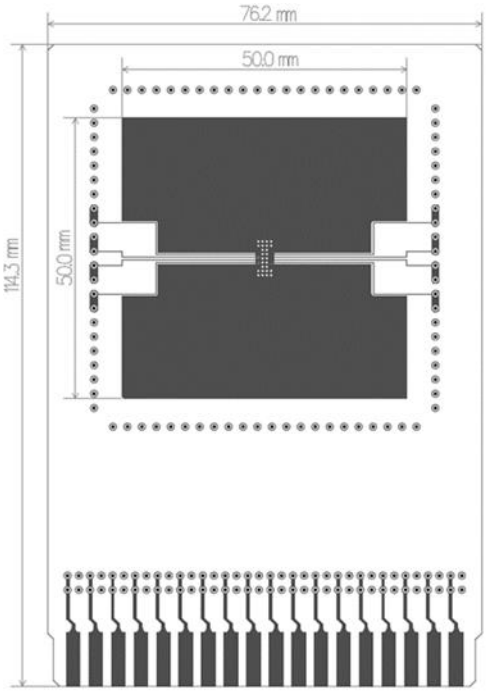
Item	Measurement Result
Thermal Resistance (θja)	27℃/W
Thermal Characterization Parameter (ψjt)	8℃/W

θja: Junction-to-Ambient Thermal Resistance

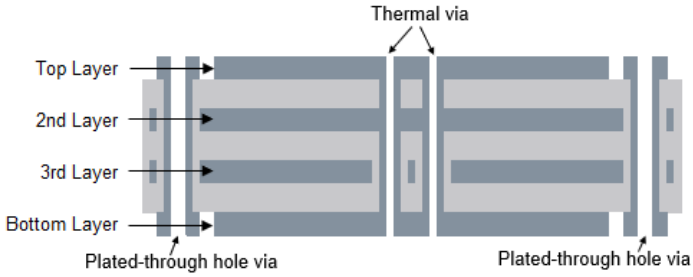
Ψjt: Junction-to-Top Thermal Characterization Parameter

Measurement Conditions

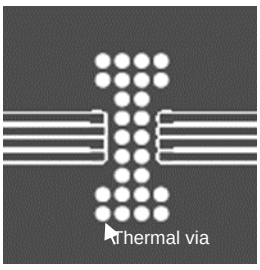
Item		Specification
Measurement Condition		Mounting on Board (Still Air)
Board material		FR-4
Board size		76.2 mm × 114.3 mm × t 1.6 mm
Copper foil layer	1	50 mm × 50 mm (coverage rate 95%), t 0.070 mm
	2	74.2 mm × 74.2 mm (coverage rate 100%), t 0.035 mm
	3	74.2 mm × 74.2 mm (coverage rate 100%), t 0.035 mm
	4	50 mm × 50 mm (coverage rate 100%), t 0.070 mm
Thermal vias		ϕ 0.25 mm × 26 pcs



Measurement Board Pattern



Cross section view of layers and vias



Enlarged view of IC mounting area

● CALCULATION METHOD OF JUNCTION TEMPERATURE

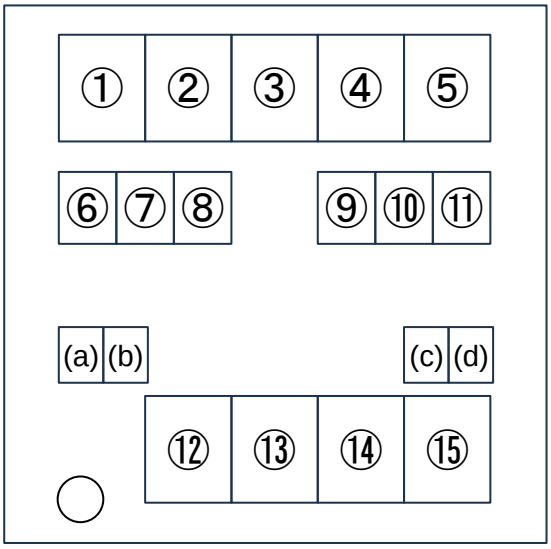
The junction temperature (T_j) can be calculated from the following formula.

$T_j = T_a + \theta ja \times P$
$T_j = Tc\ (top) + \psi jt \times P$

T_a: Ambient temperature
Tc (top): Package mark side center temperature
P (Power consumption under user's conditions): $(V_{IN} - V_{OUT}) \times I_{OUT}$

■ MARKING SPECIFICATION

①②③④⑤⑥⑦⑧: Product Code ⋯ **Refer to the following table**
⑨⑩: Output voltage version
⑪: Function version
⑫⑬⑭⑮: Lot Number ･･･Alphanumeric Serial Number
(a)(b)(c)(d): Internal control number



DFN3030-8-GQ Marking

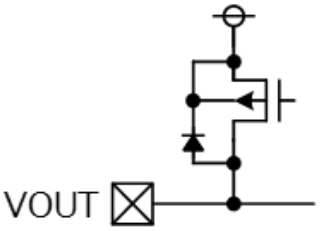
NOTICE
There can be variation in the marking when different AOI (Automated Optical Inspection) equipment is used. In the case of recognizing the marking characteristic with AOI, please contact our sales or distributor before attempting to use AOI.

MUSES100 Marking Table

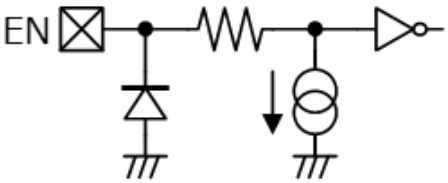
PRODUCT NAME	①②③④⑤⑥⑦⑧⑨⑩⑪
MUSES100GQ12AddS	M U S E S 1 0 0 1 2 A
MUSES100GQ15AddS	M U S E S 1 0 0 1 5 A
MUSES100GQ18AddS	M U S E S 1 0 0 1 8 A
MUSES100GQ33AddS	M U S E S 1 0 0 3 3 A
MUSES100GQ50AddS	M U S E S 1 0 0 5 0 A

■ APPLICATION NOTES

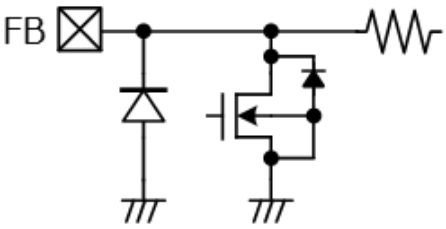
● Internal Equivalent Circuit Diagram of Pin



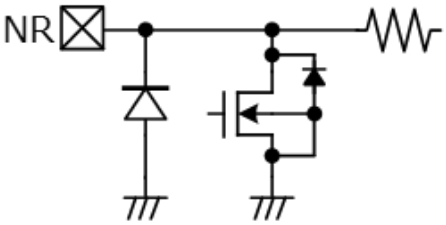
The VOUT pin



The EN pin

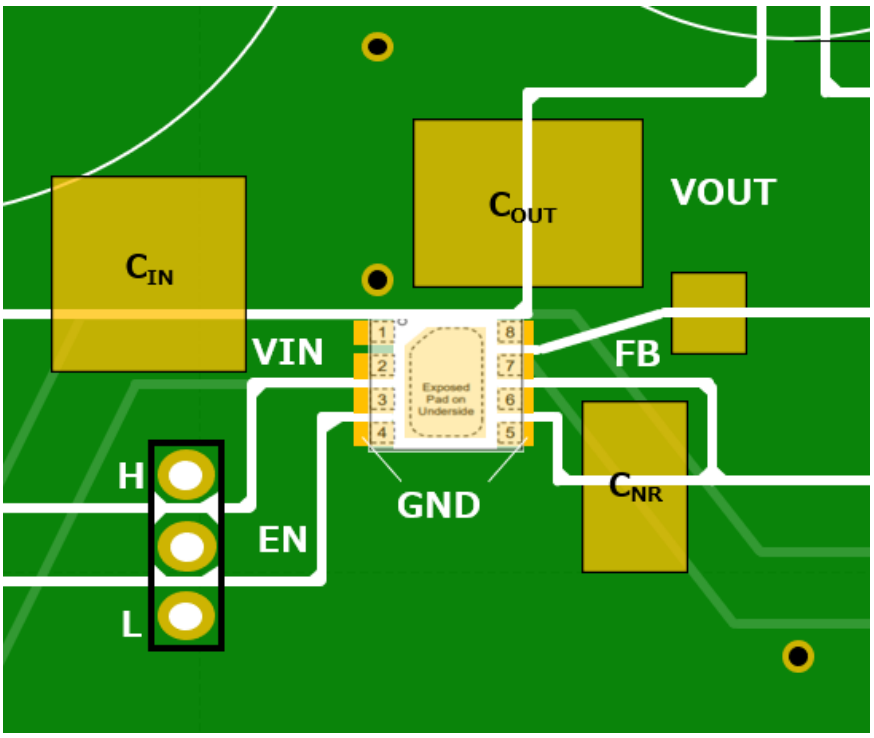


The FB pin



The NR pin

● **Evaluation Board / PCB Layout**



■ TYPICAL CHARACTERISTICS

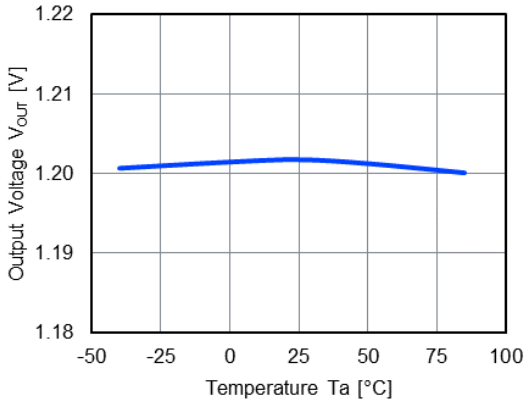
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

Unless otherwise specified, Ta = 25 °C, C_{IN} = 10 µF, C_{OUT} = 10 µF, C_{NR} = 470 nF

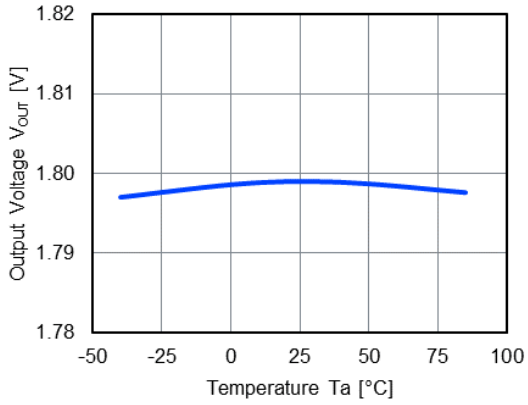
1) Output Voltage vs Temperature

V_{IN} = V_{SET} + 1 V (Min = 2.5 V, Max = 5.5 V), I_{OUT} = 1 mA

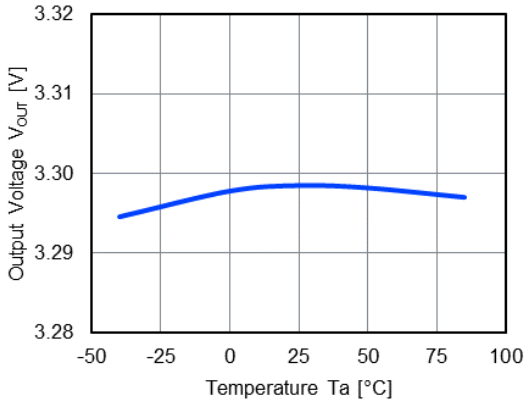
V_{SET} = 1.2 V



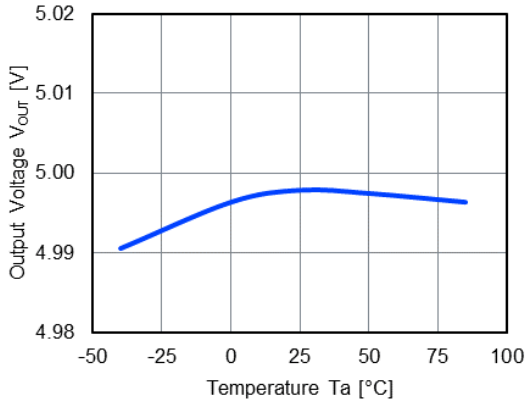
V_{SET} = 1.8 V



V_{SET} = 3.3 V



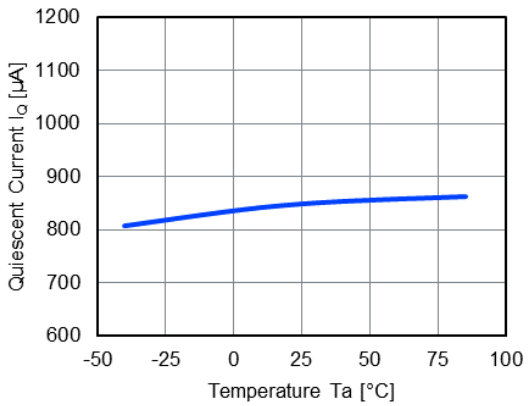
V_{SET} = 5.0 V



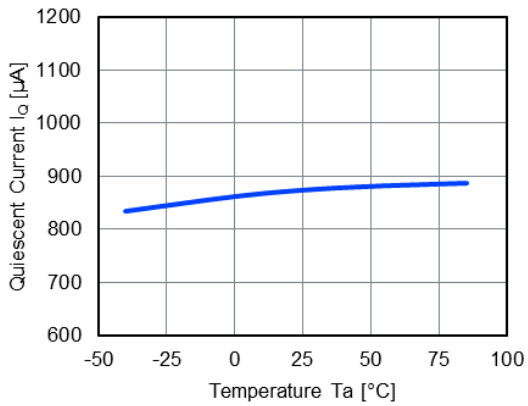
2) Quiescent Current vs Temperature

V_{IN} = V_{SET} + 1 V (Min = 2.5 V, Max = 5.5 V), C_{IN} = none

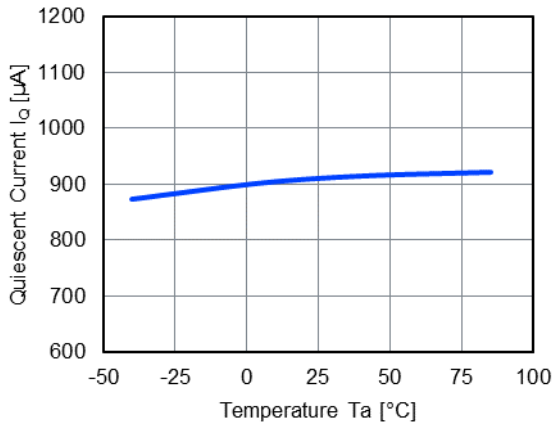
V_{SET} = 1.2 V



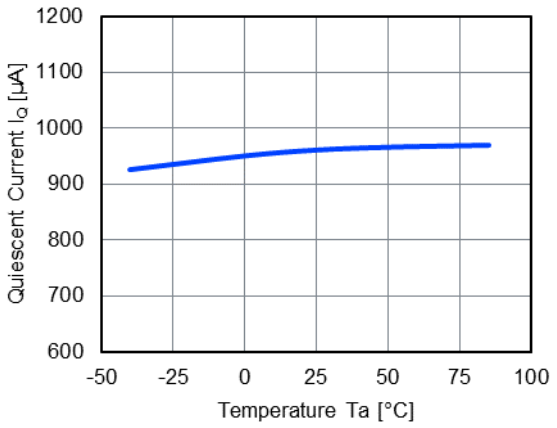
V_{SET} = 1.8 V



V_{SET} = 3.3 V



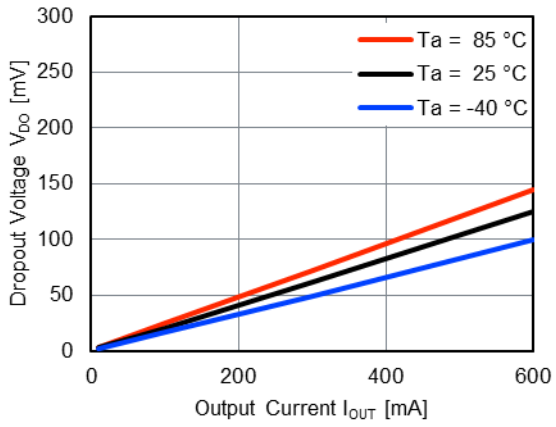
V_{SET} = 5.0 V



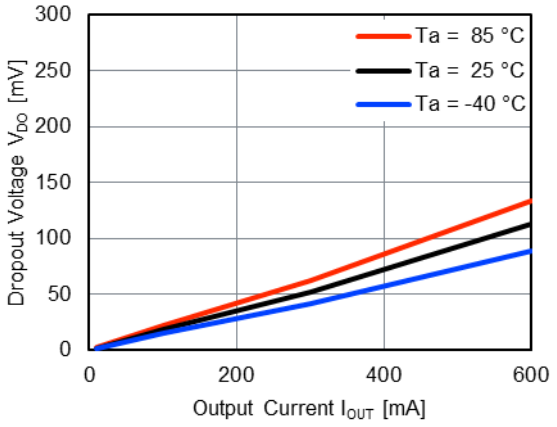
3) Dropout Voltage vs Output Current

V_{IN} = V_{SET} + 1 V (Min = 2.5 V, Max = 5.5 V)

V_{SET} = 3.3 V

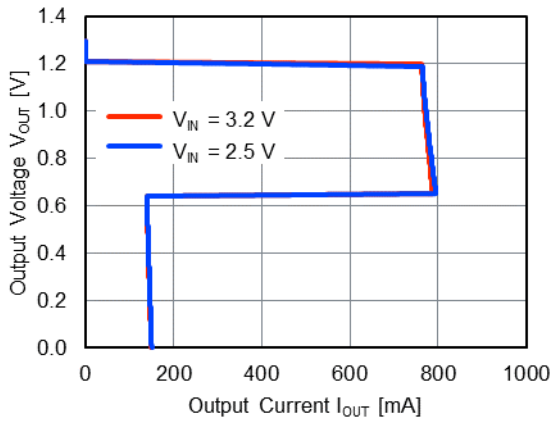


V_{SET} = 5.0 V

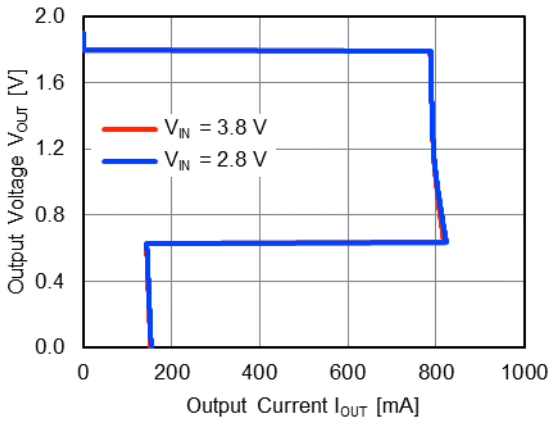


4) Output Voltage vs Output Current

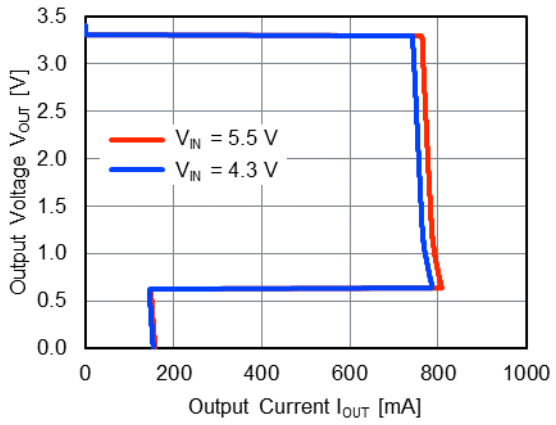
V_{SET} = 1.2 V



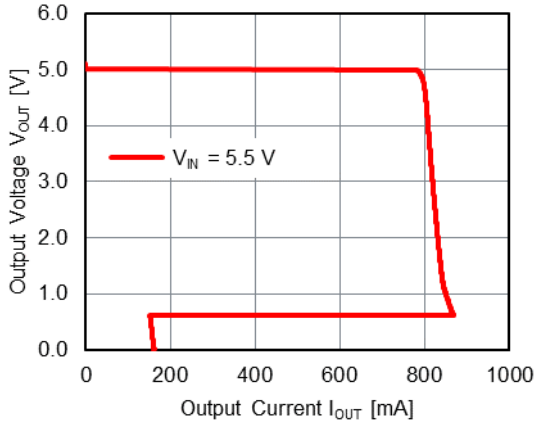
V_{SET} = 1.8 V



V_{SET} = 3.3 V

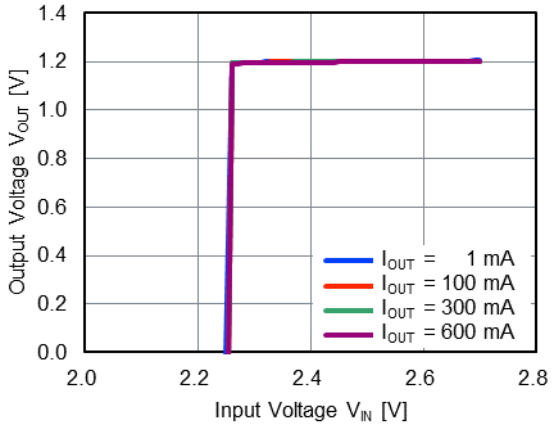


V_{SET} = 5.0 V

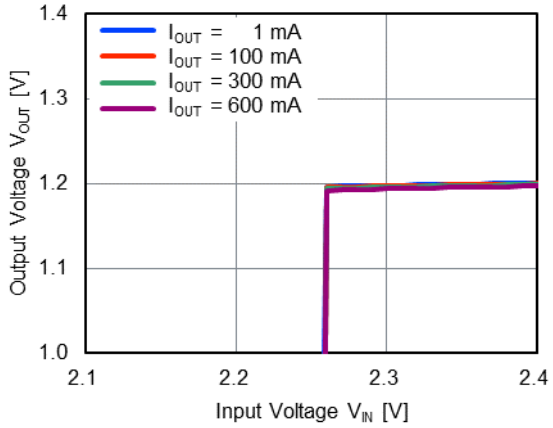


5) Output Voltage vs Input Voltage

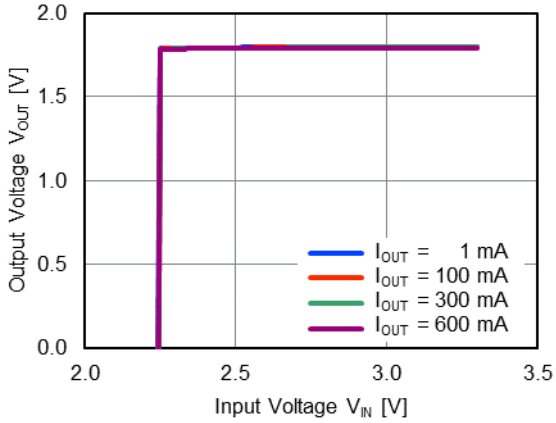
V_{SET} = 1.2 V (V_{IN} = 2.7 V to 2.0 V)



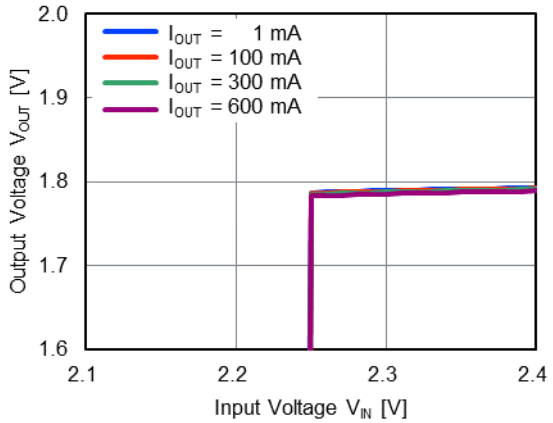
V_{SET} = 1.2 V (V_{IN} = 2.4 V to 2.1 V)



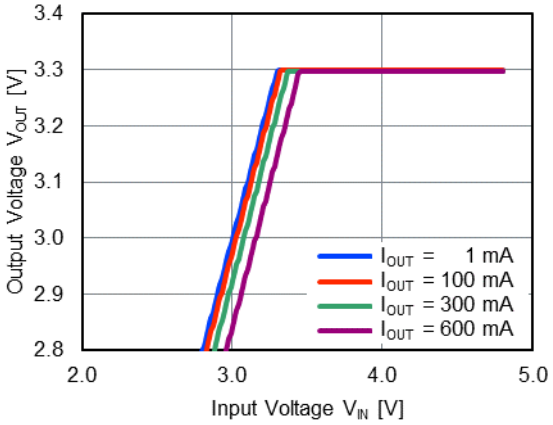
V_{SET} = 1.8 V (V_{IN} = 3.3 V to 2.0 V)



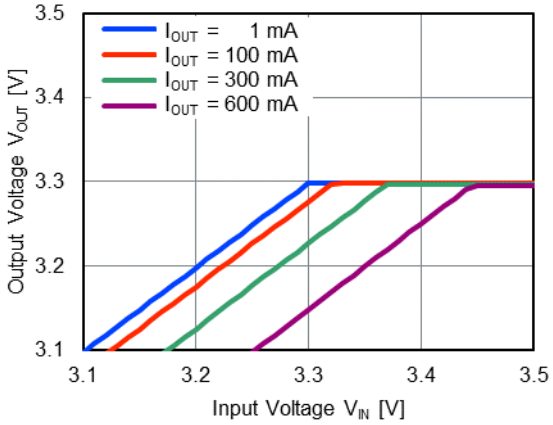
V_{SET} = 1.8 V (V_{IN} = 2.4 V to 2.1 V)



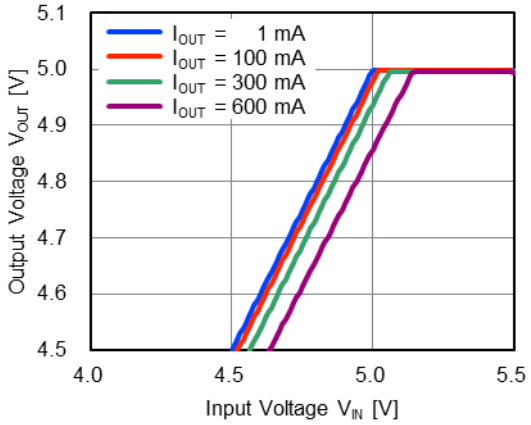
V_{SET} = 3.3 V (V_{IN} = 4.8 V to 2.0 V)



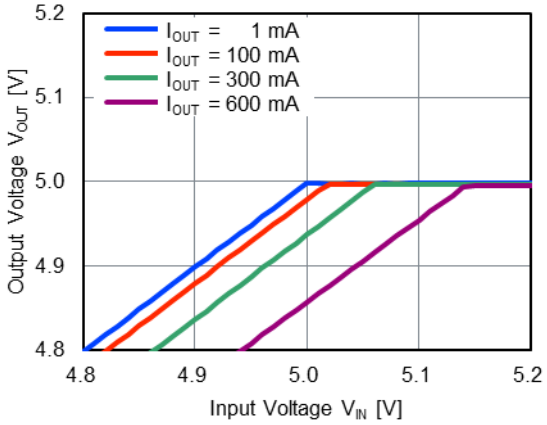
V_{SET} = 3.3 V (V_{IN} = 3.5 V to 3.1 V)



V_{SET} = 5.0 V (V_{IN} = 5.5 V to 4.0 V)



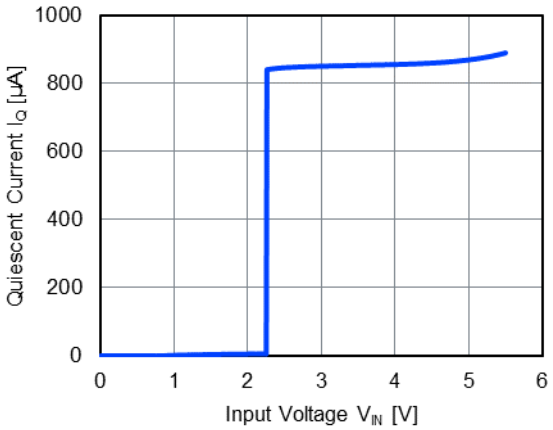
V_{SET} = 5.0 V (V_{IN} = 5.2 V to 4.8 V)



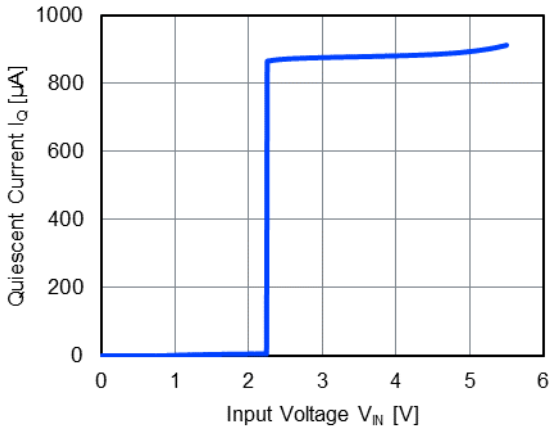
6) Quiescent Current vs Input Voltage

V_{IN} = 5.5 V to 0 V, C_{IN} = none

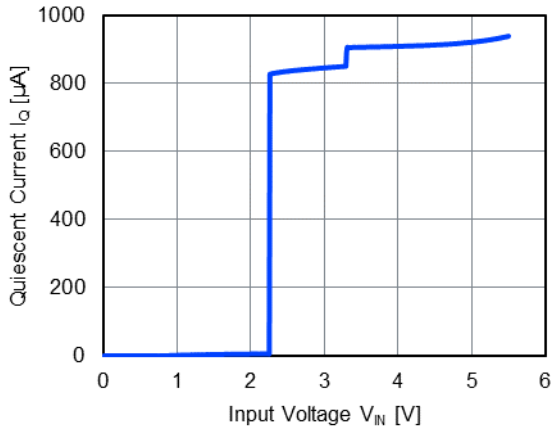
V_{SET} = 1.2 V



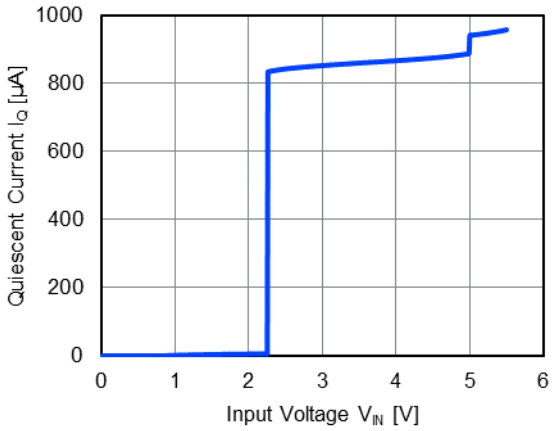
V_{SET} = 1.8 V



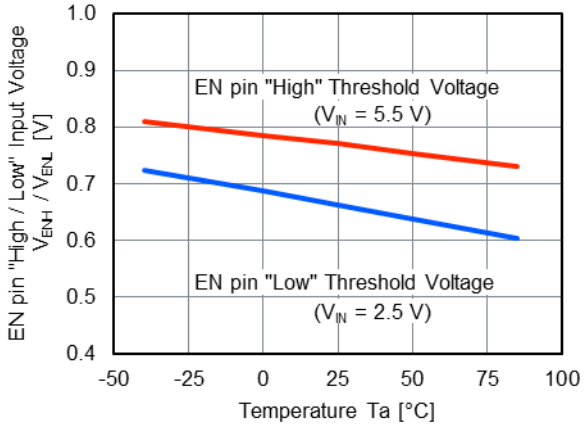
V_{SET} = 3.3 V



V_{SET} = 5.0 V

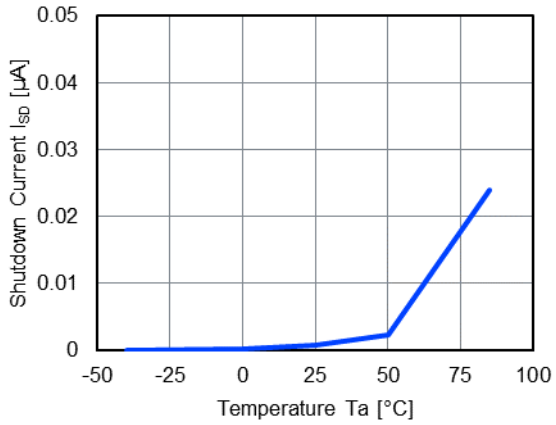


7) EN "High / Low" Input Voltage vs Temperature

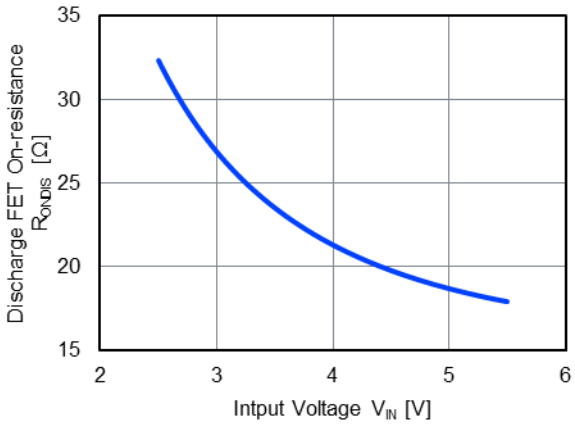


8) Shutdown Current vs Temperature

V_{SET} = 1.2 V, V_{IN} = 5.5 V, C_{IN} = none



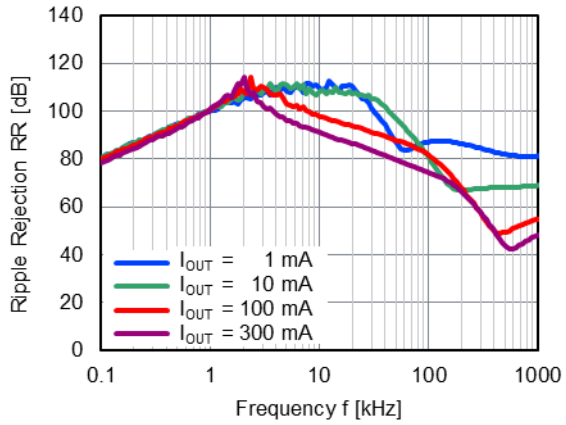
9) Discharge FET On-resistance vs Input Voltage



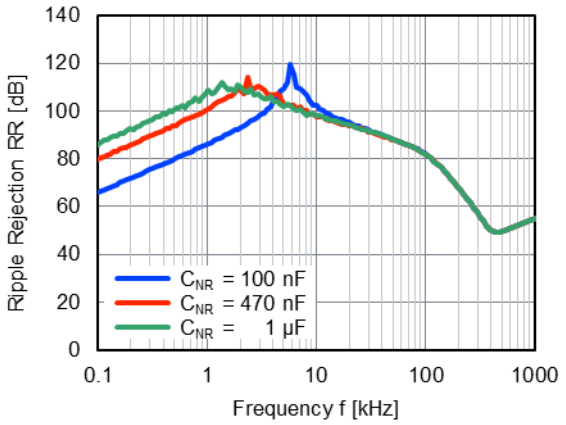
10) Ripple Rejection vs Frequency

V_{SET} = 1.2 V, V_{IN} = 2.5 V, Ripple 0.2 V_{P-P}, C_{IN} = none, C_{OUT} = 10 µF

C_{NR} = 470 nF

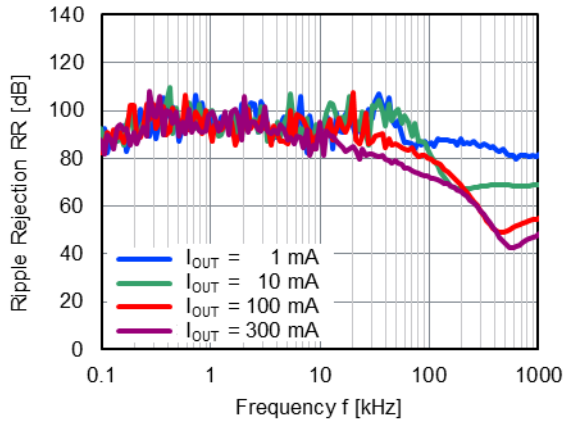


I_{OUT} = 100 mA

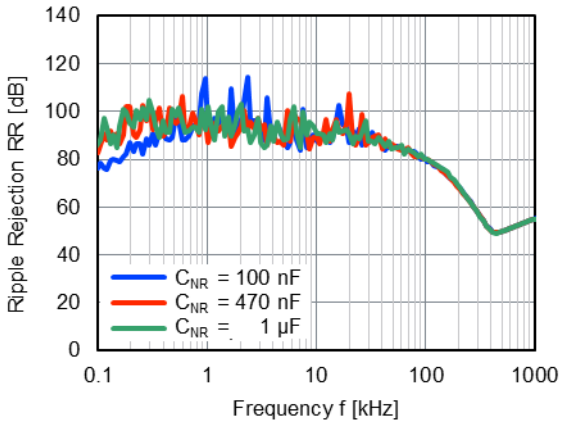


V_{SET} = 1.8 V, V_{IN} = 2.8 V, Ripple 0.2 V_{P-P}, C_{IN} = none, C_{OUT} = 10 µF

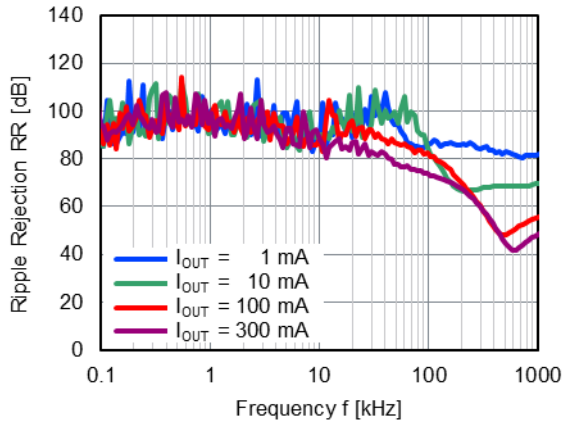
C_{NR} = 470 nF



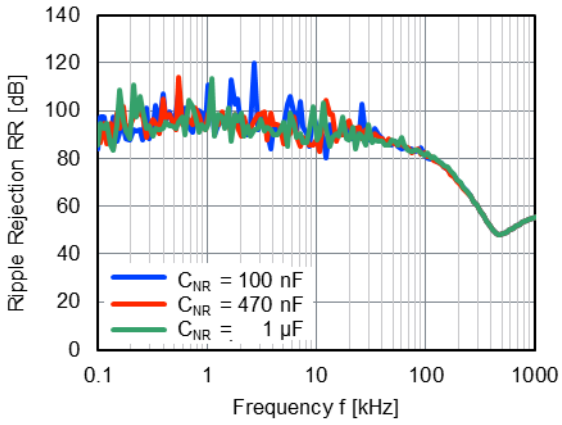
I_{OUT} = 100 mA



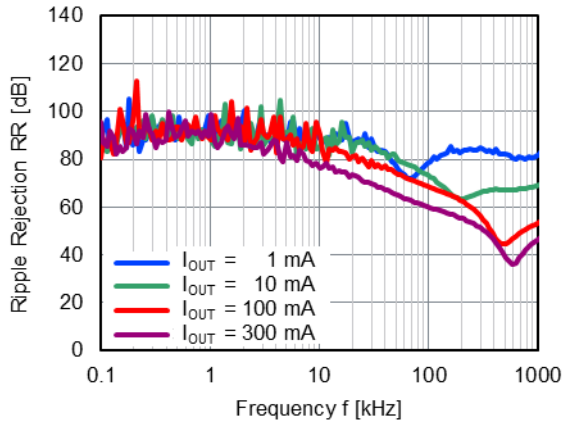
V_{SET} = 3.3 V, V_{IN} = 4.3 V, Ripple 0.2 V_{P-P}, C_{IN} = none, C_{OUT} = 10 µF
C_{NR} = 470 nF



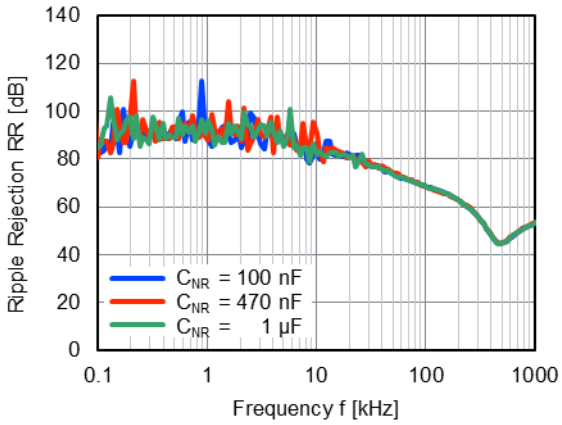
I_{OUT} = 100 mA



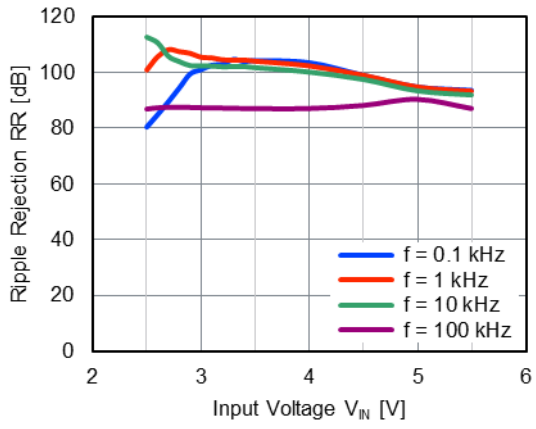
V_{SET} = 5.0 V, V_{IN} = 5.5 V, Ripple 0.2 V_{P-P}, C_{IN} = none, C_{OUT} = 10 µF
C_{NR} = 470 nF



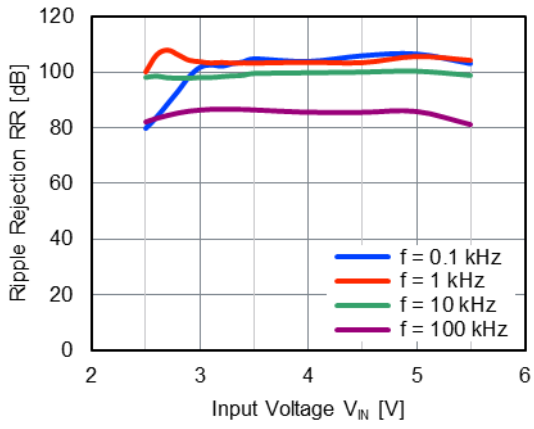
I_{OUT} = 100 mA



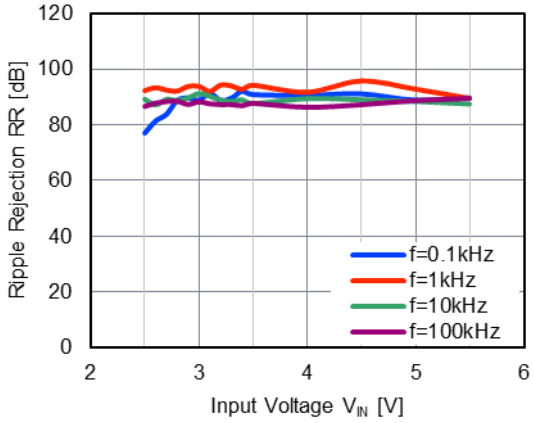
11) Ripple Rejection vs Input Voltage
Ripple 0.2 V_{P-P}, C_{IN} = none, C_{OUT} = 10 µF
V_{SET} = 1.2 V, V_{IN} = 5.5 V to 2.5 V, I_{OUT} = 1 mA



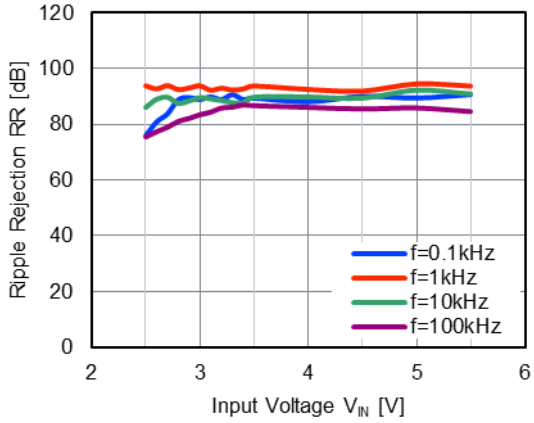
V_{SET} = 1.2 V, V_{IN} = 5.5 V to 2.5 V, I_{OUT} = 100 mA



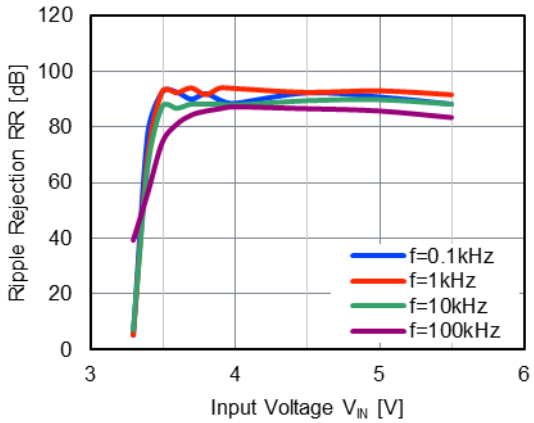
V_{SET} = 1.8 V, V_{IN} = 5.5 V to 2.5 V, I_{OUT} = 1 mA



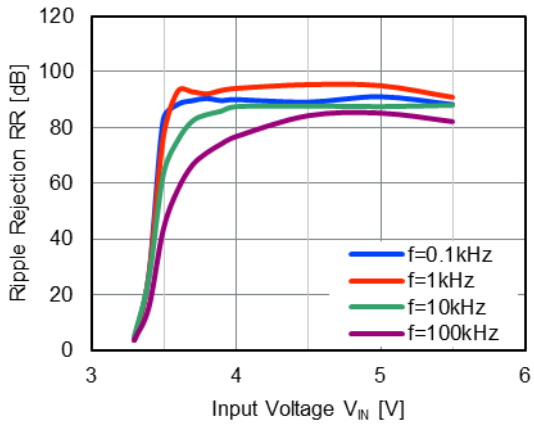
V_{SET} = 1.8 V, V_{IN} = 5.5 V to 2.5 V, I_{OUT} = 100 mA



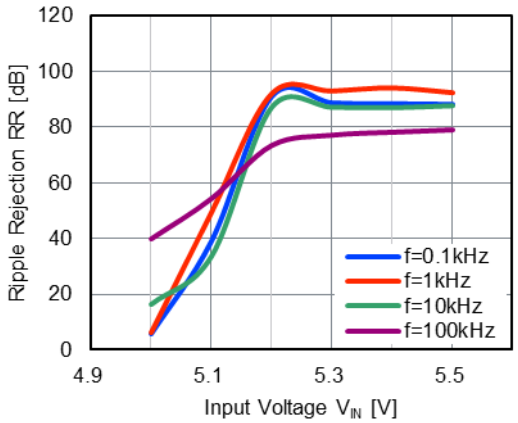
V_{SET} = 3.3 V, V_{IN} = 5.5 V to 3.3 V, I_{OUT} = 1 mA



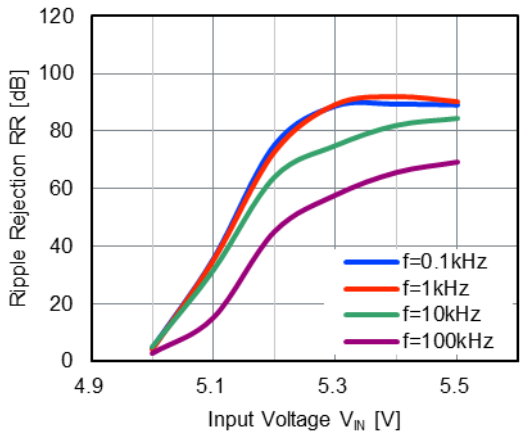
V_{SET} = 3.3 V, V_{IN} = 5.5 V to 3.3 V, I_{OUT} = 100 mA



V_{SET} = 5.0 V, V_{IN} = 5.5 V to 5.0 V, I_{OUT} = 1 mA



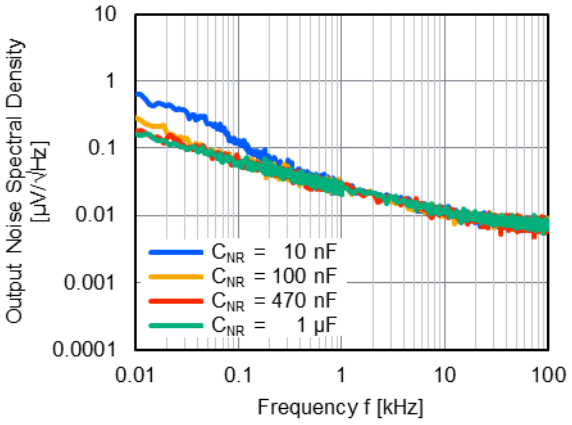
V_{SET} = 5.0 V, V_{IN} = 5.5 V to 5.0 V, I_{OUT} = 100 mA



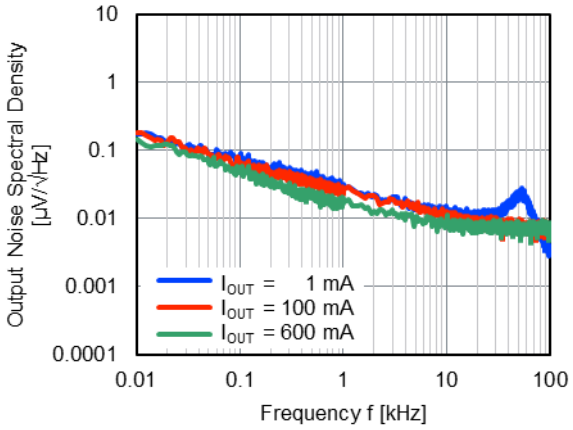
12) Output Noise Spectral Density vs Frequency

V_{SET} = 1.2 V, V_{IN} = 2.5 V, C_{OUT} = 10 µF

I_{OUT} = 100 mA

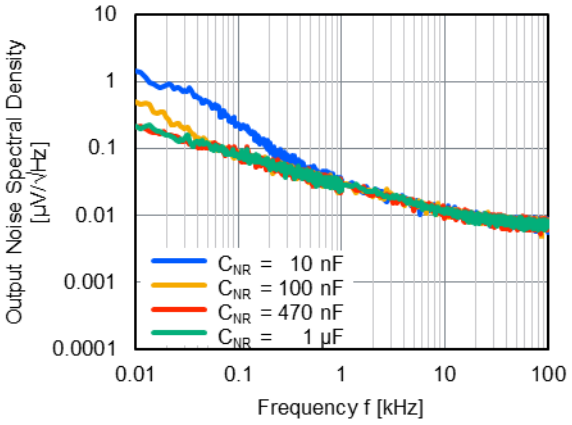


C_{NR} = 470 nF

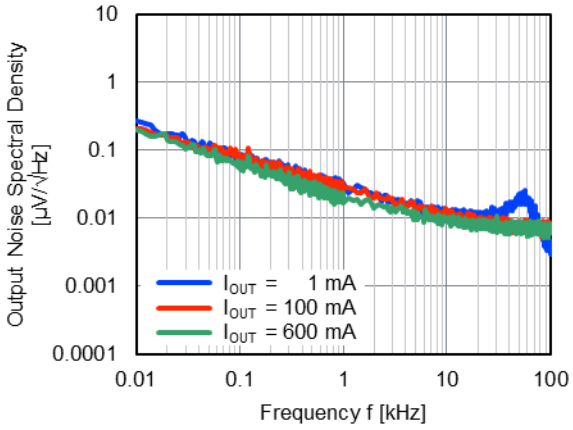


V_{SET} = 1.8 V, V_{IN} = 2.8 V, C_{OUT} = 10 µF

I_{OUT} = 100 mA

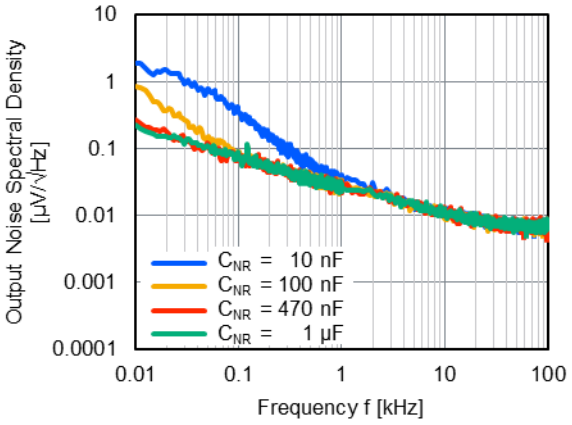


C_{NR} = 470 nF

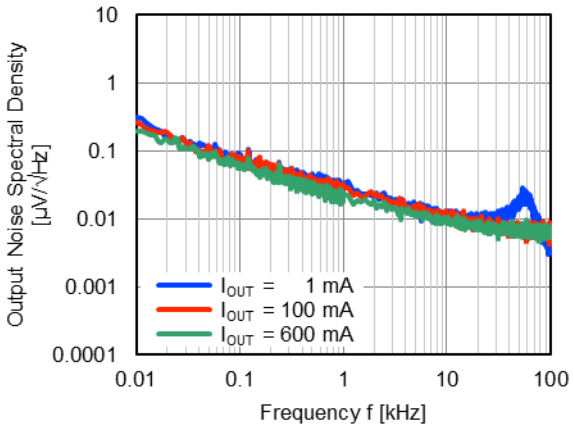


V_{SET} = 3.3 V, V_{IN} = 4.3 V, C_{OUT} = 10 µF

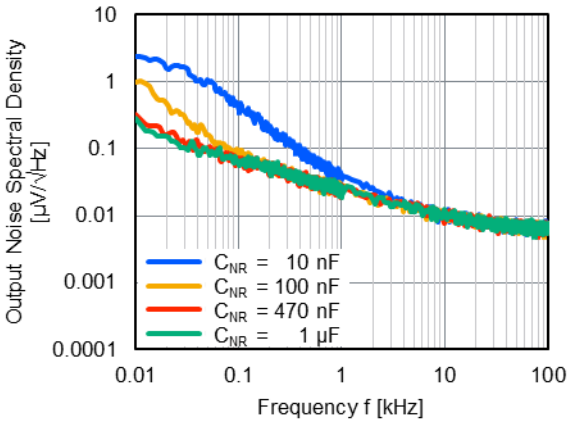
I_{OUT} = 100 mA



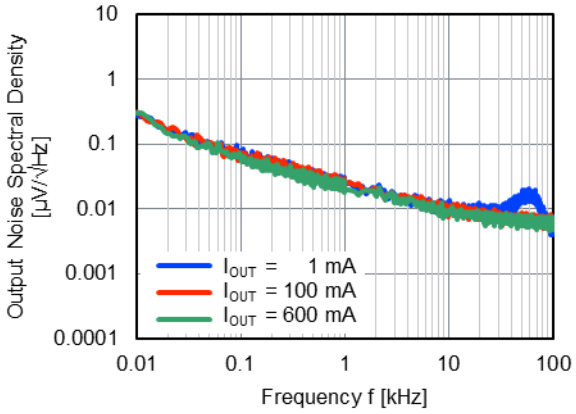
C_{NR} = 470 nF



V_{SET} = 5.0 V, V_{IN} = 5.5 V, C_{OUT} = 10 µF
I_{OUT} = 100 mA



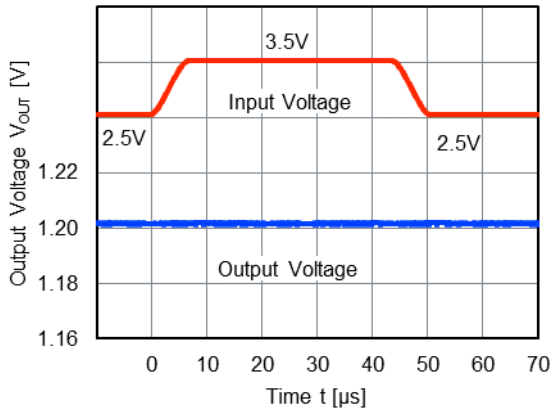
C_{NR} = 470 nF



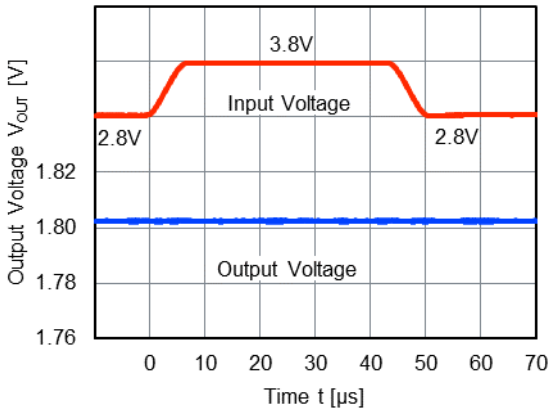
13) Input Transient Response

I_{OUT} = 1 mA, C_{IN} = none, C_{OUT} = 10 µF

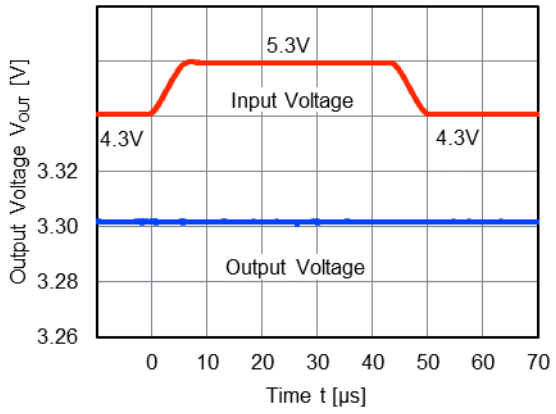
V_{SET} = 1.2 V



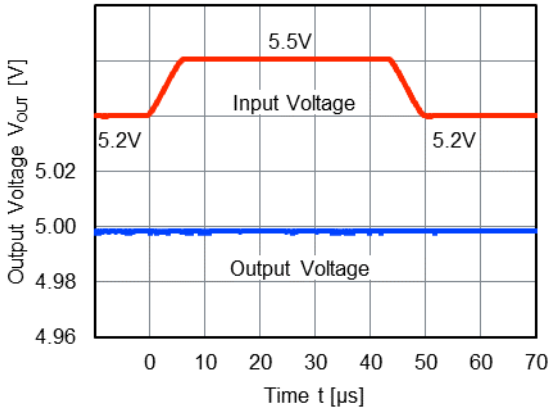
V_{SET} = 1.8 V



V_{SET} = 3.3 V



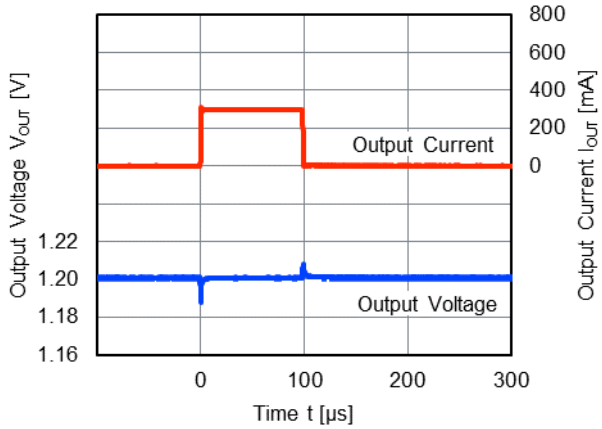
V_{SET} = 5.0 V



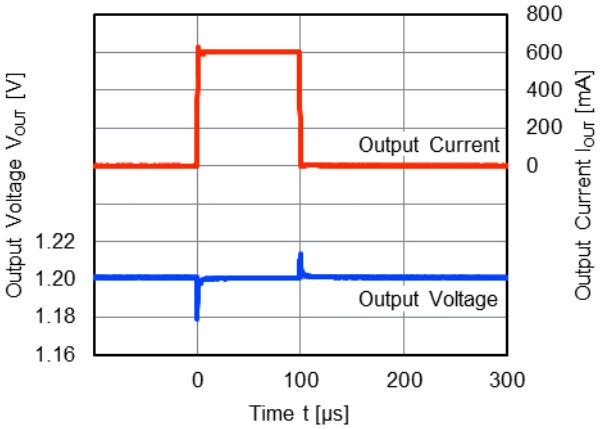
14) Load Transient Response

V_{SET} = 1.2 V, C_{OUT} = 1000 µF

I_{OUT} = 1 mA ↔ 300 mA

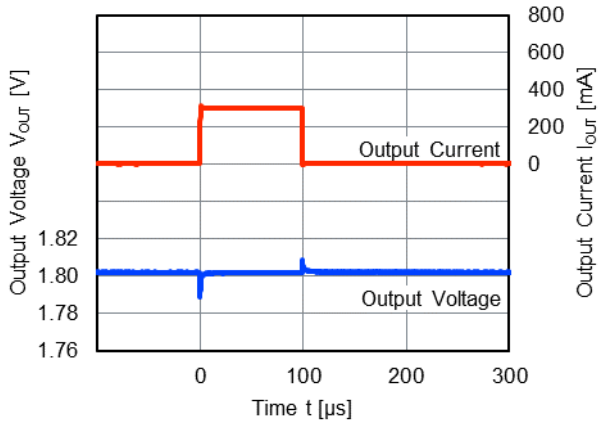


I_{OUT} = 1 mA ↔ 600 mA

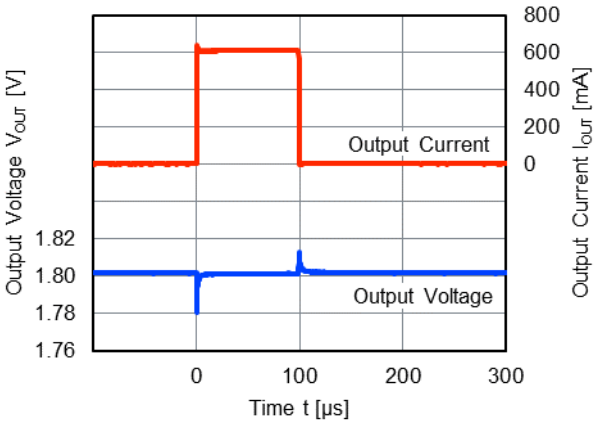


V_{SET} = 1.8 V, C_{OUT} = 1000 µF

I_{OUT} = 1 mA ↔ 300 mA

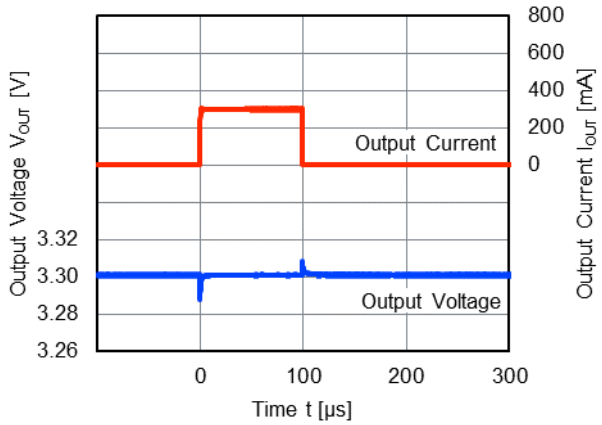


I_{OUT} = 1 mA ↔ 600 mA

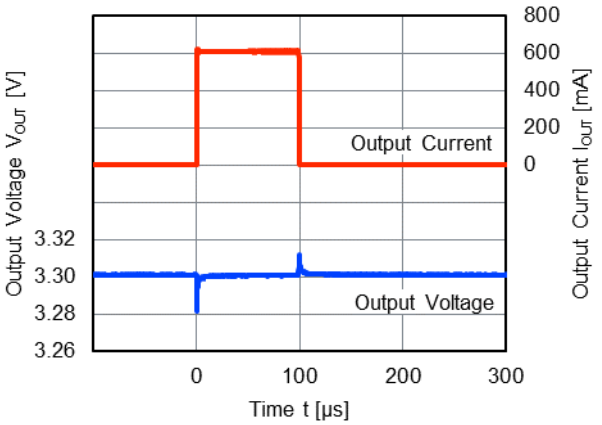


V_{SET} = 3.3 V, C_{OUT} = 1000 µF

I_{OUT} = 1 mA ↔ 300 mA

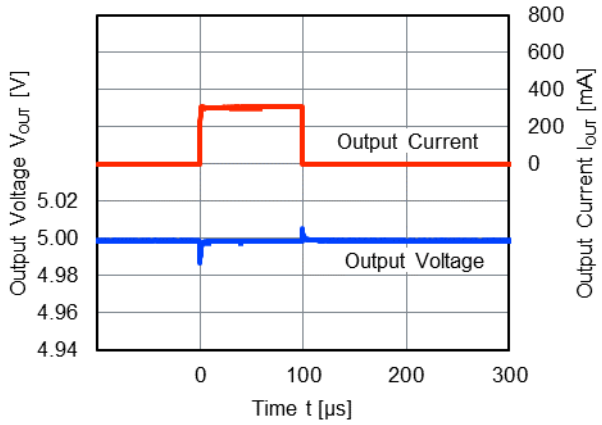


I_{OUT} = 1 mA ↔ 600 mA

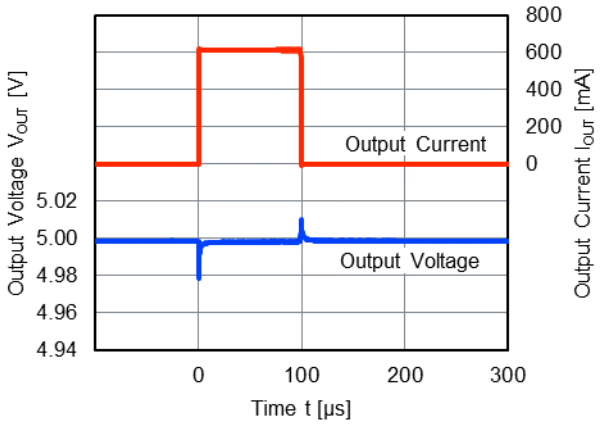


V_{SET} = 5.0 V, C_{OUT} = 1000 µF

I_{OUT} = 1 mA ↔ 300 mA



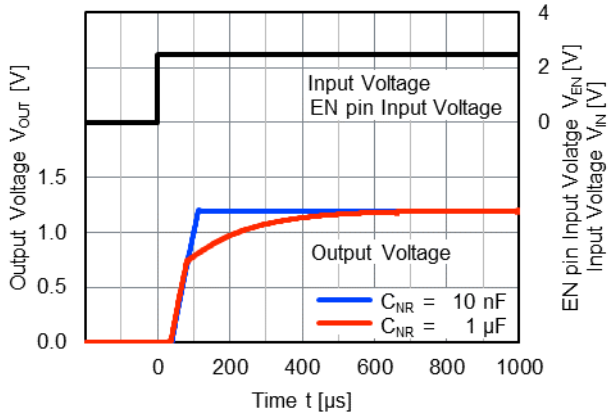
I_{OUT} = 1 mA ↔ 600 mA



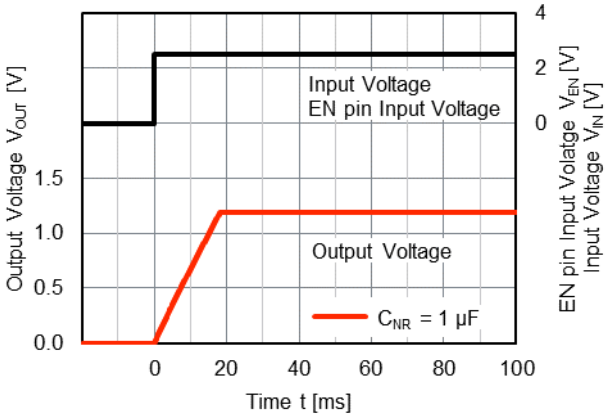
15) Turn on Speed with the EN Pin

V_{SET} = 1.2 V

C_{OUT} = 10 µF

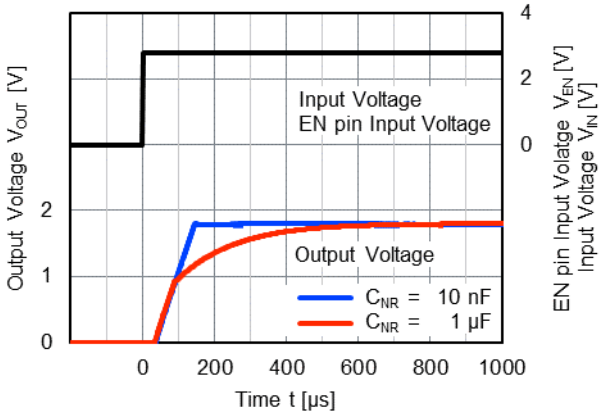


C_{OUT} = 2200 µF, C_{NR} = 1 µF

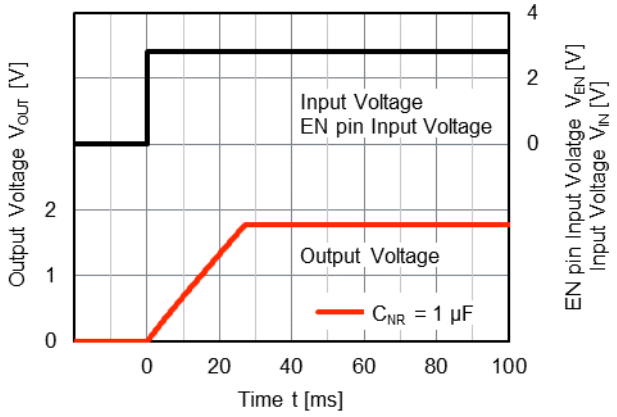


V_{SET} = 1.8 V

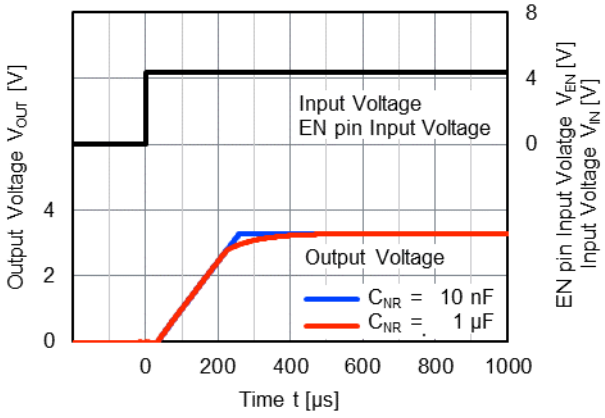
C_{OUT} = 10 µF



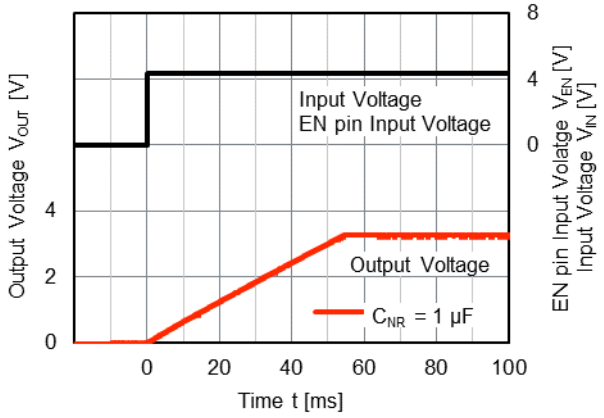
C_{OUT} = 2200 µF, C_{NR} = 1 µF



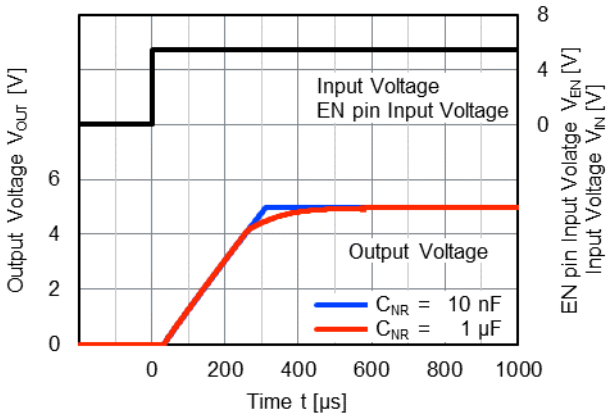
V_{SET} = 3.3 V
C_{OUT} = 10 µF



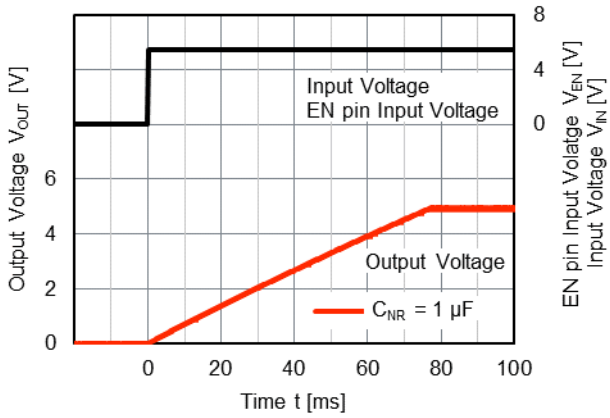
C_{OUT} = 2200 µF, C_{NR} = 1 µF



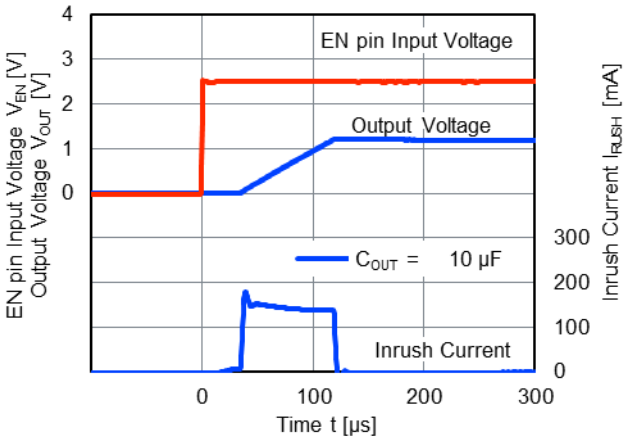
V_{SET} = 5.0 V
C_{OUT} = 10 µF



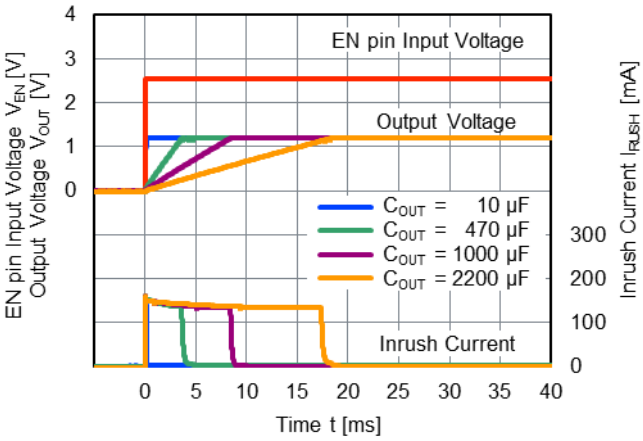
C_{OUT} = 2200 µF, C_{NR} = 1 µF



16) Inrush Current vs Output Capacitor
V_{SET} = 1.2 V
C_{OUT} = 10 µF (Enlarged View)

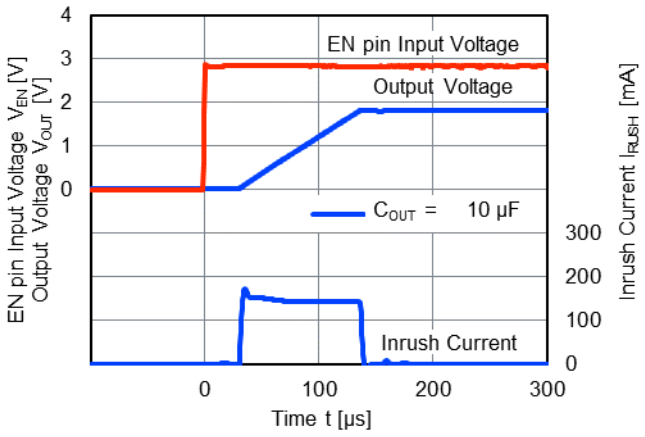


C_{OUT} = 10 µF, 470 µF, 1000 µF, 2200 µF

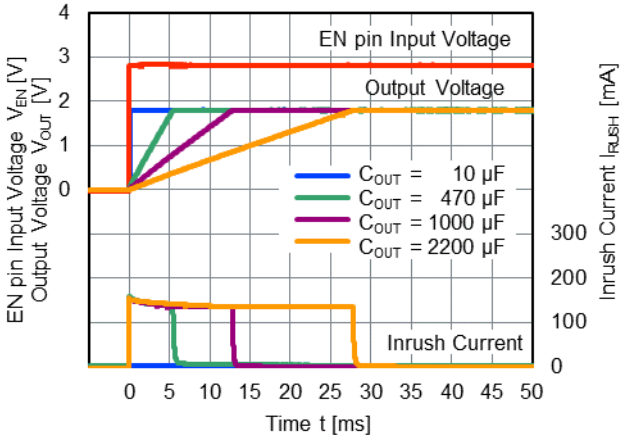


V_{SET} = 1.8 V

C_{OUT} = 10 µF (Enlarged View)

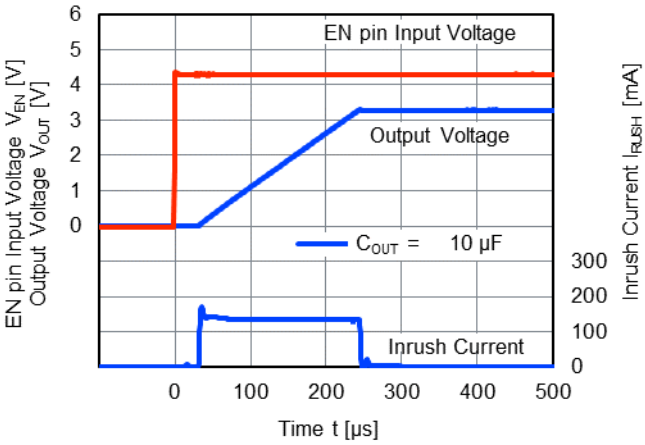


C_{OUT} = 10 µF, 470 µF, 1000 µF, 2200 µF

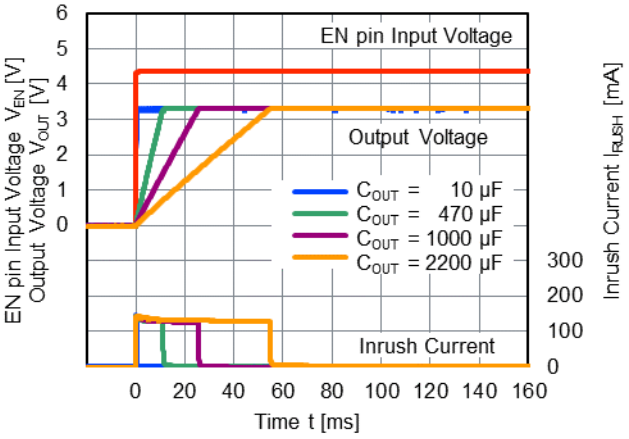


V_{SET} = 3.3 V

C_{OUT} = 10 µF (Enlarged View)

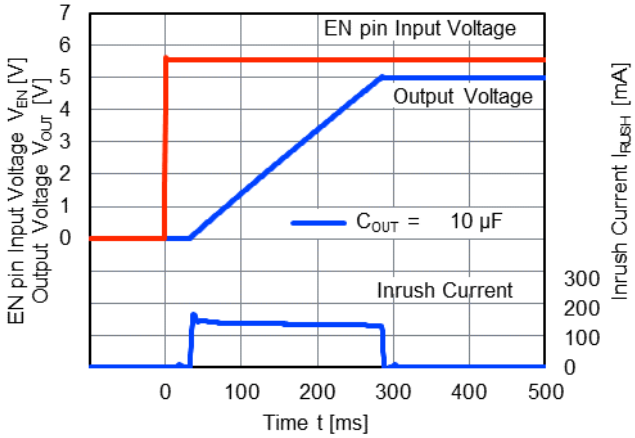


C_{OUT} = 10 µF, 470 µF, 1000 µF, 2200 µF

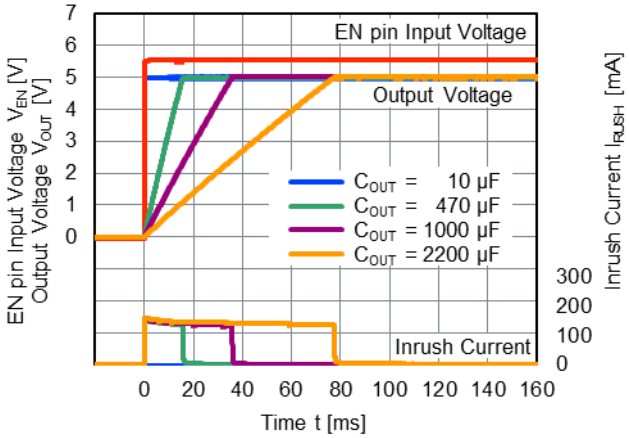


V_{SET} = 5.0 V

C_{OUT} = 10 µF (Enlarged View)



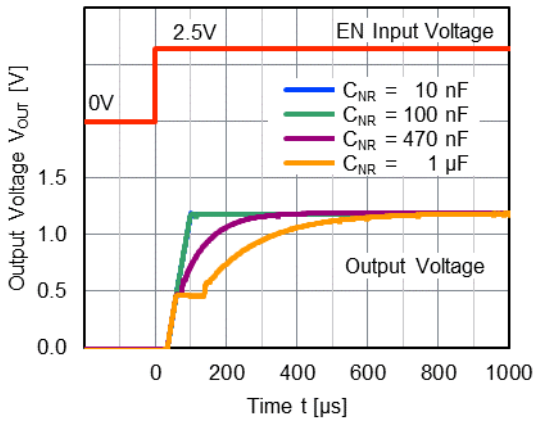
C_{OUT} = 10 µF, 470 µF, 1000 µF, 2200 µF



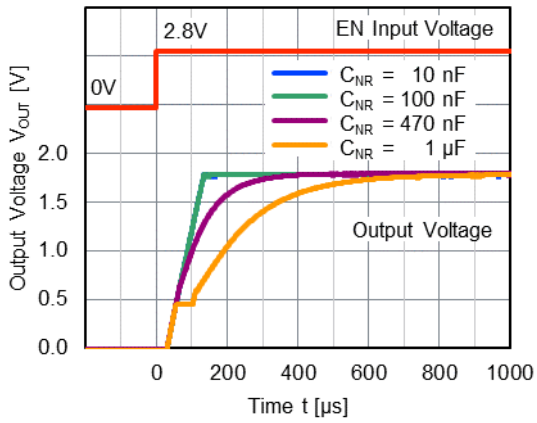
17) Turn on Speed vs Noise Reduction Capacitor

C_{OUT} = 10 µF

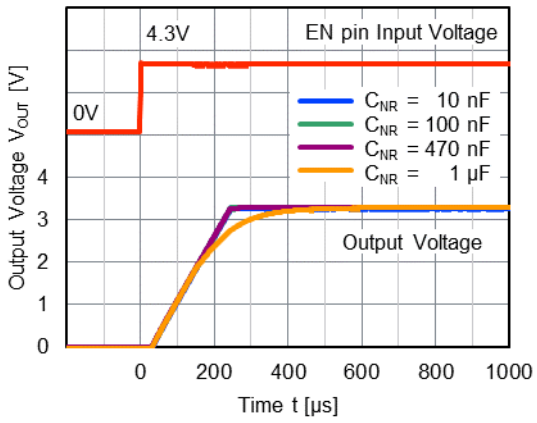
V_{SET} = 1.2 V



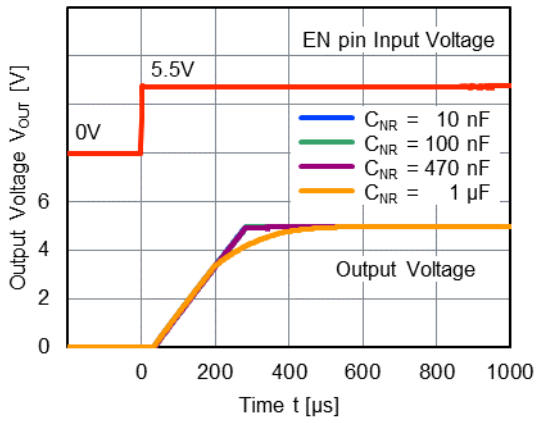
V_{SET} = 1.8 V



V_{SET} = 3.3 V



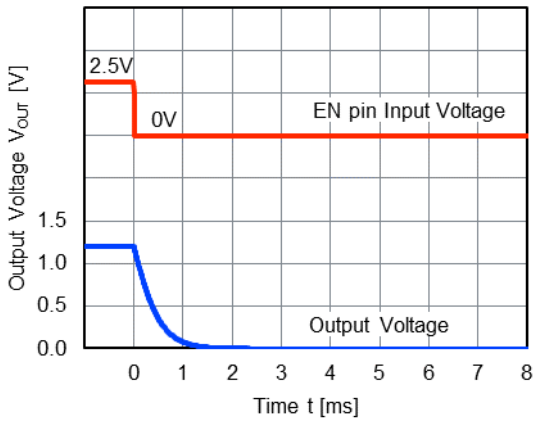
V_{SET} = 5.0 V



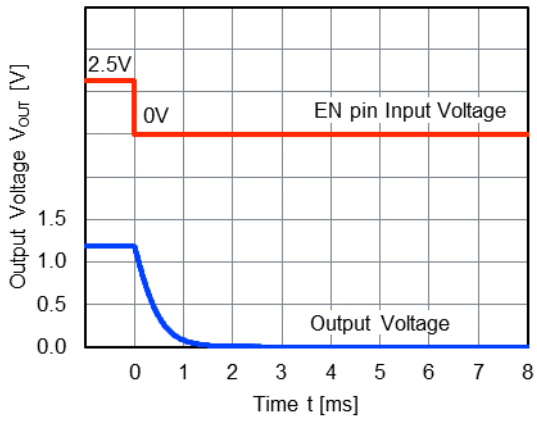
18) Turn off Speed with the EN Pin

V_{SET} = 1.2 V, C_{OUT} = 10 µF

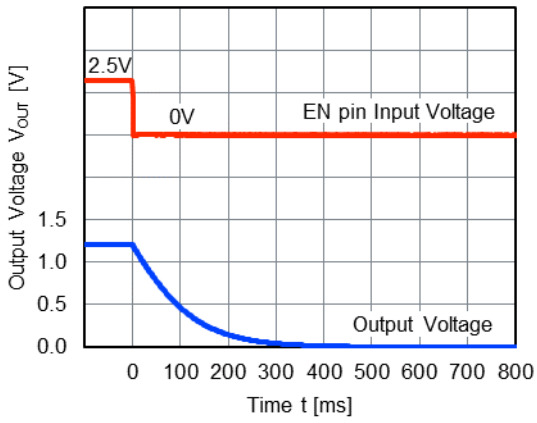
C_{NR} = 10 nF



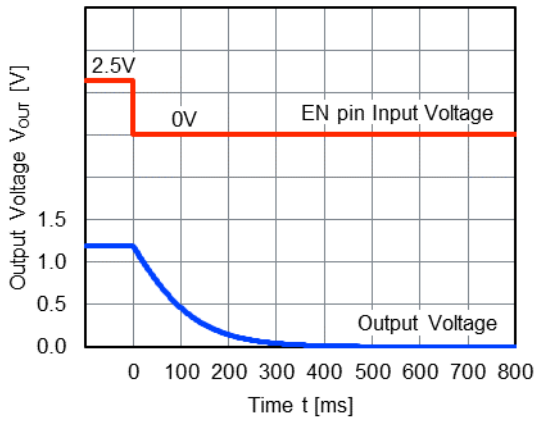
C_{NR} = 1 µF



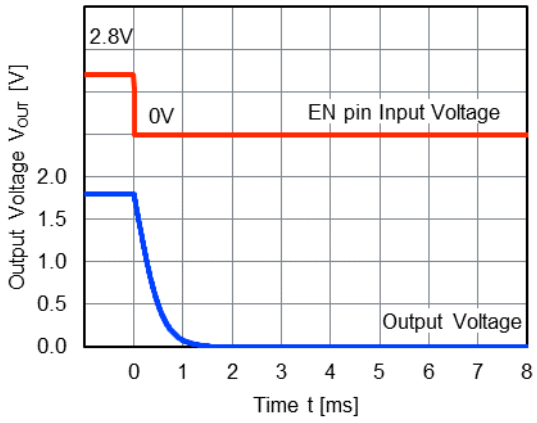
V_{SET} = 1.2 V, C_{OUT} = 2200 µF
C_{NR} = 10 nF



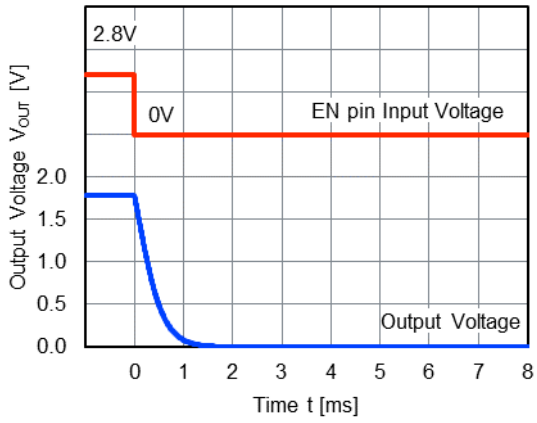
C_{NR} = 1 µF



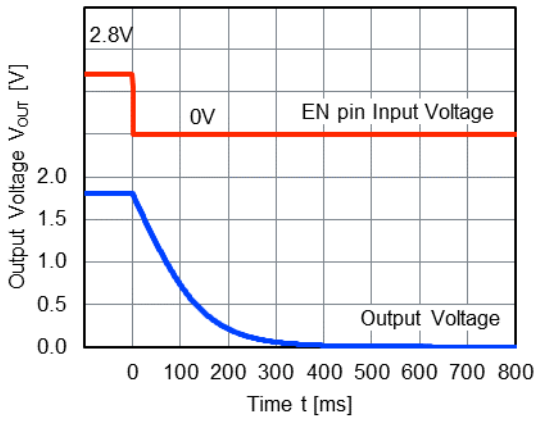
V_{SET} = 1.8 V, C_{OUT} = 10 µF
C_{NR} = 10 nF



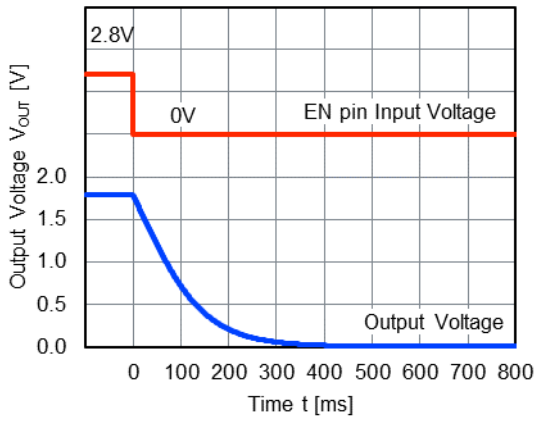
C_{NR} = 1 µF



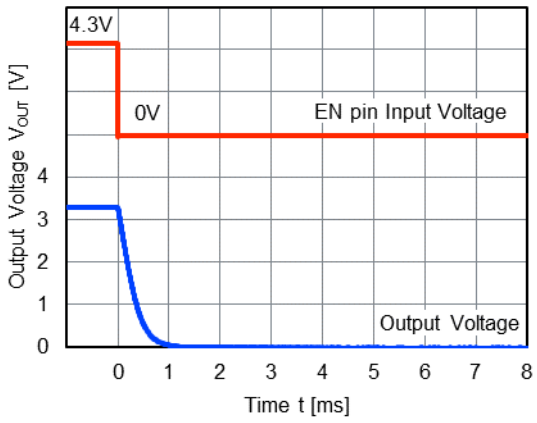
V_{SET} = 1.8 V, C_{OUT} = 2200 µF
C_{NR} = 10 nF



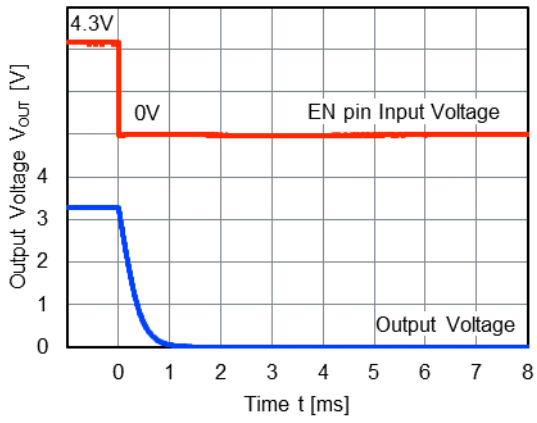
C_{NR} = 1 µF



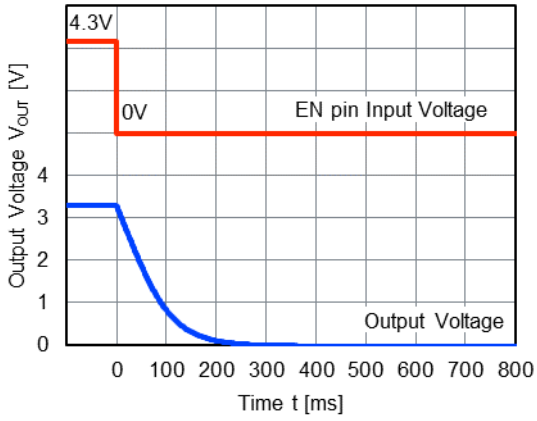
V_{SET} = 3.3 V, C_{OUT} = 10 µF
C_{NR} = 10 nF



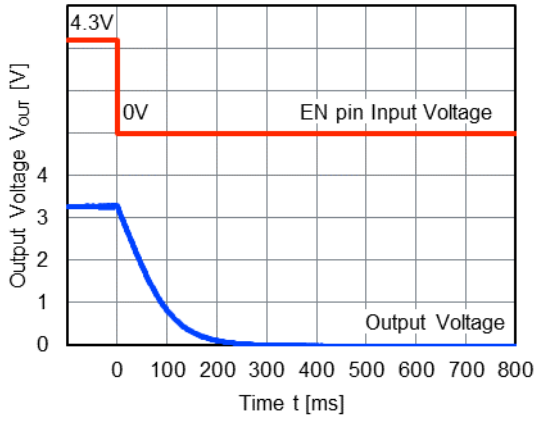
C_{NR} = 1 µF



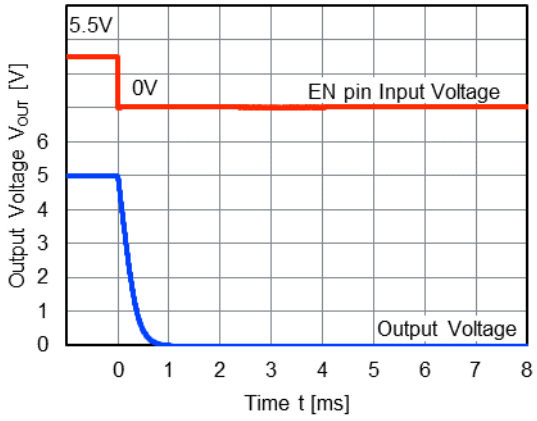
V_{SET} = 3.3 V, C_{OUT} = 2200 µF
C_{NR} = 10 nF



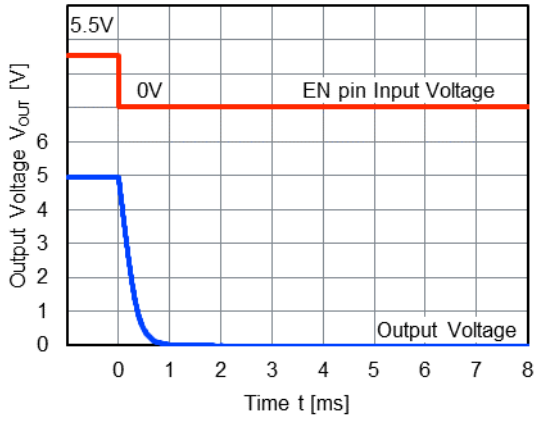
C_{NR} = 1 µF



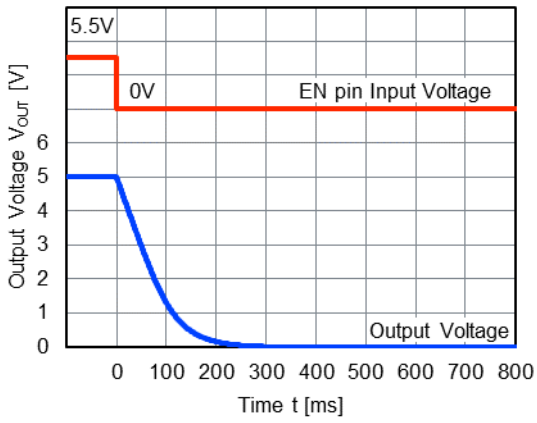
V_{SET} = 5.0 V, C_{OUT} = 10 µF
C_{NR} = 10 nF



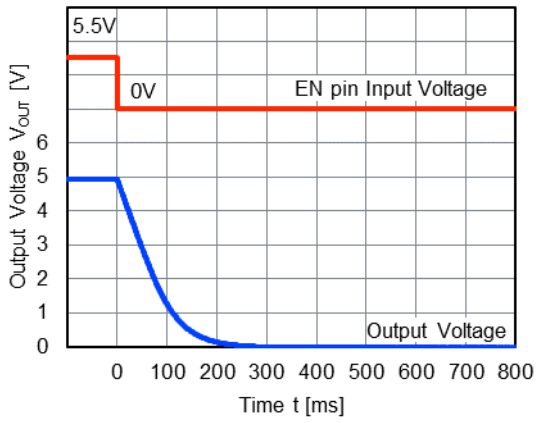
C_{NR} = 1 µF



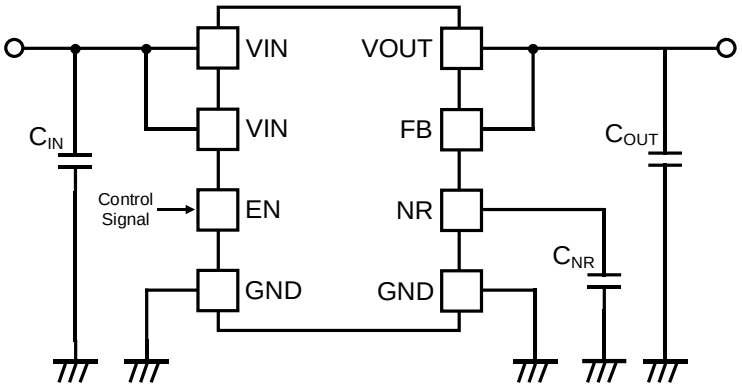
V_{SET} = 5.0 V, C_{OUT} = 2200 µF
C_{NR} = 10 nF



C_{NR} = 1 µF



■ TEST CIRCUIT



MUSES100 Test Circuit

【Components list for our evaluation】

Symbol	Capacitance	Parts Number
C_{IN}	10 µF	25NS106MD15750
C_{NR}	10 nF	63NS103MZ12012
	100 nF	63NS103MZ12012
	470 nF	35NS474MA13216
	1 µF	25NS105MA23216
C_{OUT}	10 µF	25NS106MD15750
	470 µF	UKA1C471MPD
	1000 µF	UKA1C102MPD
	2200 µF	UKA1C222MHD

■ NOTE

Precaution for counterfeit semiconductor products

We have recently detected many counterfeit semiconductor products that have very similar appearances to our operational amplifier “MUSES” in the world-wide market. In most cases, it is hard to distinguish them from our regular products by their appearance, and some of them have very poor quality and performance.
They can not provide equivalent quality of our regular product, and they may cause breakdowns or malfunctions if used in your systems or applications.

We would like our customers to purchase “MUSES” through our official sales channels : our sales branches, sales subsidiaries and distributors.

Please note that we hold no responsibilities for any malfunctions or damages caused by using counterfeit products. We would appreciate your understanding.

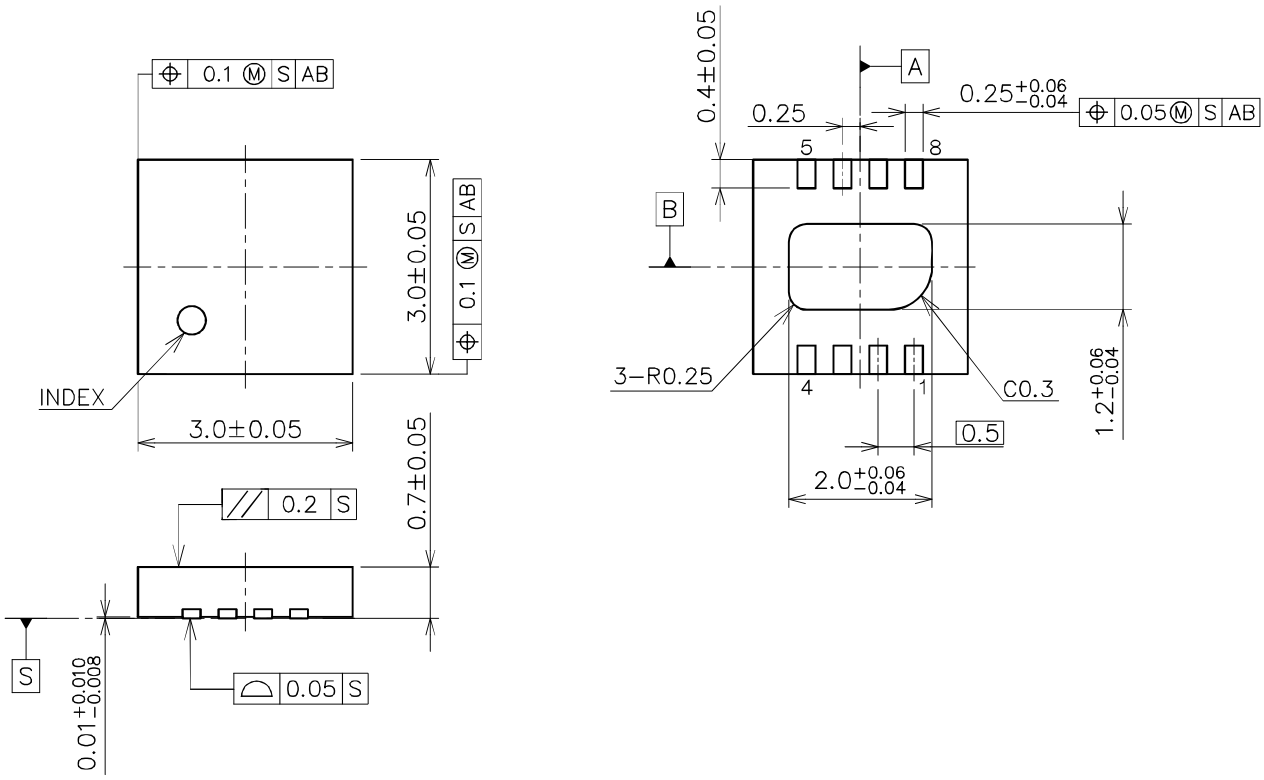
Nisshinbo Micro Devices Inc.

DFN3030-8-GQ

DFN3030-8-GQ-E-A

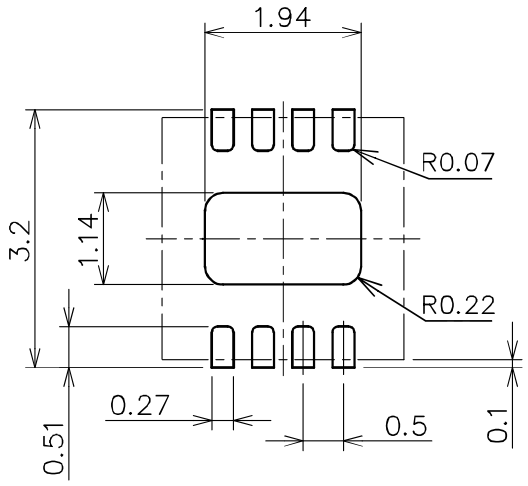
■ PACKAGE DIMENSIONS

UNIT: mm



■ EXAMPLE OF SOLDER PADS DIMENSIONS

UNIT: mm



Nisshinbo Micro Devices Inc.

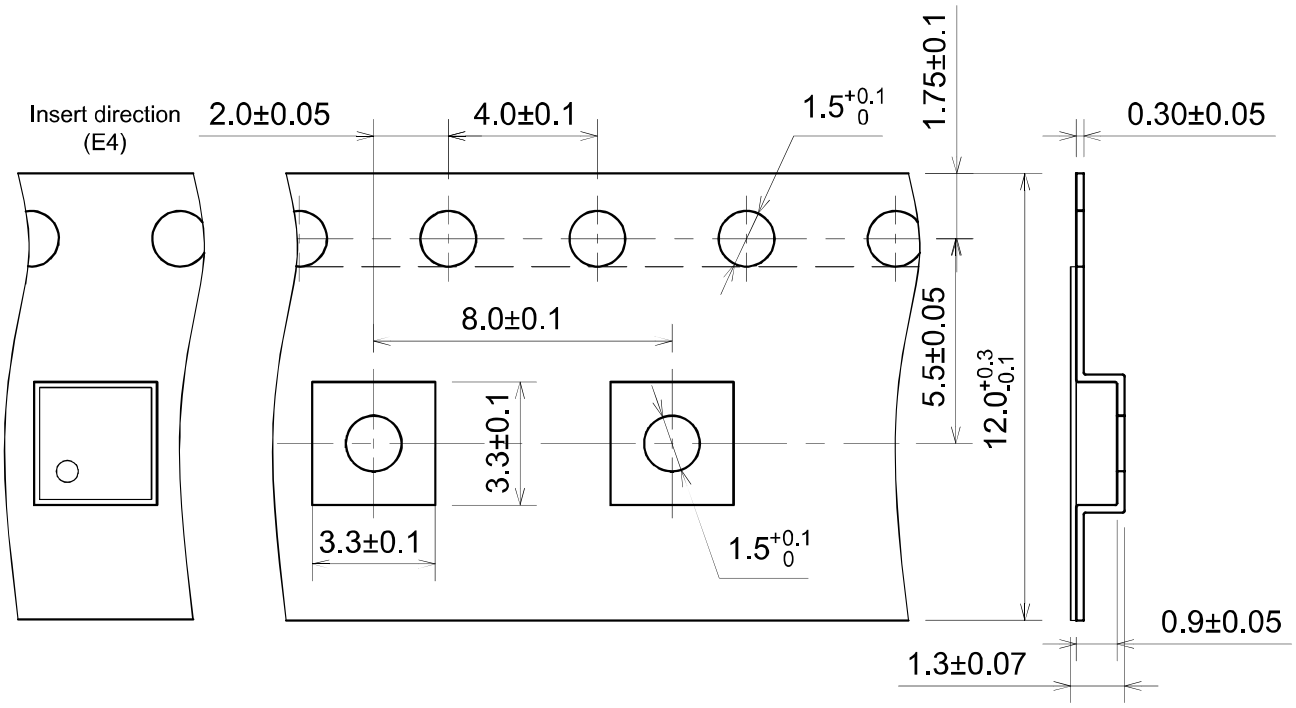
DFN3030-8-GQ

DFN3030-8-GQ-E-A

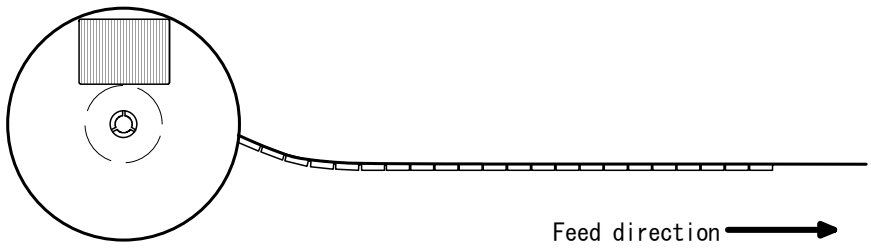
■ PACKING SPEC

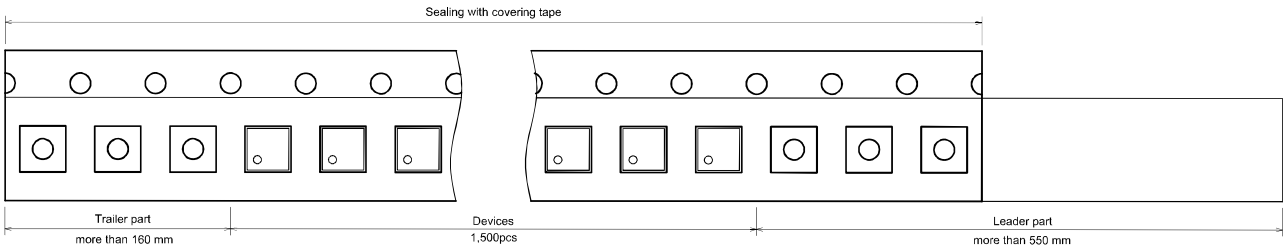
UNIT: mm

(1) Taping dimensions / Insert direction

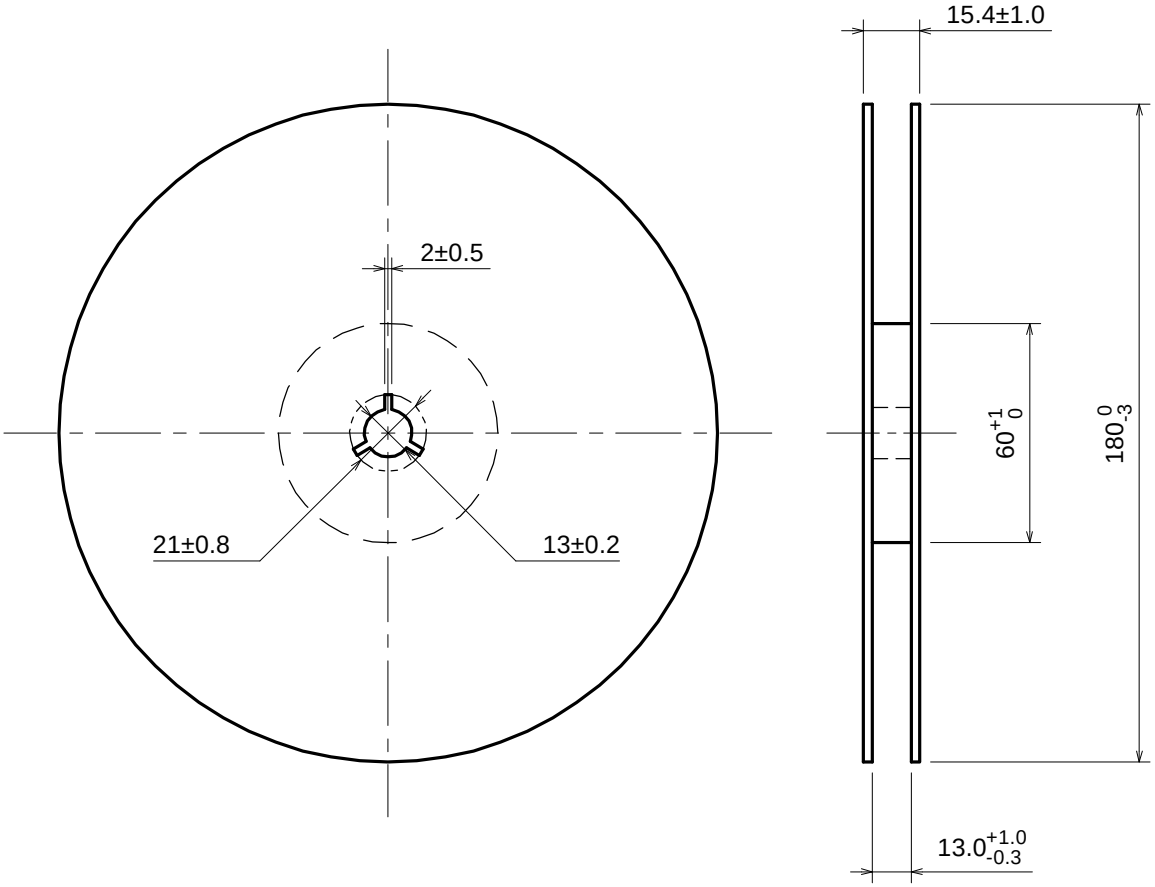


(2) Taping state





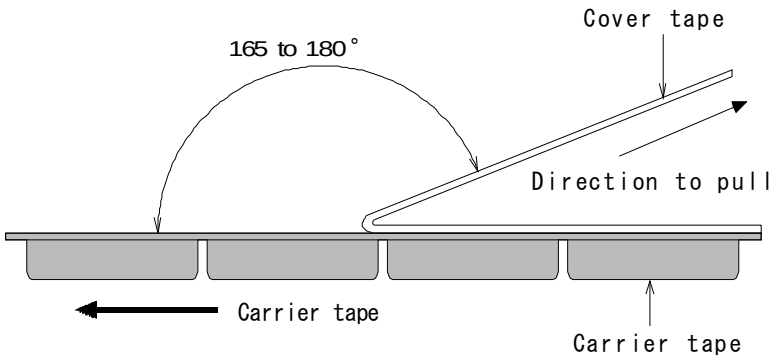
(3) Reel dimensions



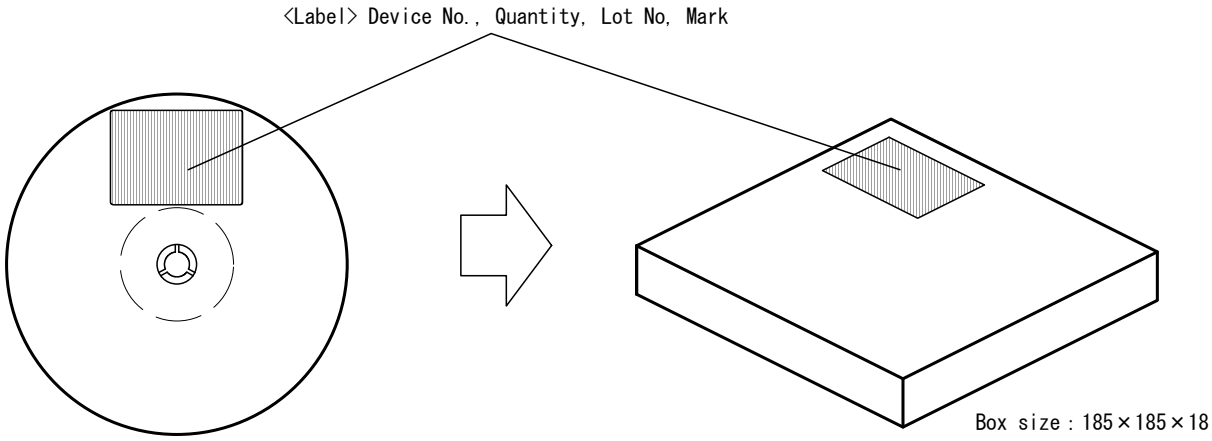
(4) Peeling strength

Peeling strength of cover tape

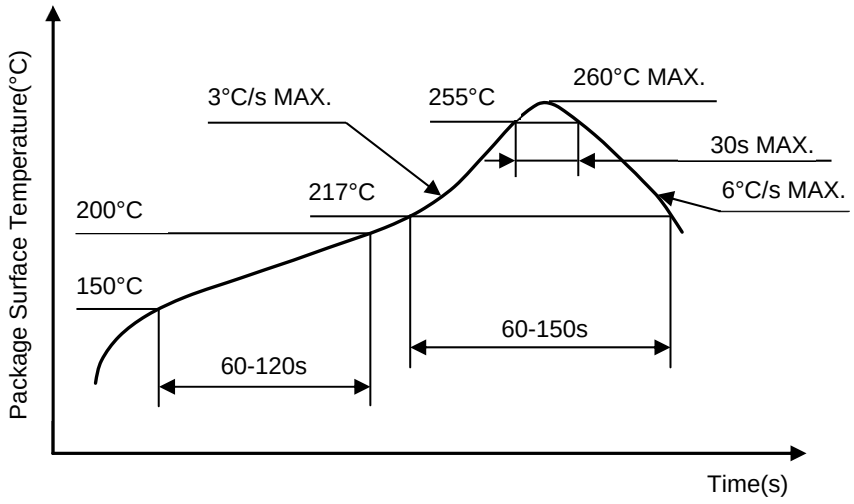
- Peeling angle 165 to 180°degrees to the taped surface.
- Peeling speed 300mm/min
- Peeling strength 0.1 to 1.3N



(5) Packing state



■ **HEAT-RESISTANCE PROFILES**



Reflow profile

■ REVISION HISTORY

Date	Revision	Contents of Changes
May 31, 2024	1.0	Initial release

1. The products and the product specifications described in this document are subject to change or discontinuation of production without notice for reasons such as improvement. Therefore, before deciding to use the products, please refer to our sales representatives for the latest information thereon.
2. The materials in this document may not be copied or otherwise reproduced in whole or in part without the prior written consent of us.
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    - Aerospace Equipment
    - Equipment Used in the Deep Sea
    - Power Generator Control Equipment (nuclear, steam, hydraulic, etc.)
    - Life Maintenance Medical Equipment
    - Fire Alarms / Intruder Detectors
    - Vehicle Control Equipment (automotive, airplane, railroad, ship, etc.)
    - Various Safety Devices
    - Traffic control system
    - Combustion equipment

    In case your company desires to use this product for any applications other than general electronic equipment mentioned above, make sure to contact our company in advance. Note that the important requirements mentioned in this section are not applicable to cases where operation requirements such as application conditions are confirmed by our company in writing after consultation with your company.
6. We are making our continuous effort to improve the quality and reliability of our products, but semiconductor products are likely to fail with certain probability. In order to prevent any injury to persons or damages to property resulting from such failure, customers should be careful enough to incorporate safety measures in their design, such as redundancy feature, fire containment feature and fail-safe feature. We do not assume any liability or responsibility for any loss or damage arising from misuse or inappropriate use of the products.
7. The products have been designed and tested to function within controlled environmental conditions. Do not use products under conditions that deviate from methods or applications specified in this datasheet. Failure to employ the products in the proper applications can lead to deterioration, destruction or failure of the products. We shall not be responsible for any bodily injury, fires or accident, property damage or any consequential damages resulting from misuse or misapplication of the products.
8. Quality Warranty
    8-1. Quality Warranty Period
    In the case of a product purchased through an authorized distributor or directly from us, the warranty period for this product shall be one (1) year after delivery to your company. For defective products that occurred during this period, we will take the quality warranty measures described in section 8-2. However, if there is an agreement on the warranty period in the basic transaction agreement, quality assurance agreement, delivery specifications, etc., it shall be followed.
    8-2. Quality Warranty Remedies
    When it has been proved defective due to manufacturing factors as a result of defect analysis by us, we will either deliver a substitute for the defective product or refund the purchase price of the defective product.
    Note that such delivery or refund is sole and exclusive remedies to your company for the defective product.
    8-3. Remedies after Quality Warranty Period
    With respect to any defect of this product found after the quality warranty period, the defect will be analyzed by us. On the basis of the defect analysis results, the scope and amounts of damage shall be determined by mutual agreement of both parties. Then we will deal with upper limit in Section 8-2. This provision is not intended to limit any legal rights of your company.
9. Anti-radiation design is not implemented in the products described in this document.
10. The X-ray exposure can influence functions and characteristics of the products. Confirm the product functions and characteristics in the evaluation stage.
11. WLCSP products should be used in light shielded environments. The light exposure can influence functions and characteristics of the products under operation or storage.
12. Warning for handling Gallium and Arsenic (GaAs) products (Applying to GaAs MMIC, Photo Reflector). These products use Gallium (Ga) and Arsenic (As) which are specified as poisonous chemicals by law. For the prevention of a hazard, do not burn, destroy, or process chemically to make them as gas or power. When the product is disposed of, please follow the related regulation and do not mix this with general industrial waste or household waste.
13. Please contact our sales representatives should you have any questions or comments concerning the products or the technical information.

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