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ADVANCE INFORMATION

DS3046-2.1

MV1403

PCM MACROCELL DEMONSTRATOR

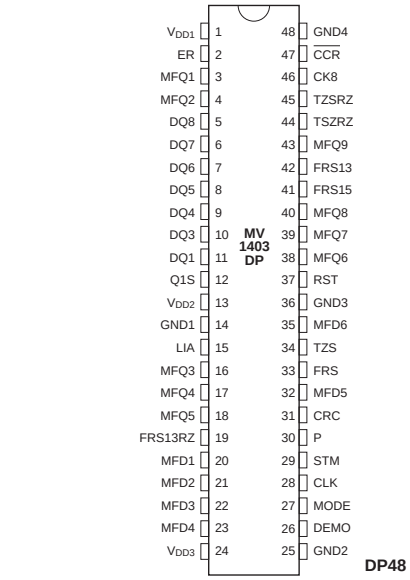
The MV1403 contains 8 PCM macrocells which can be configured so as to perform the common channel signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link, operating to the appropriate CCITT recommendations. The MV1403 also allows access to all the macrocells individually and is implemented in GPS CMOS technology utilising the CLA60000 series gate array, offering high performance, low power and fast turn-round. The following macrocells are included in the MV1403.

Timeslot Zero Transmitter - **TXTSZ**
Timeslot Sixteen Transmitter - **TXTS16**
Cyclic Redundancy Check Generator - **CRCGEN**
High Density Bipolar (HDB) 3 Encoder - **HDB3EC**
Timeslot Zero Receiver - **RXTSZ**
Timeslot Sixteen Receiver - **RXTS16**
Cyclic Redundancy Checker - **CRCCHK**
High Density Bipolar (HDB) 3 Decoder - **HDB3DC**

With the MV1403 set up to combine the internal macrocells, two demonstration modes are available, referred to as Transmit and Receive demonstration modes.

In Transmit demonstration mode, timeslot zero sync word (including user data bits and optional CRC check bits), timeslot sixteen data and 30 voice channels are combined and transmitted as pseudo-ternary HDB3 encoded outputs. The Transmit demonstration mode can also be set to generate CRC multiframe data in accordance with CCITT Recommendation G. 704.

In Receive demonstration mode, the pseudo-ternary HDB3 inputs are decoded back to NRZ form and frame synchronisation is achieved by detection of the Frame Alignment signal in the incoming data stream. This permits extraction of user data bits, timeslot sixteen data and voice channel data. An optional CRC mode generates CRC multiframe alignment and a cyclic redundancy check is carried out on the incoming data. In addition receive demonstration mode generates appropriate alarms for loss of input, double violation on the HDB3 inputs, loss of frame or CRC multiframe alignment, detection of erroneous frame alignment word, remote alarm received from the transmitter, and detection of a CRC error in either submultiframe 1 or 2.



NOTE: MFD is multi-function input,
MFQ is multi-function output

Figure 1: Pin connections - top view

FEATURES

- Single + 5V Supply
- All Inputs and Outputs TTL Compatible
- Selectable as PCM Transmitter or Receiver
- Allows Access to all 8 Macrocells Individually
- HDB3 Encoding and Decoding to CCITT Recommendation G. 703
- Transmitted Frame Structure to CCITT Recommendation G. 704
- Receiver Frame Synchronisation to CCITT
- Recommendation G. 732
- Selectable CRC Mode
- CRC Generation and Checking to CCITT Recommendation G. 704

FUNCTIONAL DESCRIPTION

The MV1403 PCM macrocell demonstrator contains a family of 4 Transmit PCM and 4 Receive PCM macrocells which may be configured to function individually, or be connected together to form demonstrations of their operation. In order to keep the pin count to a minimum, some of the input and output pins are shared. Pin functions thus depend upon whether the device is configured as a transmitter or receiver. The operational modes of the MV1403 are selected under control of the MODE and DEMO pins, as shown in Table 1. Note that the MODE pin selects either the transmit or receive set of macrocells and that the DEMO pins selects either individual or combined connections.

In addition the operation of the MV1403 is controlled by a further two control inputs, STM and CRC. The STM pin is used for device testing and should be tied low for normal operation. The CRC control pin selects whether or not the device-performs the CRC generation/checking procedure. A logic High' on this pin puts the device in Cyclic Redundancy Generate/Check mode.

More detailed information about all 8 macrocells can be found in the individual macrocell publications.

INDIVIDUAL TRANSMIT MODE, TX1

In this mode (MODE = 0, DEMO = 0) the four transmitter macrocells (TXTSZ, TXTS16, CRCGEN and HDB3EC) are all accessed individually. The functional diagram of the MV1403 in this mode is shown in Fig. 2. All four macrocells are synchronised to a common 2.048MHz clock, and the TXTSZ, TXTS16 and CRCGEN macrocells are also synchronised to a second timing input, FRS (Frame Sync). This is an 8 clock period high going pulse at 8kHz which masks timeslot zero to enable frame alignment. The function of each transmit macrocell is now described separately.

TIMESLOT ZERO TRANSMITTER

The Timeslot Zero Transmitter macrocell generates a Frame Alignment Signal (FAS) in accordance with CCITT Recommendation G. 704. This is combined with the international spare bit (the D1 input) and output on Q during timeslot zero of alternate frames, denoted sync frames. During the other interleaved frames, denoted non-sync frames, bit 2 is fixed at logic 1 to avoid imitation of the FAS. This bit is slotted together with the international spare bit (D1 input) and 6 user data bits (the D3N-D8N inputs) for output on Q.

A TZS output (Timeslot Zero Sync frame) is provided to denote whether a sync frame or non-sync frame is being output. It changes state one clock period after the end of timeslot zero and is high during timeslot zero of sync frames.

Fig. 3 shows the timing diagram for this macrocell.

TIMESLOT SIXTEEN TRANSMITTER

This macrocell takes in a continuous 64kbit data stream (D input) and outputs it in 8 bit packets at a bit rate of 2.048 Mbit during timeslot 16 of successive frames on its Q output. The position of timeslot 16 is determined from the FRS timing input, which masks timeslot zero. The TS16 output is an 8 clock period high going pulse at 8kHz, similar to FRS, but high during the 8 bits of timeslot sixteen.

Fig. 4 shows the timing diagram for this macrocell.

CYCLIC REDUNDANCY CHECK GENERATOR

This macrocell has two modes of operation, selected by its EN control input. When EN is 'high', CRC generation mode is selected. However, both modes are concerned with producing the data bit to be inserted into the international spare bit of timeslot zero (CCITT G. 704 structure). In non-CRC mode, this data is selected to be either the D1S (sync frames) or DlN (non-sync frames) input depending upon whether a sync or non-sync frame is about to be transmined (determined by the TZS input).

With CRC mode enabled, the macrocell generates CRC words and outputs this data during the international spare bit of sync frames. During non-sync frames, the 6 bit CRC Multiframe Alignment Signal is output along with the two user data inputs, DlS and D1N. This procedure is carried out in accordance with CCITT Recommendation G. 704. The CRC word is generated from the incoming data stream on the D input pin. CCITT Recommendation G. 704 defines the 16 frame CRC multiframe structure, not related to the possible use of a 16 frame multiframe structure in timeslot 16. Each 16 frame CRC multiframe is divided into two 8 frame sub-multiframes, denoted submultiframes 1 and 2 (SMF1 and SMF2). The CRC procedure is carried out on each sub-multiframe of data and the resulting 4 bit CRC word is output during the international spare bit of sync frames during the following sub-multiframe. All data is output on the Q output pin. Table 2 displays the CRC multiframe structure in more detail .

HIGH DENSITY BIPOLAR (HDB3)ENCODER

The HDB3 Encoder macrocell converts the incoming NRZ data on its D input pin into HDB3 pseudo-ternary form for transmission over a 2.048 Mbit PCM link in accordance with CCITT Recommendation G.703. The two TXD outputs represent the HDB3 data in pseudo-ternary form. They are always low during the high half cycle of CLK, but may be high or low during the low half cycle. The Q output represents the D input but delayed by one period. Fig. 5 shows the timing diagram of this macrocell.

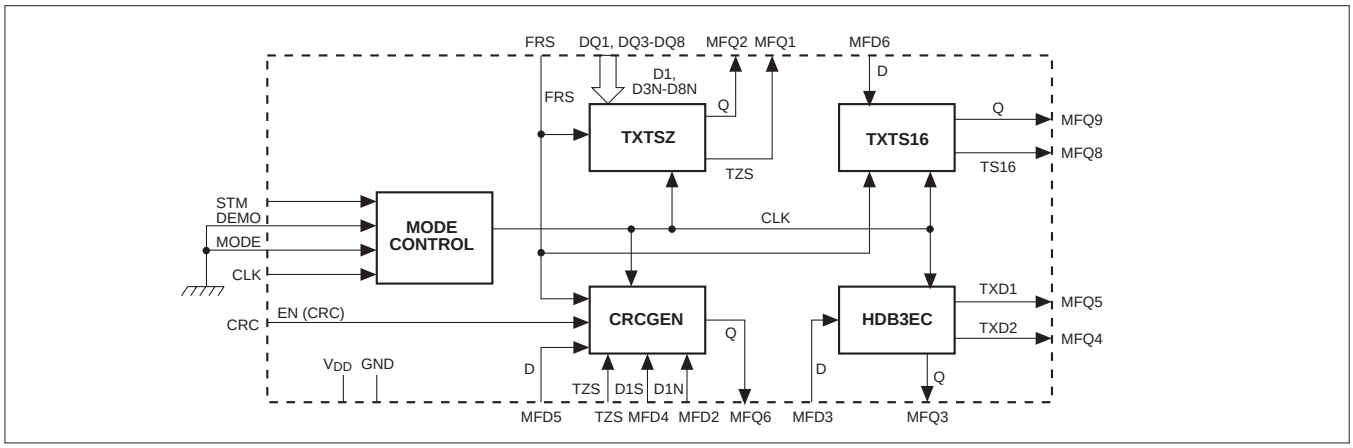


Figure 2: TX1 Individual Transmit mode functional diagram

Mode Name	MODE input	DEMO input	CRC input	STM input	Mode description
TX1	0	0	0/1	0	MV 1403 is configured as individual Transmit PCM macrocells
TX2	0	1	0/1	0	MV1403 is configured as a PCM Transmitter demonstration, using the Transmit macrocells
RX1	1	0	0/1	0	MV1403 is configured as individual Receive PCM macrocells
RX2	1	1	0/1	0	MV1403 is configured as a PCM Receiver demonstration, using the Receive macrocells
TX1/2	0	0/1	0	0	CRC generation mode of the CRCGEN macrocell is disabled
TX1/2	0	0/1	1	0	CRC generation mode of the CRCGEN macrocell is enabled
RX1/2	1	0/1	0	0	CRC mode of the RXTSZ macrocell is disabled
RX1/2	1	0/1	1	0	CRC mode of the RXTSZ macrocell is enabled
-	X	X	X	1	MV1403 is configured in device test mode. This mode should not be used for normal operation

Table 1: Operational modes of the MV1403

	CRC Multiframe															
	Sub-Multiframe 1 (SMF1)								**Sub-Multiframe 2 (SMF2)**							
Frame number	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Bit one of timeslot zero	C1	0	C2	0	C3	1	C4	0	C1	1	C2	1	C3	D1S	C4	D1N

NOTES:
1. C1, C2, C3, C4 are the bits of the CRC word.
2. 001011 is the CRC Multiframe Alignment Signal (MAS).
3. Even numbered frames are denoted Sync frames; odd numbered frames are denoted non-sync frames.

Table 2: Structure of the CCITT CRC Multiframe

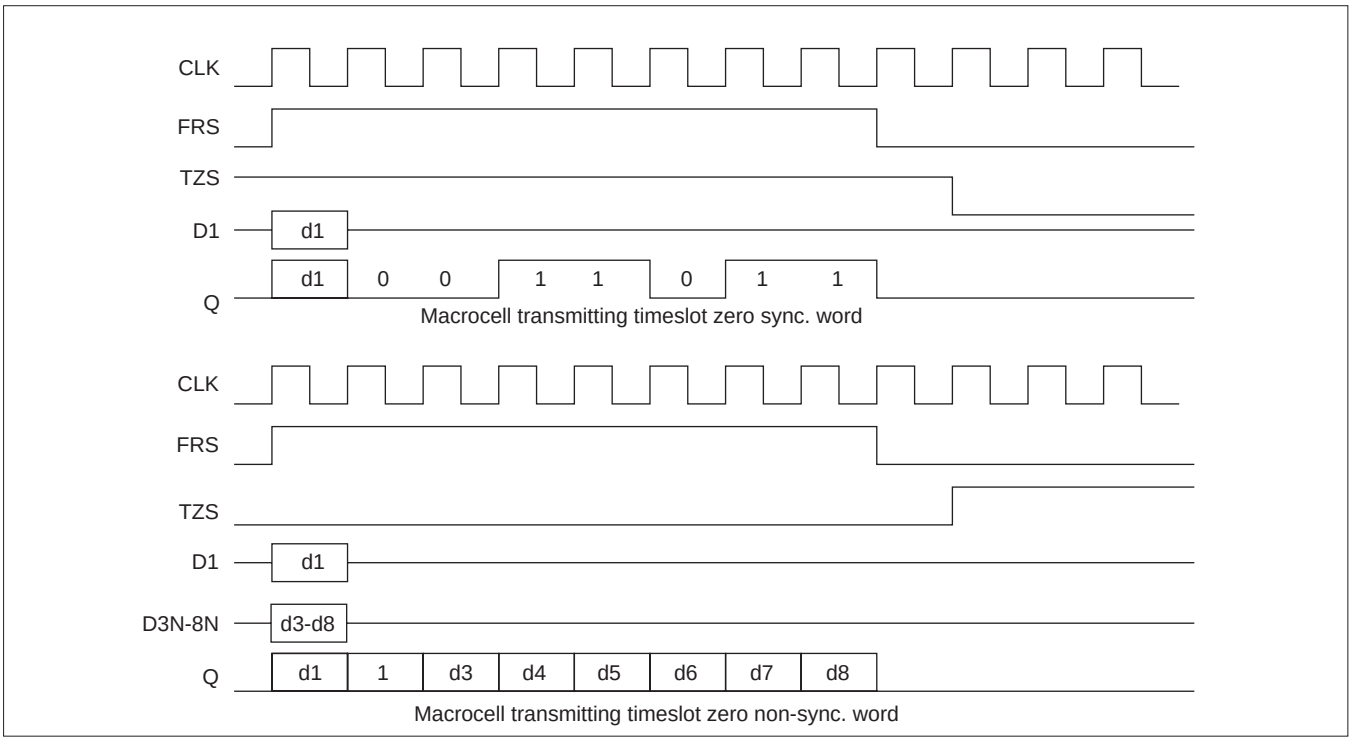


Figure 3: Timeslot zero transmitter timing

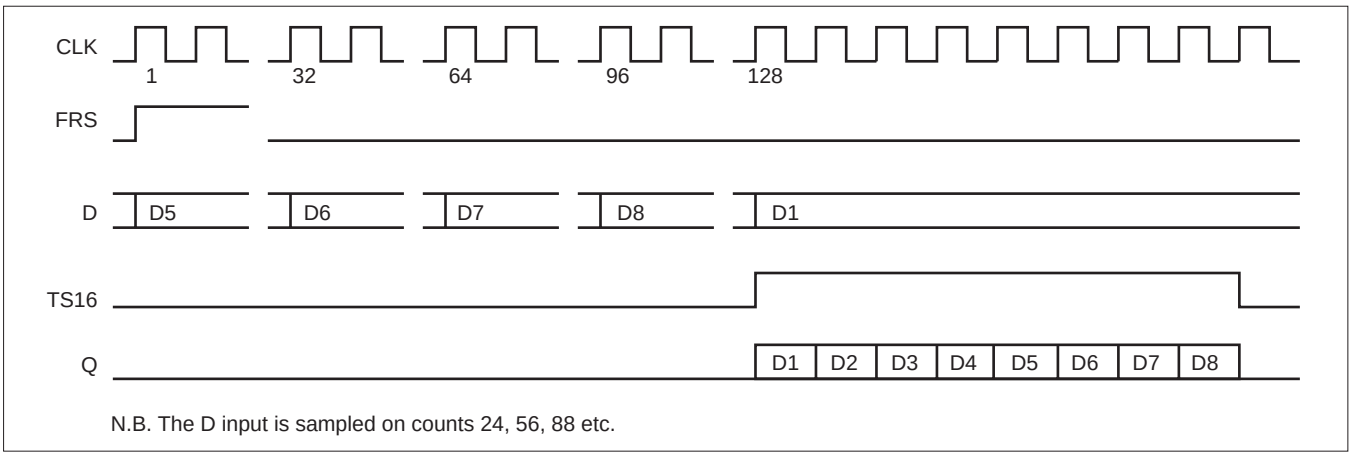


Figure 4: Timeslot sixteen transmitter timing

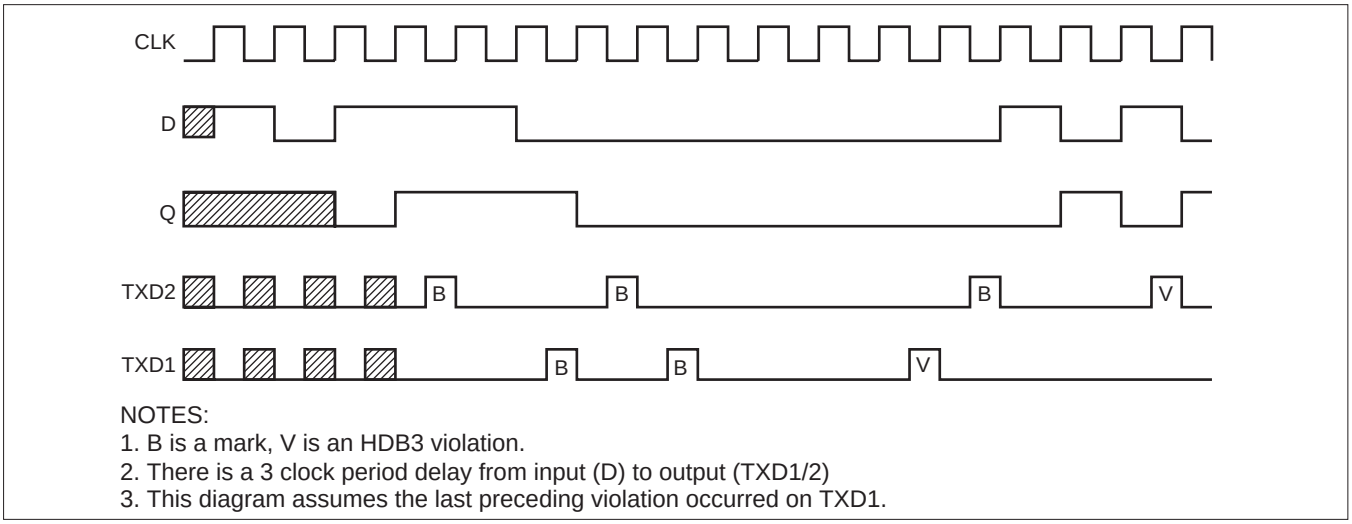


Figure 5: HDB3 encoder timing

TRANSMIT DEMONSTRATION MODE, TX2

Transmit demonstration mode (MODE =0, DEMO= I) uses the four transmitter macrocells connected together internally, to demonstrate how they may be utilised to perform the common channel signalling and error detection functions of a 2.048 Mbit 30 channel PCM transmitter. The functional diagram of the MV1403 in this mode is now as shown in Fig. 6. Again all four macrocells are synchronised to a common 2.048MHz clock with frame synchronisation achieved from the FRS input.

The Timeslot Zero transmitter alternately outputs sync words and non-sync words, during timeslot zero, denoting which by its TZS output. The user data bits of the nonsync word (D3N-D8N) are available as parallel data inputs. The Timeslot Zero data is used as one of the inputs to the transmission multiplexer.

The Timeslot Sixteen transmitter takes in the continuous 64kbit data stream from its D input and outputs this in 8 bit bursts during timeslot 16. This data along with the TS16 frame marker are also used as inputs to the transmission multiplexer, TMUX.

The transmission multiplexer forms a single PCM data stream at its Q output by multiplexing the timeslot zero and timeslot 16 data with the remaining 30 channels (timeslots 1-15 and 17-31) of voice data. This is controlled by the two frame marker inputs to the multiplexer, FRS and TS16.

The output from TMUX is input to the Cyclic Redundancy Check Generator and HDB3 Encoder macrocells.

When in CRC mode (EN=1), the CRC Generator macrocell performs its CRC procedure on this incoming data stream. In non-CRC mode, this macrocell uses its two data inputs, D1S and D1N, along with the timing input, TZS, to determine its output. However, in CRC mode the output consists ol the CRC word data bits interleaved with the CRC multiframe alignment word and the two user data bits, D1S and D1N, as previously displayed in Table 2. In either case, the output data is input directly to the international spare bit input of the Timeslot Zero Transmitter. The TZS input of the CRC generator is connected directly to the TZS output of the Timeslot Zero Transmitter.

The output data from the transmission multiplexer is also input to the HDB3 Encoder macrocell. This macrocell converts the incoming NRZ data into pseudo-ternary HDB3 transmission code, ensuring adequate clock recovery at the receiver. This data is output on the TXD1 and TXD2 output pins. The Q output of the HDB3 Encoder macrocell is a single period delayed version of its D input and as such allows the output from the transmission multiplexer to be observed.

Fig. 6 shows that all of the intemal connections except the output from TMUX, are also available as outputs from the MV1403, allowing the interaction of the rnacrocells to be observed.

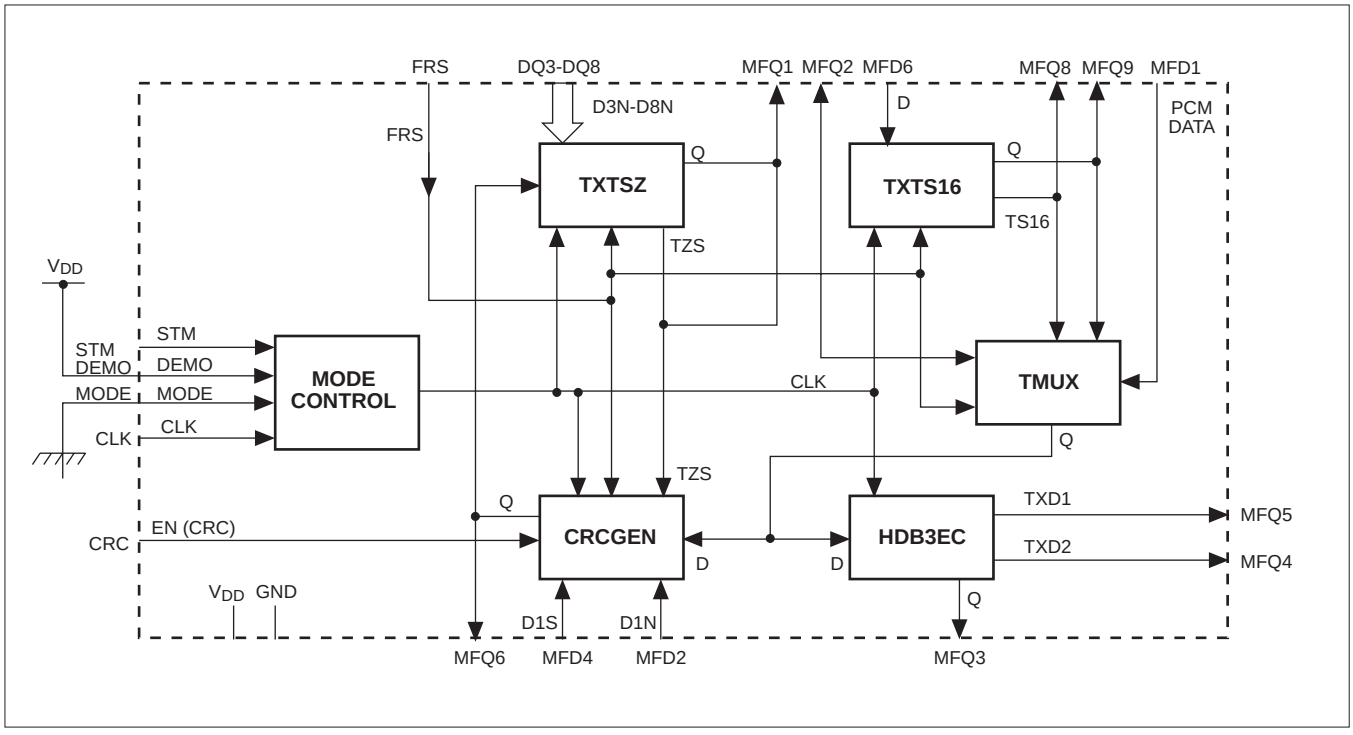


Figure 6: TX2 Transmit demonstration mode functional diagram

INDIVIDUAL RECEIVE MODE, RX1

In this mode (MODE = 1, DEMO = 0) the MV1403 allows access to the four receiver macrocells (HDB3DC, RXTSZ, RXTS16 and CRCCHK) individually. The functional diagram for the MV1403 in RX1 mode is shown in Fig. 7. The only common connection between the macrocells is the 2.048MHz clock used to synchronise the four macrocells. The function of each individual macrocell is now described separately.

High Density Bipolar (HDB3) Decoder

The HDB3 decoder macrocell decodes the HDB3 pseudo-ternary input data on its inputs, RXD1 and RXD2, into NRZ form to be output on a This process is carried out in accordance with CCITT Recommendation G. 703. In addition the macrocell provides two alarm outputs, DV and LIA and a clock recovery output, CDR.

The first of these, DV, is used to signal that a double polarity violation has occurred on one of the pseudo-ternary inputs, whilst the second, LIA (Loss of Input Alarm), signals that eleven consecutive zeros have been received on the inputs. The CDR output is provided to assist regeneration of the 2.048MHz clock. This output is essentially just a logical 'OR' function of the two RXD inputs.

Since either a regenerated clock from the input data or a clock local to the PCM receiver may be used to synchronise the receiver, the two input signals cannot be guaranteed to straddle a rising clock edge and as such the two inputs were made asynchronous by the use of set-reset type latches before the first synchronous storage elements on the inputs.

However, to ensure correct operation of the macrocell the rising edge of either of the RXD inputs should not occur within 50ns of the rising edge of CLK. The timing diagram for this macrocell is shown in Fig. 8.

Timeslot Zero Receiver

This macrocell is principally responsible for searching for and locking on to the Frame Alignment Signal (FAS) present in timeslot zero of the incoming data stream on the D input. This process is carried out in accordance with the loss and recovery of frame alignment strategy described in CCITT Recommendation G.732. When frame alignment has been achieved this macrocell outputs various timing reference signals for use by the other macrocells and external circuitry.

The most important reference signal is the TSZ (Timeslot Zero) output, which is equivalent to the FRS input signal required by the transmitter macrocells. It is an 8 clock period long active high pulse masking Timeslot Zero, allowing the other macrocells to achieve frame alignment. This output will free run when frame alignment is lost. The second timing output is TZS (Timeslot Zero Sync. frame). This 4kHz signal changes state once per frame, one period after the end of Timeslot Zero to identify sync and non sync frames. The TZS output is high during Timeslot Zero of sync frames.

Two timing outputs, $\overline{CCR}$ (Channel Reset) and CK8, are not used by the other macrocells but may be used by external circuitry. $\overline{CCR}$ is a low going pulse, one period wide, occurring immediately after each timeslot zero sync frame. CK8 is an 8kHz signal going low at the end of bit 7 in each timeslot zero and high at the end of bit 7 in each timeslot sixteen. The TZS, CK8 and $\overline{CCR}$ outputs also free run when frame alignment is lost.

Two alarm outputs are provided to signal errors in the incoming data stream. The first of these, is an error alarm, ER, which goes high for one frame following the frame in which a Timeslot Zero sync word, containing a corrupted alignment pattern, has been received. This alarm is only active whilst the receiver is in sync. Note that three consecutive errors of this type will put the receiver out of sync. Thus the second alarm output, SA (Sync. Alarm), goes high when the receiver is out of sync. In additon to the frame synchronisation process, the Timeslot Zero Receiver is also responsible for extracting the user data bits of non-sync words and the two international spare bits. The former of these are accessed via the parallel outputs Q3N-Q8N. The third bit of non-sync words (Q3N) is used as the remote alarm bit from the transmitter and a third alarm output RAI (Remote Alarm Indication), is derived from this bit. This alarm is a persistence checked version of Q3N and when the receiver is in sync, this alarm goes high when two consecutive (Q3N bits have been received as high.

In order to extract the international spare bits of Timeslot Zero, the macrocell must be in sync with CRC mode correctly enabled or disabled. This is done using the M input with a logic 'high' on this pin putting the macrocell in CRC mode.

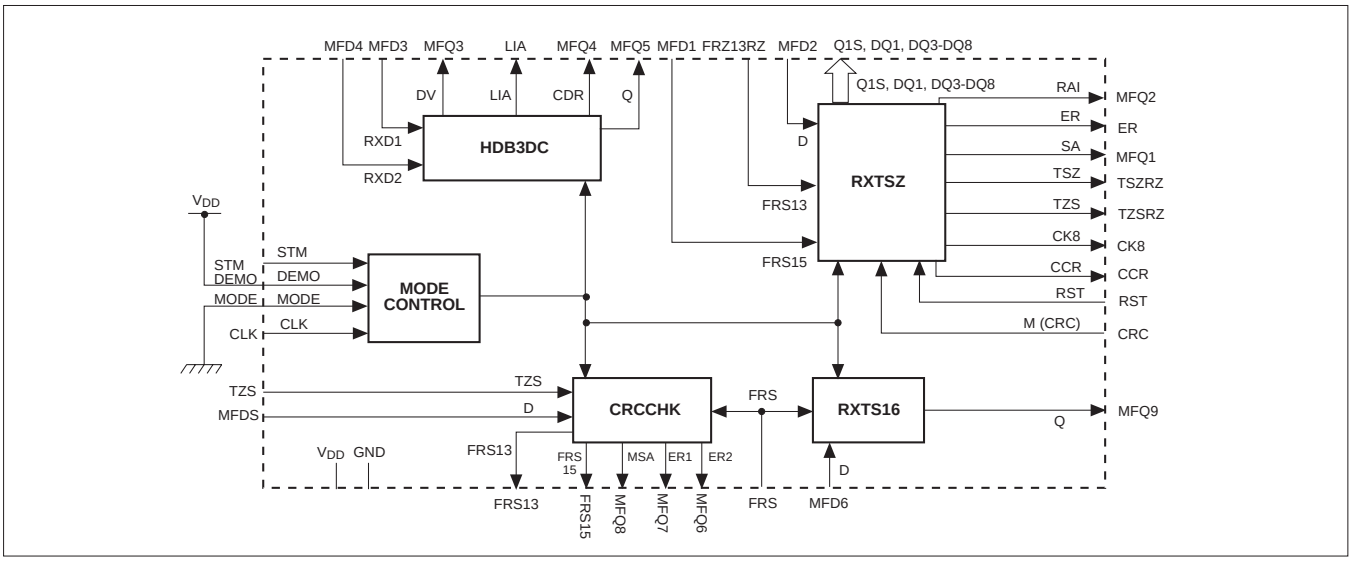
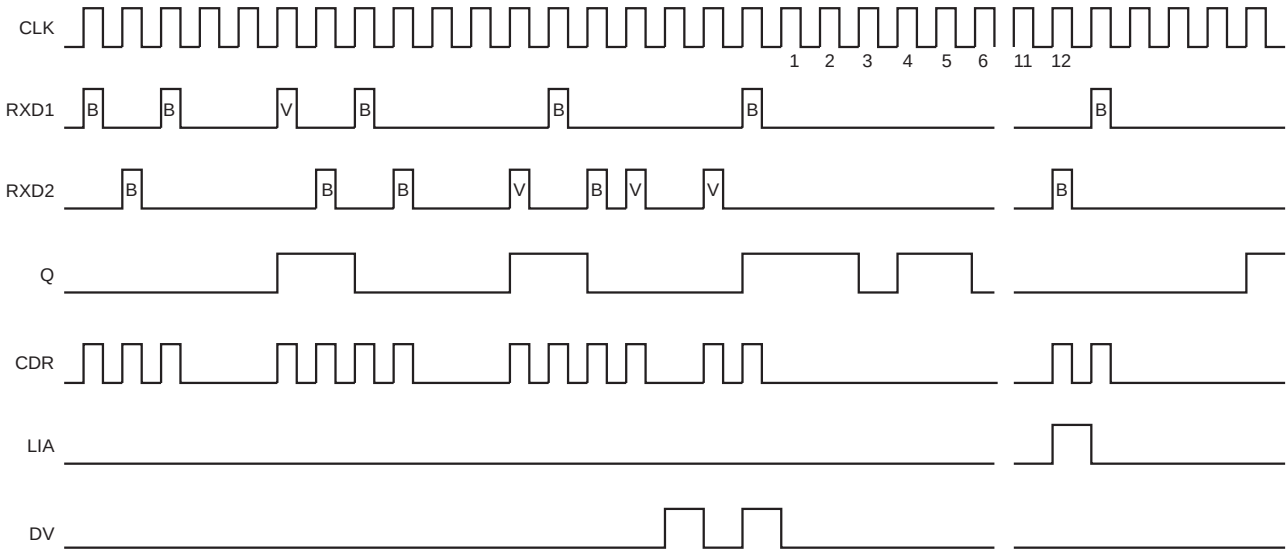


Figure 7: RX1 individual receive mode functional diagram



NOTES:
1. B is a mark, V is a HDB3 violation.
2. There is a 5 period delay from input (RXD1/RXD2) to output (Q).
3. This diagram assumes that the rising edges of the RXD inputs occur at least 50ns before the rising edge of CLK.

Figure 8: HDB3 decoder timing - macrocell decoding HDB3 data and detecting errors

When in non CRC mode the international spare bit outputs, Q1S and Q1N, represent data extracted from the bit position of all sync frames and non-sync. frames respectively. If CRC mode is enabled, these outputs now represent data extracted from the bit 1 position of frames 13 and 15 respectively of the CRC multiframe structure. In order to accomplish this, two timing inputs, FRS13 and FRS15, are required. These inputs are required to be high during bit 8 of the appropriate frame, low during bit 8 of any other non-sync frame and any state elsewhere. A final input to this macrocell, RST, may be used to reset the synchronisation process, putting the macrocell out of sync. Timing diagrams for the Timeslot Zero P(eceiver macrocell are shown in Fig. 10.

Timeslot Sixteen Receiver

The Timeslot Sixteen Receiver macrocell extracts the 8 bits of common channel signalling data present in Timeslot 16 of successive frames of PCM data input on D. This 2.048Mbit input data burst is stored and output as a continuous 64kbit data stream. A single timing input, FRS, also common to the CRCCHK macrocell, is required, this input being an 8 bit pulse masking Timeslot Zero. Fig. 9 shows the timing of this macrocell.

Cyclic Redundancy Checker

The Cyclic Redundancy Checker macrocell (CRCCHK) performs a cyclic redundancy check procedure on the received data in accordance with CCITT Recommendation G.704, this procedure being performed on the data input on its D input pin. The macrocell also extracts the first bit of each Timeslot Zero (the first bit of each frame) and searches for the CRC Multiframe Alignment Signal (MAS) in the bits from non-sync frames.

When the MAS has been found the macrocell synchronises to it. This process requires two timing inputs, FRS and TZS. The FRS input must be high only during timeslot zero and TZS must be high during timeslot zero of sync frames.

The macrocell generates CRC words from the input data and extracts the CRC bits being received in the first bit of sync frames. Each generated CRC word is compared with the CRC word received in the next sub-multiframe. Associated with this process are three alarm outputs, MSA, ER1 and ER2. The MSA (Multiframe Sync Alarm) output indicates whether multiframe synchronisation has occured. It is high whilst the macrocell is out of sync, and goes low after the beginning of frame 11 in which a correct alignment pattern has been received. The two error outputs, ER1 and ER2 indicate that CRC errors were detected in submultiframes 1 and 2 respectively. These two outputs can only change state on the first rising clock edge after the first bit of frames 0 and 8 respectively.

When in CRC multiframe alignment, the macrocell also produces two timing outputs, FRS13 and FRS15, to reference the positions of frames 13 and 15. These signals may be used to allow the Timeslot Zero Receiver macrocell to extract the international spare bits of these frames.

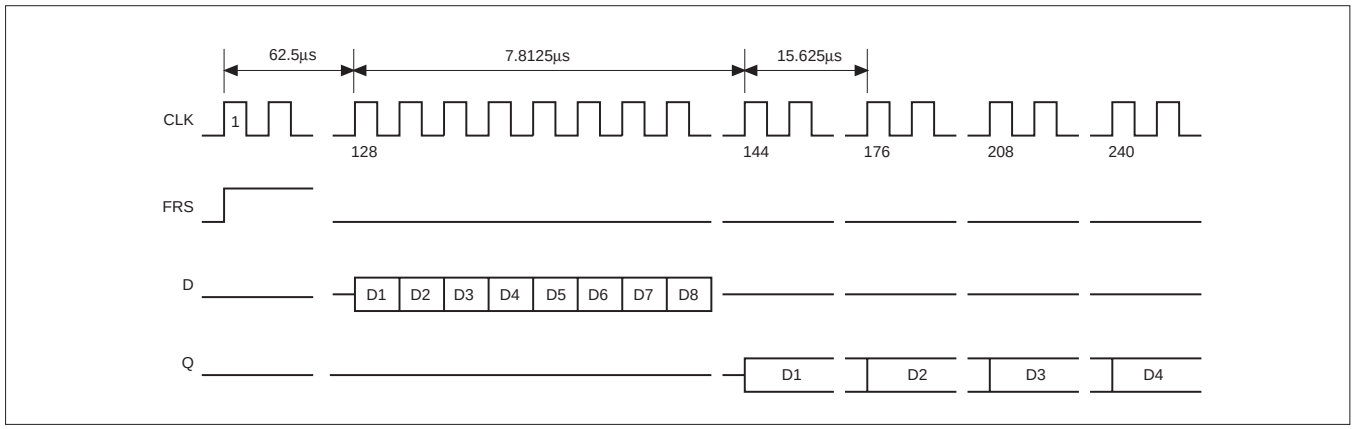


Figure 9: Timeslot sixteen receiver timing

RECEIVE DEMONSTRATION MODE, RX2

In the last mode (MODE = 1, DEMO = 1) the four receiver macrocells are connected together internally to demonstrate how they may be utilised to perform the required functions of a 2.048 MBit PCM receiver. The functional diagram of the MV1403 will now be as shown in Fig. 11.

The received pseudo-ternary HDB3 data is input to the HDB3 Decoder macrocell, which decodes this data and outputs it to the other three macrocells and external circuitry, as well as raising appropriate alarms as previously described for the individual receive mode.

The Timeslot Zero Receiver then synchronises itself to the Frame Alignment Signal present in this data stream and produces various timing outputs tor use by the remaining two receiver macrocells and external circuitry. In addition this macrocell also raises appropriate alarms as required.

The data being output by the HDB3 decoder is used as the D input to the Timeslot 16 Receiver macrocell which also uses the Timeslot Zero Receiver's TSZ output as its FRS timing input. From this the macrocell determines the position of timeslot 16 and extracts the 8 bits of signalling data from this timeslot. This data is then converted into a continuous 64kbit output data stream.

The Cyclic Redundancy Checker macrocell uses the HDB3 Decoder's output data and the Timeslot Zero Receivers timing outputs TSZ and TZS as its D, FRS and TZS inputs respectively. From this information the macrocell synchronises itself to the CRC multiframe alignment signal and performs its CRC check procedure on the incoming data. Its two timing outputs, FRS13 and FRS15, are input to the Timeslot Zero Receiver to allow it to extract the international spare bits of the CRC multiframe.

In non CRC mode, the Cyclic Redundancy Checker's error outputs are disabled by the alarm gating circuitry. When in CRC mode, this circuitry will also disable the ER1 and ER2 alarms whilst the macrocell is out of multiframe alignment.

In addition to the required outputs, all the internal timing signals are also available as outputs from the MV1403, allowing the interaction of the macrocells to be observed.

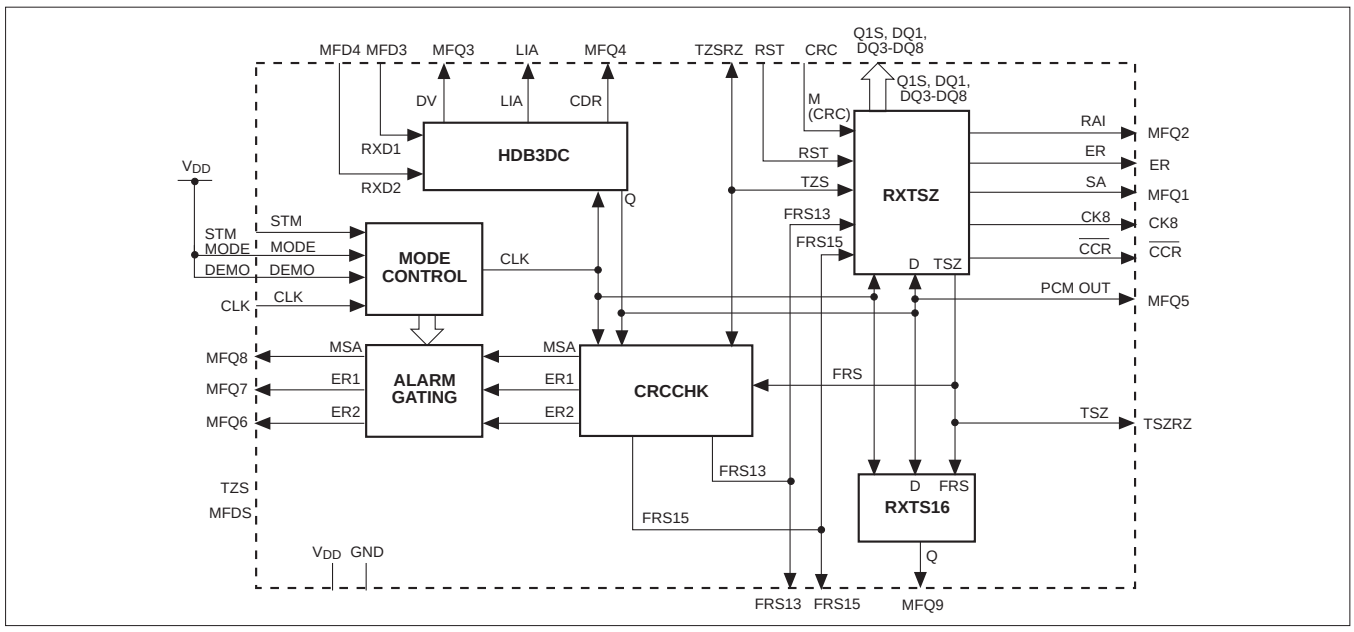
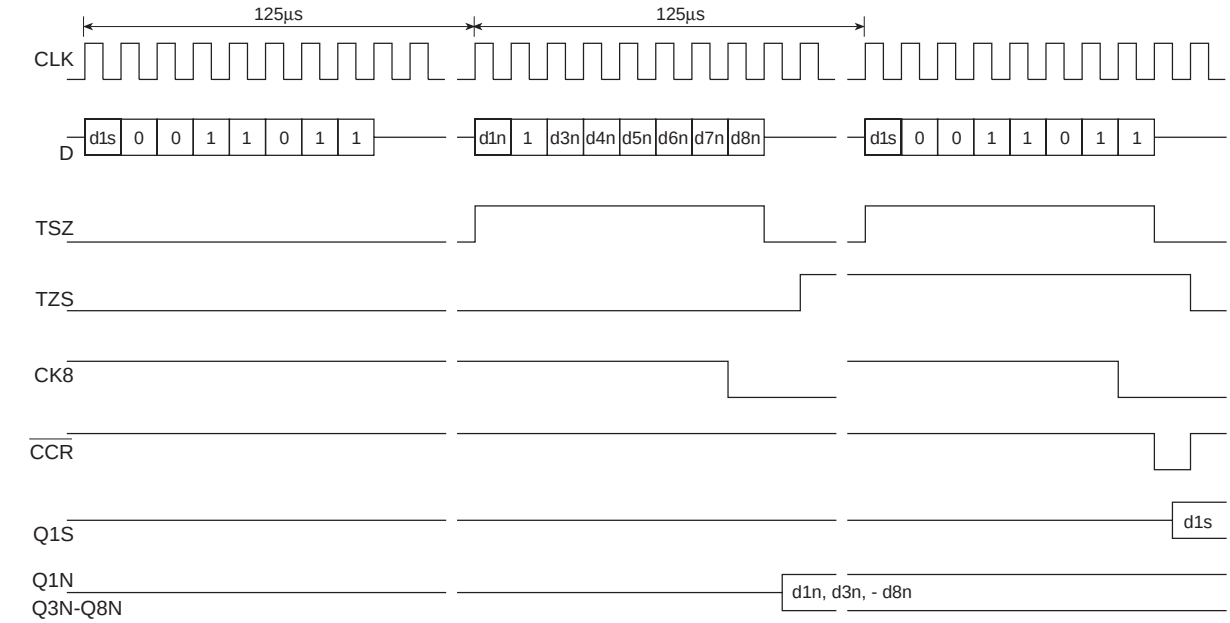
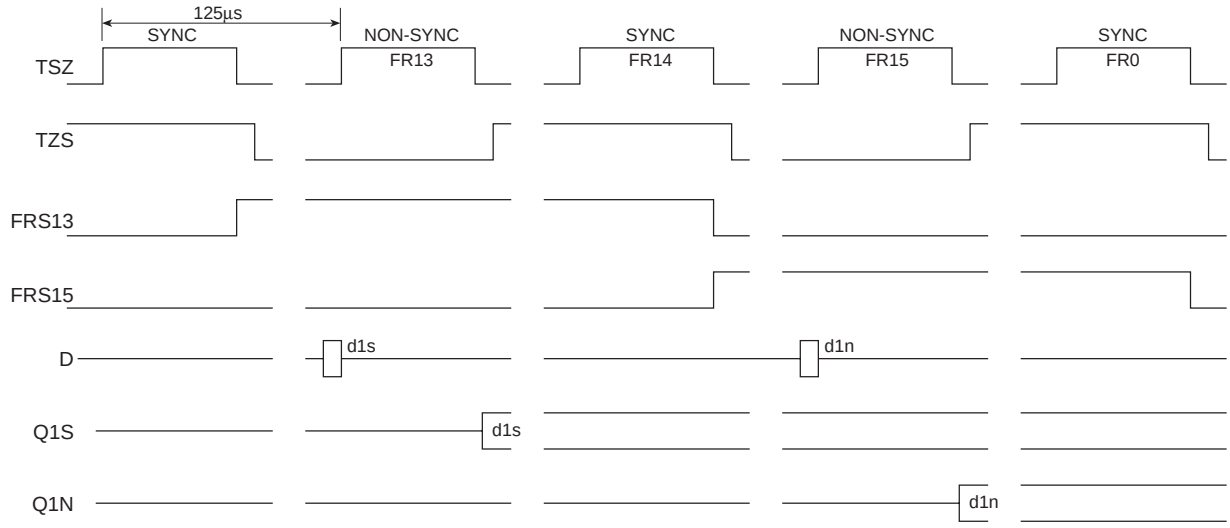


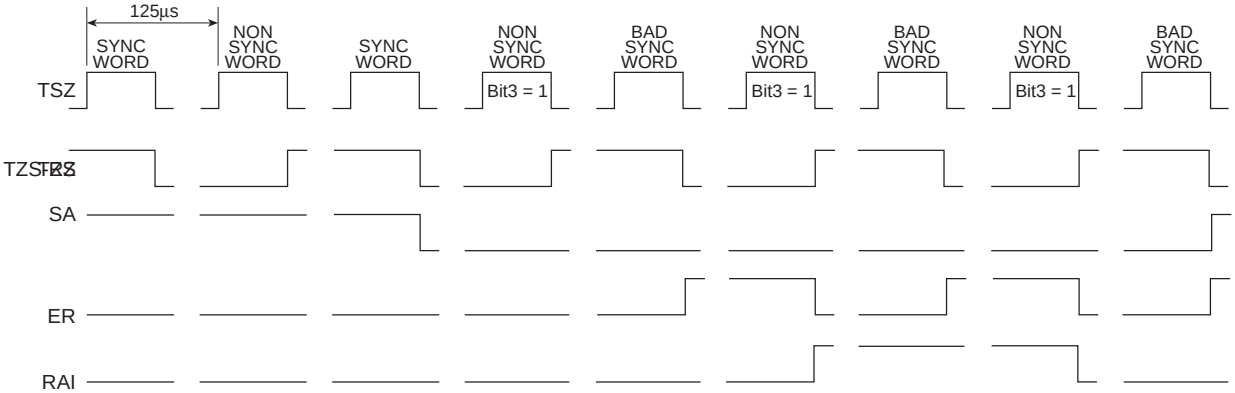
Figure 11: RX2 receive demonstration mode functional diagram



Macrocell first coming into sync., generating timing signals (non-CRC mode)



Macrocell extracting Signalling Data (CRC mode)



Macrocell synchronisation process

Figure 10: Timeslot zero receiver timing

PIN DESCRIPTIONS

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
$V_{DD}1$			GLOBAL	Digital supply voltage. 5V (Note 2)
ER	2	2	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Sync Word Error Output (ER). This flag goes high for one frame immediately after detection of a bad timeslot zero sync word, whilst the macrocell is in sync. Three consecutive errors of this type will put the receiver out of sync. The last ER pulse of this sequence will be longer than 256 periods if a valid sync word is detected during the pulse.
MFQ1	3	3	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Synchronisation Alarm Output (SA). This error flag goes high when the macrocell is out of sync and only changes state at the end of a sync frame timeslot zero.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Timeslot Zero Sync frame marker (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of timeslot one, bit 2 of every frame.
MFQ2	4	4	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Remote Alarm Indication Output (RAI) This is a persistence checked version of the Q3N output. When RXTSZ is in sync, this output goes high if the current and previous timeslot zero bit 3 of non-sync frames are both high. This output changes state at bit 1, timeslot 1 of non-sync frames. When the macrocell is out of sync this output is forced low in the non-sync frame following the last bad sync frame, and is held low until the macrocell comes back into sync.
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Output (Q). The sync word and signalling data word appear here in 8 bit bursts during timeslot zero. Bit 1 appears immediately after the rising edges of CLK and FRS. This output is low during all timeslots except timeslot zero.
DQ8 DQ7 DQ6 DQ5 DQ4 DQ3	5 6 7 8 9 10	5 6 7 8 9 10	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Outputs (Q8N-Q3N). These outputs are extracted from bits 8-3 of timeslot zero during non-sync frames respectively. These outputs change at the start of bit 1, timeslot 1 of non-sync frames .
			TX	Timeslot Zero Transmitter (TXTSZ) Macrocell Data Inputs (D8N-D3N). These data inputs are inserted into bits 8-3 of timeslot zero during non-sync frames respectively. This data must be set up prior to the rising edge of FRS.
DQ1	11	11	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1 N). With CRC = 0, this output latches data from bit I, timeslot zero of non-sync frames. The output changes at the beginning of bit l, timeslot 1 of non-sync frames. With CRC=1, this output latches data from bit 1 of frame 15 of the CRC multiframe.
			TX1 .	Timeslot Zero Transmitter (TXTSZ) Macrocell - Data Input (D1). The data on this pin is inserted into the International spare bit (bit 1, timeslot zero of both sync and non-sync frames), and must be set up prior to the rising edge of FRS.
			TX2	This pin is unused since the Dl input of the Timeslot Zero Transmitter is connected internally to the Q output of the CRC Generator.
Q1S	12	12	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Output (Q1S). With CRC = 0, this output latches data from bit 1, timeslot zero of sync frames. The output changes at the beginning of bit 1, timeslot 1 of sync frames. With CRC = 1, this output latches data from bit 1 of frame 13 of the CRC multiframe.
$V_{DD}2$	13	-	GLOBAL	Digital supply voltage. 5V (Note 2)
GND1	14	13	GLOBAL	Digital ground. 0V (Note 2)
LIA	15	14	RX	HDB3 Decoder (HDB3DC) Macrocell - Loss of Input Alarm Output (LIA). This alarm output goes high after 11 consecutive zeros have been detected on the HDB3 inputs. It is reset on detection of a mark (1) on either HDB3 input.

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
MFQ3	16	15	RX	HDB3 Decoder (HDB3DC) Macrocell - Double Violation Alarm Output (DV). This pin goes high one period after detection of a double violation on either of the HDB3 inputs.
			TX	HDB3 Encoder (HDB3EC) Macrocell - Data Output (a). This output is a single period delayed version of this macrocells D input.
MFQ4	17	16	RX	HDB3 Decoder (HDB3DC) Macrocell - Clock Regeneration Output (CDR). This output is a logical 'OR' function of the two HDB3 inputs and may be used by external clock regeneration circuitry. This signal has a variable mark-to space ratio.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 2 (TXD2). This output is always low during the high half cycle of clock and is only high the low half cycle if a mark is to be output.
MFQ5	18	17	RX	HDB3 Decoder (HDB3DC) Macrocell - HDB3 Decoded Output (Q). This output is the HDB3 inputs decoded back to NRZ form.
			TX	HDB3 Encoder (HDB3EC) Macrocell - HDB3 Encoded Output 1 (TXD1). As TXD2 (MFQ4).
FRS13RZ	19	18	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 13 Marker Input (FRS13). In CRC mode, this input should be high during bit 8, Frame 13 of the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS13 input ol the Timeslot Zero Receiver is connected internally to the FRS13 output of the CRC Checker.
MFD1	20	19	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Frame 15 Marker input (FRS15). In CRC mode, this input should be high during bit 8, Frame 15 ot the CRC multiframe and low during bit 8 of all other non-sync frames.
			RX2	This pin is unused since the FRS15 input of the Timeslot Zero Receiver is connected internally to the FRS15 output of the CRC Checker.
			TX1	No Connection.
			TX2	PCM Voice Channel Input. In Transmit Demonstration mode this pin is used as the serial data input to the Transmission Multiplexer.
MFD2	21	20	RX1	Timeslot Zero Receiver (RXTSZ) Macrocell - Data Input (D). This pin is used to input the 2.048 Mbit data stream to this macrocell.
			RX2	This pin is unused since the D input of the Timeslot Zero Receiver is connected internally to the Q output of the HDB3 Decoder.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1 N). This pin is used to input the data to be inserted into bit 1 of non sync frames (CRC = 0) or bit 1 of frame 15 of the CRC multiframe (CRC = 1).
MFD3	22	21	RX	HDB3 Decoder (HDB3EC) Macrocell - Data Input 1 (RXD1). This input latches the incoming HDB3 encoded data and is rising edge sensitive. The rising edge of this input should not occur within 50 ns of the rising edge of CLK.
			TX1	HDB3 Encoder (HDB3EC) Macrocell - Data Input (D). This pin is used to input NRZ data for conversion into pseudo ternary HDB3 format.
			TX2	This pin is unused since the D input of the HDB3 Encoder is connected internally to the Q output of the Transmission Multiplexer.
MFD4	23	22	RX	HDB3 Decoder (HDB3DC) Macrocell - Data Input 2 (RXD2). As RXD1 (MFD3)
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Signalling Data Input (D1S). This pin is used to input the data to be inserted into bit 1 of sync frames (CRC = 0) or bit 1 of frame 13 of CRC multiframe (CRC = 1).
V_{DD3} V_{DD}	24 _	- 23	GLOBAL	Digital supply voltage. 5V (Note 2)

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
GND2	25		GLOBAL	Digital ground. 0V (Note 2)
DEMO	26	24	GLOBAL	Demonstration pin. A logic high on this pin puts the MV1403 into demonstration mode, RX2 or TX2 with all the transmit or receive macrocells connected together internally. A low on this pin allows access to the macrocells individually (ie. RX1 or TX1 mode).
MODE	27	25	GLOBAL	Transmit/Receive Mode pin. A logic high on this pin places the MV1403 in Receive mode RX1 or RX2. A low places it in Transmit mode TX1 or TX2
CLK	28	26	GLOBAL	2.048MHz Master Clock input.
STM	29	27	GLOBAL	Scan Path Test Mode pin. A logic high on this pin places the MV1403 in scan test mode. For normal operation this pin should be tied low.
P	30	28	GLOBAL	Scan Test Data input. In Scan Path Test Mode, this pin is used as the input to the scan path.
CRC	31	29	GLOBAL	CRC Mode pin. This pin is used as the CRC mode input to the CRCGEN (EN input) or RXTSZ (M input) macrocells. A logic high on this pin will put the MV1403 into Cyclic Redundancy Check mode.
MFD5	32	30	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Data Input (D). This pin is used as the 2.048Mbit serial data input to this macrocell.
			RX2	This pin is unused since the D input ol the CRC Checker is connected internally to the a output of the HDB3 Decoder.
			TX1	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Input (D). This pin is the 2.048 Mbit data input to this macrocell.
			TX2	This pin is unused since the D input to the CRC Generator is connected internally to the a output of the Transmission Multiplexer
FRS	33	31	RX1	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input to the Timeslot Sixteen Receiver (RXTS16) and Cyclic Redundancy Checker (CRCCHK) macrocells. It is required to be high only during timeslot zero of each frame.
			RX2	This pin is unused since the FRS inputs to the CRC Checker and Timeslot 16 Receiver are connected internally to the TSZ output of the Timeslot Zero Receiver .
			TX	Frame Sync Input (FRS). This pin is the 8kHz timeslot zero frame marker input. It is required to be high only during timeslot zero of each frame.
TZS	34	32	RX1	Cyclic Redundancy Checker (CRCCHK) Macrocell - Timeslot Zero Sync Frame Marker Input (TZS). This 4KHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
			RX2	This pin is unused since the TZS input of the CRC Checker is connected internally to the TZS output of the Timeslot Zero Receiver.
			TX1 .	Cyclic Redundancy Check Generator (CRCGEN) Macrocell Timeslot Zero Sync Frame Marker Input (TZS). This 4kHz input is required to be high during timeslot zero of sync frames and change at the beginning of bit 2, timeslot 1 of every frame.
MFD6	35	33	RX1	Timeslot Sixteen Receiver (RXTS16) Macrocell - 2.048Mbit Serial Data Input (D). The 8 bits of signalling data in timeslot t6 are extracted from this input during timeslot 16.
			RX2	This pin is unused since the D input of the Timeslot 16 Receiver is connected intermally to the (; output of the HDB3 Decoder.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - 64kbit Signalling Data Input (D). The continuous stream of data to be output as 8 bit bursts during timeslot 16 is input on this pin.
GND3	36		GLOBAL	Digital ground,OV. (Note 2)

PIN DESCRIPTIONS (continued)

Symbol	Pin No.		Mode name (see note 1)	Pin name and description
	DP48	HP44		
RST	37	34	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Reset Input (RST). A logic high on this pin will reset the state machine of this macrocell, forcing the macrocell out of frame alignment. Due to the 100kΩ pull-up resistors on all the inputs, this pin should be tied low when not in use.
MFQ6	38	35	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 2 Error Alarm Output (ER2). A logic high on this output indicates the detection of a CRC error in sub-multiframe 2.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Data Output (Q). This pin is used to output the data to be inserted into bit 1, timeslot 0.
MFQ7	39	36	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Sub-multiframe 1 Error Alarm Output (ER1). A logic high on this output indicates the detection of a CRC error in sub-multiframe 1.
			TX	Cyclic Redundancy Check Generator (CRCGEN) Macrocell - Scan Test Data Output (STQ). In scan test mode, this pin is the scan path output of this macrocell.
MFQ8	40	37	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Multiframe Sync Alarm Output (MSA). A logic high on this output denotes that the macrocell is out of CRC multiframe alignment.
			TX	Timeslot Sixteen Transminer (TXTS16) Macrocell - Timeslot 16 Marker Output (TS16). This output is high only during timeslot 16.
FRS15	41	38	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 15 Marker Output (FRS15). When the macrocell is in CRC multiframe alignment, this output is high during frame 15 and low during all other non-sync frames.
FRS13	42	39	RX	Cyclic Redundancy Checker (CRCCHK) Macrocell - Frame 13 Marker Output (FRS13). When the macrocell is in CRC multiframe alignment, this output is high during frame 13 and low during all other non-sync frames.
M FQ9	43	40	RX	Timeslot Sixteen Receiver (RXTS16) Macrocell - Signalling Data Output (Q). This pin is used to output the 8 bits of signalling data extracted from timeslot 16 as a continuous 64kbit data stream.
			TX	Timeslot Sixteen Transmitter (TXTS16) Macrocell - Signalling Data Output (Q). The 8 bit data bursts produced by this macrocell are output at 2.048MHz on this pin during timeslot 16. This output is low at all other times.
TSZRZ	44	41	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Marker Output (TSZ). This output goes high for the 8 periods of timeslot zero and is low at all other times.
TZSRZ	45	42	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Timeslot Zero Sync Frame Marker Output (TZS). This output is high during timeslot zero of sync frames and changes state at the beginning of bit 2, timeslot 1 of every frame.
CK8	46	43	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - 8kHz Clock Output (CK8). This output goes low at the end of bit 7, timeslot zero and high at the end of bit 7, timeslot 16.
$\overline{\text{CCR}}$	47	44	RX	Timeslot Zero Receiver (RXTSZ) Macrocell - Channel Reset Output ($\overline{\text{CCR}}$). This output pulses low for a single period during bit 1, timeslot 1 of sync frames.
GND4 GND2	48 1		GLOBAL	Digital ground. 0V (Note 2).

NOTES
1. TX refers to TX1 and TX2 modes. RX reters to RX1 and RX2 modes. GLOBAL refers to all modes.
2. All the V_{DD} and GND pins of the 48-pin device, and two GND pins of the 44-pin device are connected together internally and as such there is no need to connect up all these supplies. However, it is recommended that all supply pins are connected to facilitate supply decoupling.
3. Since the device is intended as a demonstrator allowing access to the individual macrocells, 100kΩ pull-up resistors have been included on all the input pins to prevent any unconnected inputs from floating.

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated)
Supply Voltage V_{DD} = 5V ± 0 .V, Ambient Temperature T_{amb} = 0 to 70°C

STATIC CHARACTERISTICS

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
Low level input voltage	V_{IL}			0.8	V	
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level output voltage	V_{OL}	0		0.4	V	I_{SINK} = 10mA
High level output voltage	V_{OH}	2.4		V_{DD}	V	I_{SOURCE} = 5mA
Input leakage current	I_{IL}	-20		-200	µA	$V_{IN} = V_{SS}$
		-10		+10	µA	$V_{IN} = V_{DD}$
Supply current	I_{CC}		1.5	3.0	mA	All outputs unloaded
Input capacitance	C_{IN}		5		pF	
Output capacitance	C_{OUT}		5		pF	

DYNAMIC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min	Typ	Max		
Clock						
Clock frequency	f_{CLK}		2.048		MHz	
Clock rise time	t_{CR}			20	ns	See Fig. 12
Clock high time	t_{CH}	150			ns	See Fig. 12
Clock fall time	t_{CF}			20	ns	See Fig. 12
Clock low time	t_{CL}	150			ns	See Fig. 12
Outputs						
Output propagation delay	t_{OPD}			50	ns	See Fig. 17, note 1
CDR propagation delay	t_{CDRPD}			50	ns	See Fig. 18
Frame synchronisation & related inputs						
FRS rising hold time	t_{FRH}	50			ns	See Fig. 13
FRS rising setup time	t_{FRs}	100			ns	See Fig. 13
FRS falling hold time	t_{FFH}	50			ns	See Fig. 13
FRS falling setup time	t_{FFS}	100			ns	See Fig. 13
TZS setup time	t_{SFS}	50			ns	See Fig. 13
TZS hold time	t_{SFH}	50			ns	See Fig. 13
User data setup time	t_{UDS}	50			ns	See Fig. 13
International data bits setup time	I_{IDS}	100			ns	See Fig. 13
Timeslot Zero data hold time	t_{TZDH}	100			ns	See Fig. 13
Data inputs						
Data setup time	t_{DS}	50			ns	See Fig. 14, note 2
Data hold time	t_{DH}	50			ns	See Fig. 14, note 2
Timeslot 16 transmitter data setup time	t_{T16DS}	50			ns	See Fig. 15, note 3
Timeslot 16 transmitter data hold time	t_{T16DH}	50			ns	See Fig. 15, note 3
HDB3 input data setup time	t_{RXDS}	50			ns	See Fig. 16
HDB3 input data pulse width	t_{RXDW}	50		488	ns	See Fig. 16

NOTES
1. The output propagation delay, t_{OPD}, is valid for all outputs except CDR (from the HDB3DC macrocell) and is specified with FRS rising betore CLK. All output delays are measured with a 50pF load.
2. The data setup and hold parameters, t_{DS} and t_{DH}, apply to the following macrocell inputs: D (CRCGEN), D (HDB3EC) PCM DATA (TMUX), D (RXTSZ), FRS13,15 (RXTSZ), RST (RXTSZ), D (RXTS16), D (CRCCHK), P (GLOBAL)
3. Timeslot 16 transmitter data setup and hold times apply to the rising edge of clock cycles 24, 56, 88 etc (see Fig 4)

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings are limiting values above which opertaing life may be shortened or specified parameters may be degraded.

Positive supply voltage, V_{DD}	- 0.5 to + 7V
Inputs	V_{DD} + 0.3V to GND - 0.3V
Outputs	V_{DD} + 0.3V to GND - 0.3V

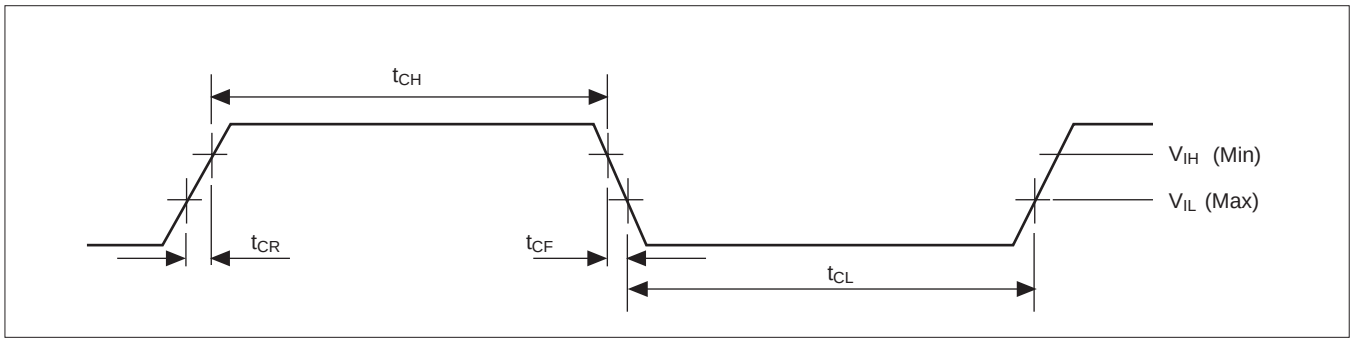


Figure 12: Timing - clock inputs

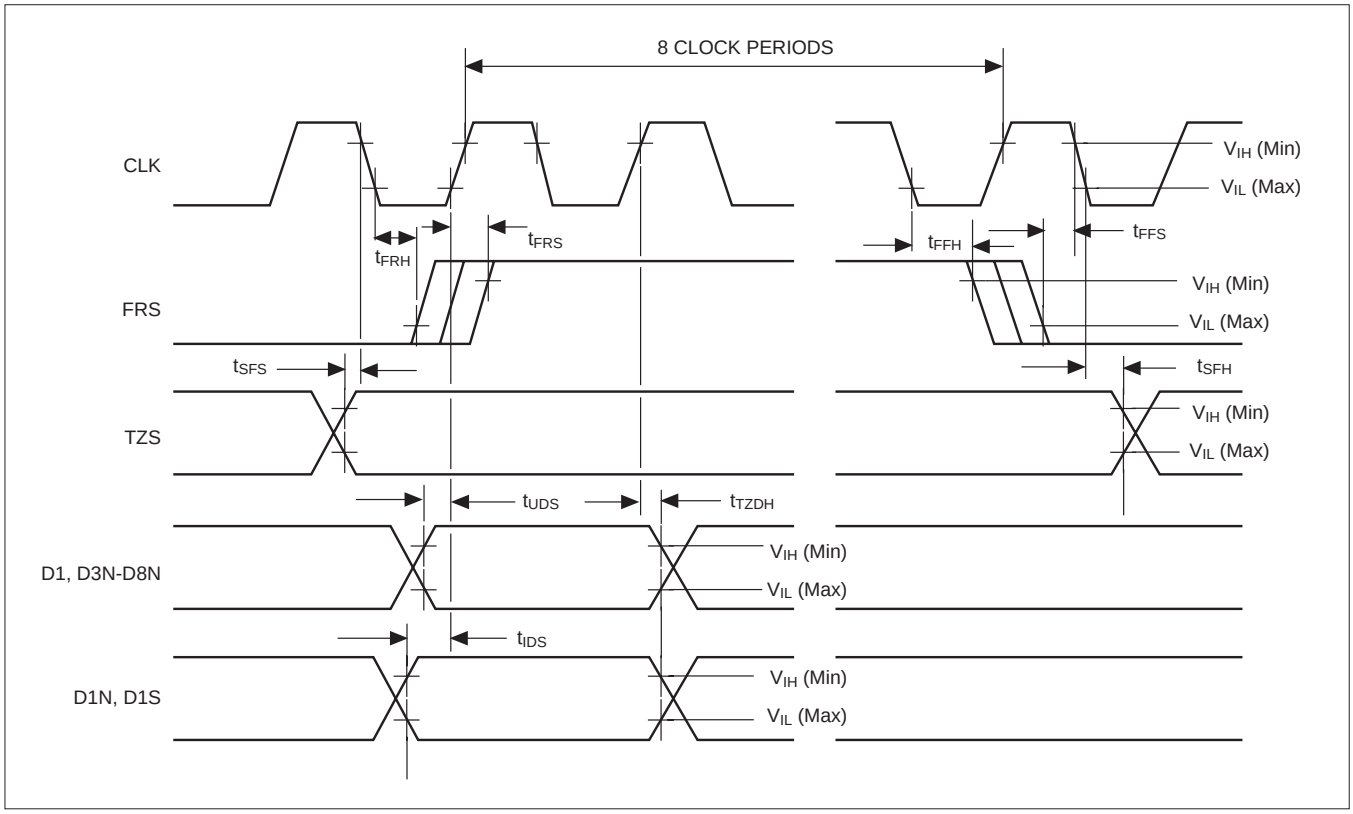


Figure 13: Timing - FRS and related parameters

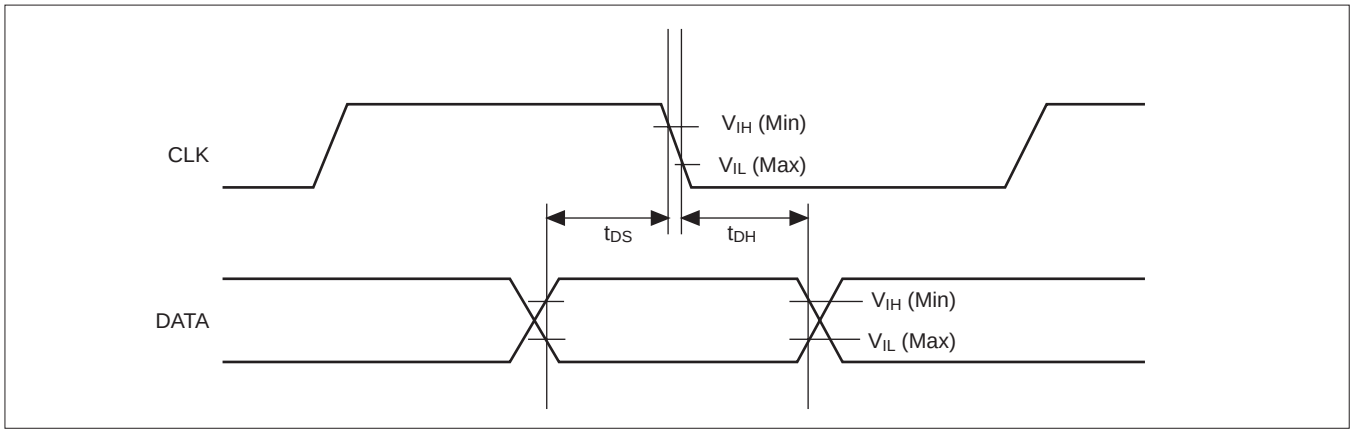


Figure 14: Timing - data inputs

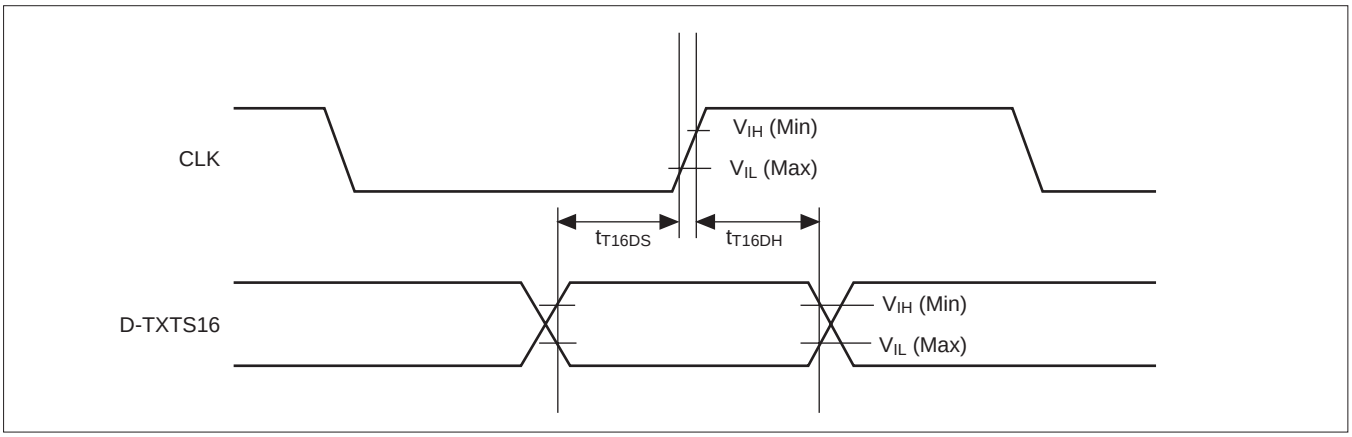


Figure 15: Timing - Timeslot 16 transmitter data input

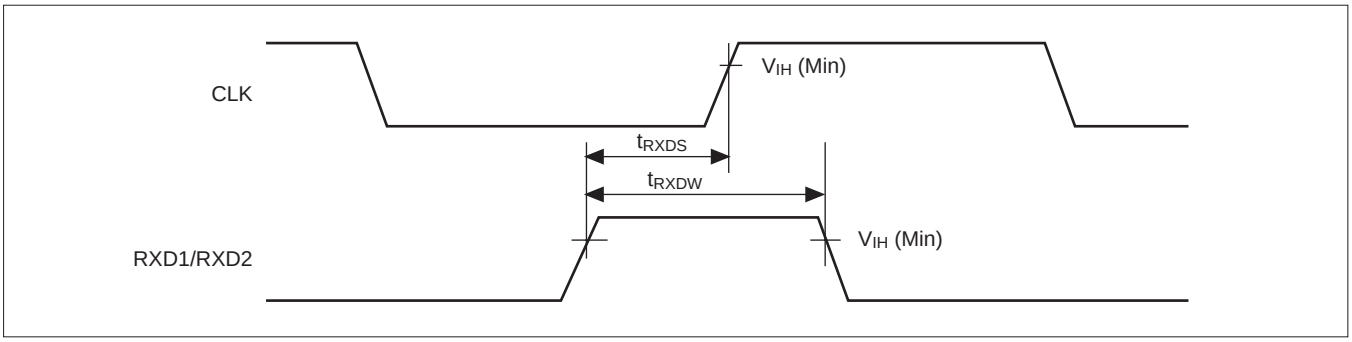


Figure 16: Timing - RXD inputs

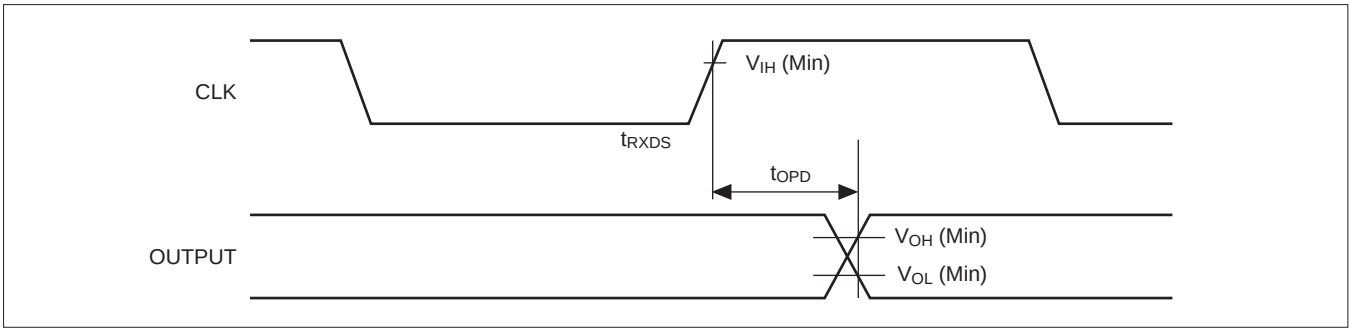


Figure 17: Timing - output propagation delay

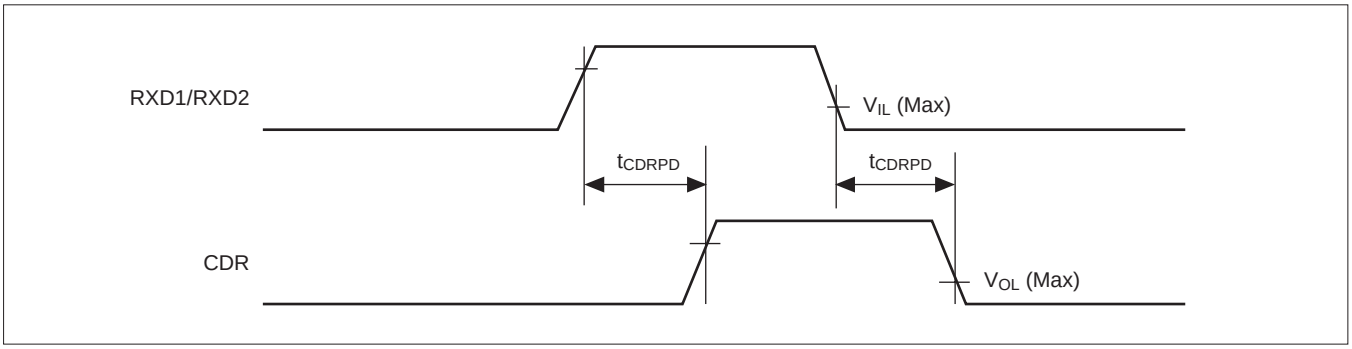


Figure 18: Timing - CDR propagation delay

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