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ADVANCE INFORMATION
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MV3100

3 VOLT CODEC WITH ANALOG INTERFACE FOR DIGITAL MOBILE TELEPHONES

(Supersedes version in June 1990 Personal Communications IC Handbook)

The MV3100 is a complete integrated audio interface for digital mobile telehones.Using mixed signal CMOS technology the device contains a DSP codec for audio to PCM conversion, together with gain programmable microphone and loudspeaker amplifiers.

The use of a DSP architecture for the codec function enables device operation from supplies of 2·7 to 3·6 volts and allows software programming of gain characteristics.The device requires a minimum of external components giving a physically small solution, ideal for hand-portable telephones.

FEATURES

- Highly Integrated Solution with On-chip Audio Interface
- Meets Relevant Performance Parameters from MPT1375, I-ETS 300 131:1990, BS6833 and CCITT G714
- Low Voltage Operation, 2·7V to 3·6V
- Low Power Consumption, 25mW typ
- Excellent RF Immunity
- 16-Bit Linear/8-Bit Companded A/μ-Law Programmable PCM Interface
- Gain Programmability Supports many Microphone and Loudspeaker Sensitivities
- On-chip PLL Generates all Internal Clocks

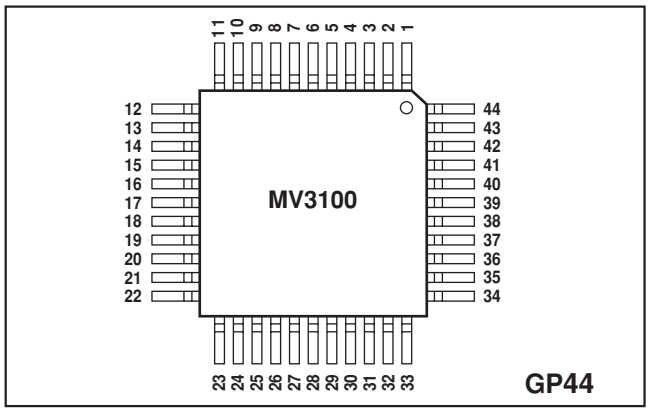


Fig.1 Pin connections - top view. See pin list, Table 1.

APPLICATIONS

- Digital Cordless Telephones (CT2, DECT, JDCT, Spread Spectrum)
- Digital Cellular Telephones (GSM, ADC, JDC)
- Digital Mobile Radio

ORDERING INFORMATION

MV3100 IG GPBR (Industrial - plastic QFP package)

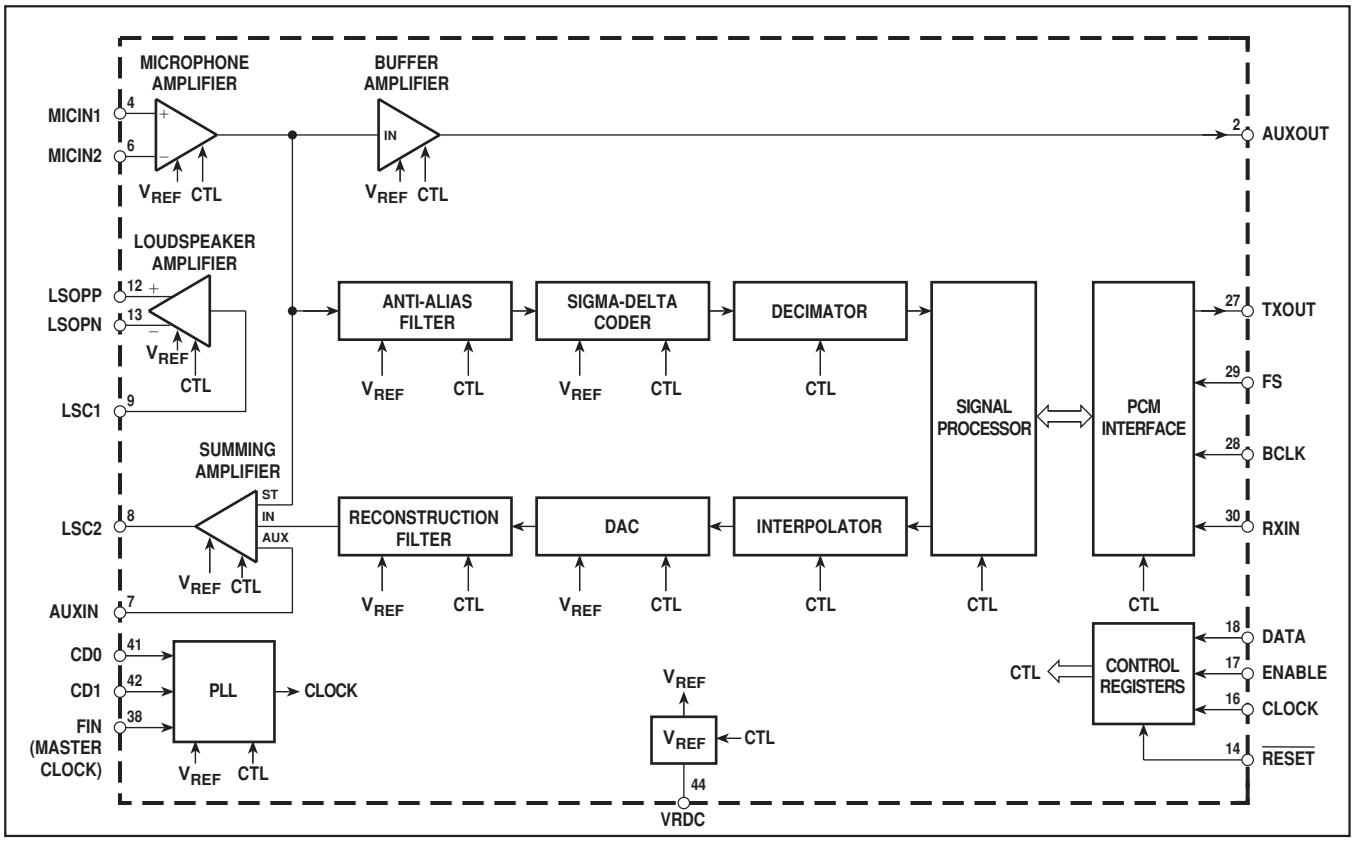


Fig. 2 MV3100 block diagram

Pin	Name	Description
1	V_{DD}TX	Transmit path analog V_{DD}
2	AUXOUT	Transmit path auxiliary output
3	IC	Internal connection - do not connect
4	MICIN1	Microphone amp. input non-inverting input
5	GNDTX	Transmit path analog ground
6	MICIN2	Microphone amp. inverting input
7	AUXIN	Receive path auxiliary input
8	LSC2	Summing amplifier intermediate output
9	LSC1	Loudspeaker amplifier intermediate input
10	GNDRX	Receive path analog ground
11	V_{DD}RX	Receive path analog V_{DD}
12	LSOPP	Loudspeaker amp. non-inverting output
13	LSOPN	Loudspeaker amp. inverting output
14	$\overline{\text{RESET}}$	Master reset (active low)
15	IC	Internal connection - do not connect
16	CLOCK	Control interface data clock
17	ENABLE	Control interface enable
18	DATA	Control interface data input
19	IC	Internal connection - do not connect
20	IC	Internal connection - do not connect
21	IC	Internal connection - do not connect
22	IC	Internal connection - do not connect
23	IC	Internal connection - do not connect
24	NC	No connection
25	V_{DD}D	Digital V_{DD}
26	NC	No connection
27	TXOUT	PCM interface transmit data output
28	BCLK	PCM interface data clock
29	FS	PCM interface frame sync.
30	RXIN	PCM interface receive data input
31	GNDD	Digital ground
32	NC	No connection
33	IC	Internal connection - do not connect
34	NC	No connection
35	IC	Internal connection - do not connect
36	IC	Internal connection - do not connect
37	IC	Internal connection - do not connect
38	FIN	PLL reference frequency input (Master Clock)
39	V_{DD}PL	PLL V_{DD}
40	GNDPL	PLL ground
41	CD0	PLL capacitor ground connection
42	CD1	PLL capacitor signal connection
43	NC	No connection
44	VRDC	Voltage reference decoupling

Table 1 Pin list

FUNCTIONAL DESCRIPTION

The transmit circuit has a low noise differential input microphone amplifier front end and is suitable for use with an electret microphone. For use in cordless or mobile telephone applications the sensitive analog inputs are designed to be immune to RF pickup. The transmit gain may be varied over a range of 22·8 dBm0/dBV to 37·8 dBm0/dBV in 1dB steps. An auxiliary analog output is available.

The analog transmit signal is passed through a simple Anti-alias Filter and is then sampled by the Sigma-Delta Coder which, combined with the Decimator, performs a high linearity analog to digital conversion. This digital signal is then passed to the Signal Processor which performs the transmit filtering. The transmit filter may be set to either of two modes. For handset use the full band-pass filter is implemented, while for base station use the transmit filter has reduced bass roll-off.

The filtered digital transmit signal from the Signal Processor is output via the serial PCM interface. The PCM interface can be programmed via the control interface to operate in one of three modes, 16-bit 2's complement linear PCM, 8-bit companded A-Law coding or 8-bit companded μ-Law coding. In all modes, each word or byte is output as a serial bit stream at a frame rate of 8K words/bytes per second under the control of the bit clock BCLK and the frame sync FS inputs. A mute function is included on the output.

The digital receive signal is input to the Signal Processor via the PCM interface as a series of sixteen-bit words or eight-bit bytes as described above. A separately controlled mute function may also be applied.

The Signal Processor performs the receive band-pass filtering and then passes the filtered digital signal to the Interpolator. The Interpolator in conjunction with the DAC performs a high linearity digital to analog conversion. The resulting analog output is filtered by the Reconstruction Filter to remove the sampling noise.

The Summing Amplifier may optionally add to the received signal the auxiliary analog input and the sidetone signal from the transmit path. The nominal sidetone gain may be varied from 19·7 dB to 28·7 dB in 3dB steps. The Summing Amplifier output is connected externally to the Loudspeaker Amplifier input to enable external filtering components to be added if required. The Loudspeaker Amplifier is a bridge amplifier which has been designed to drive a ceramic loudspeaker. It can produce a low distortion drive into loads of up to 105nF at a peak to peak amplitude near to twice V_{DD}.

The Phase Locked Loop generates the internal clock signals from a 32kHz input clock. After power-up the PLL clock must be enabled by programming Control Register 100 bit 3 (PLL Clock Enable) to the on state ('0').The PLL is specifically designed to extract a low phase error clock in cases where there is jitter on the input clock, provided that there are exactly 64 input clock cycles in every 500Hz period. This ensures accurate clock extraction from the CT2 'ping-pong' signalling system.

The on-chip bandgap voltage reference provides the necessary biasing and reference voltages required by the analog circuitry.

Programming of the various gains and operating modes for the device is by means of a three-wire serial interface to the Control Registers. Data is clocked into the Data input under control of the Clock and Enable inputs. The digital circuitry and various parts of the analog circuitry may be powered down individually by means of the control interface. This may be used to minimise power consumption during various phases of call set-up and standby operation.

The device is designed to operate from a nominal 3 volt supply. Separate supply and ground pins are provided for the transmit analog, receive analog and digital circuits to improve decoupling between transmit and receive paths and reduce digital noise breakthrough into the analog circuitry.

DETAILED DESCRIPTION

Microphone Input

The Microphone Amplifier was designed to meet the CT2 Common Air Interface specification MPT1375 Part 4. With the transmit gain set to its nominal value, an input of −34·8dBV will produce a digital output of 0 dBm0. The circuit was designed for a microphone with a nominal sensitivity of −41·8dBV/Pa. This gain may be varied by +3·0dB to −12·0dB in steps of 1dB by means of the control interface. This gain range is intended to provide for a microphone sensitivity tolerance of ±3 dB and permits a gain reduction of up to 9dB to reduce sensitivity for use in conditions of high ambient noise.

The Microphone Amplifier may be powered down by means of the control interface when not in use to reduce power consumption.

Auxiliary Output

The auxiliary output has a nominal gain of 19·9 dB from the microphone input. The output level is dependent on the gain setting giving a gain range of 7·9dB to 22·9dB. The output is designed to be able to deliver a 500 mV rms signal into a 30kΩ +20 pF load.

The auxiliary output may be turned off by means of the control interface when not in use to reduce power consumption.

Loudspeaker Output

The Loudspeaker Amplifier was designed to meet the CT2 Common Air Interface specification MPT1375 Part 4. With the receive gain set to its nominal value, an output of −6·1dBV will be produced for a digital input of 0dBm0. The circuit was designed for a loudspeaker with a nominal sensitivity of +12·0 dBPa/V. The gain may be varied by +9·0dB to −22·0dB in steps of 1dB by means of the control interface. This gain range is intended to provide for a loudspeaker sensitivity tolerance of ± 3dB and permit a gain variation of +6dB to−18dB to enable the implementation of a user volume control.

The Loudspeaker Amplifier may be powered down when not in use by means of the control interface to reduce power consumption.

The nominal gain from the auxiliary input to the loudspeaker output is 13·4dB. This gain is dependent on the receive gain setting giving a gain range of +22·4dB to−8·6dB. The auxiliary input may be disconnected by means of the control interface if not required.

The nominal sidetone gain from the microphone input to the loudspeaker output (with both transmit and receive gains set to nominal) is 25·7dB. This gain may be varied by +3·0dB to −6·0dB in 3·0dB steps by means of the control interface. If not required, the sidetone may be turned off by means of the control interface.

PCM INTERFACE

The PCM Interface inputs the received digital signal RXIN and outputs the transmit digital signal TXOUT in the form of sixteen-bit words or eight-bit bytes as a serial bit stream under the control of the two timing signals FS and BCLK.

Three PCM coding options are programmable via the control interface, linear sixteen-bit 2's complement PCM, eight-bit A-Law companded PCM or eight bit μ-Law companded PCM. It is normal in a system to have a single coding scheme; for this reason Transmit and Receive coding are programmed simultaneously to work with the same scheme.

The serial PCM interface thus consists of four pins; three inputs and one output.

BCLK	PCM data clock input
FS	PCM frame sync input
TXOUT	PCM transmit data output
RXIN	PCM receive data input

Interface timings are shown in Figs. 3 and 4.

NOTES

1. The Sync pulse is nominally one clock pulse wide, changes in state nominally coinciding with the rising edge of the clock. Jitter on the FS rising edge can occur up to ±5μs on the actual and ideal edge positions.
2. The Data bits are nominally one clock cycle wide, nominally changing on the rising edge of the clock.
3. Data bits (RXIN) will be latched nominally on the falling edge of the clock.
4. The data output (TXOUT) will be high impedance between the end of the last data bit of one word/byte and the beginning of the first data bit of the next word/byte.
5. The RXIN signal must always be at a solid logic level, even though it is only the data at the times indicated which is used. In the case of RXIN the mid-line should be taken to indicate a 'don't care' state, not a high impedance state.
6. The Clock signal BCLK may consist of either a train of at least seventeen pulses in linear PCM mode or nine pulses in A/μ-Law companded PCM mode (one for FS and one for each data bit), or be a continuous clock.

This block is the interface between parallel 2's complement sixteen-bit linear PCM data and serial sixteen- bit linear 2's complement or serial eight-bit A/μ-Law companded PCM data, performing parallel-to-serial conversion in the transmit direction and serial-to-parallel conversion in the receive direction. In addition to the conversion and coding function the PCM block implements a mute function. Both TX and RX can be independently muted. The mute functions are controlled from the microprocessor bus control interface.

A-Law and μ-Law Codes (8 Bit)

These are non-linear codes in which the signal is described in terms of a sign bit plus segment and chord bits which denote the magnitude. There are 7 segments for A- Law and 8 for μ-Law. The size of the segment increases in approximately exponential steps. Each segment is divided up linearly into chords (except the zero level in μ-Law). This means that the resolution is finer at smaller input voltages than at larger. Tables detailing these

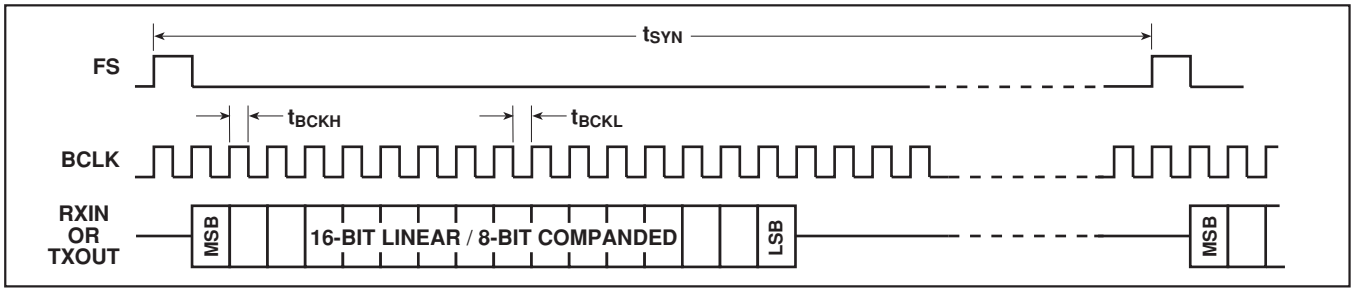


Fig. 3 PCM Interface timing diagram

Parameter	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
BCLK frequency (linear mode)	f_{BCK}	256		2048	kHz	
BCLK frequency (companded mode)	f_{BCK}	128		2048	kHz	
BCLK rise time	t_{BCKR}		5		ns	
BCLK fall time	t_{BCKF}		5		ns	
BCLK high time	t_{BCKH}	200			ns	
BCLK low time	t_{BCKL}	200			ns	
FS pulse period	t_{SYN}		125		μs	FIN = 32kHz

NOTE 1: The Frame Sync (FS) MUST be frequency locked to the 32kHz PLL Master Clock (FIN). The phase relationship is not important.

Table 2 PCM Interface timings

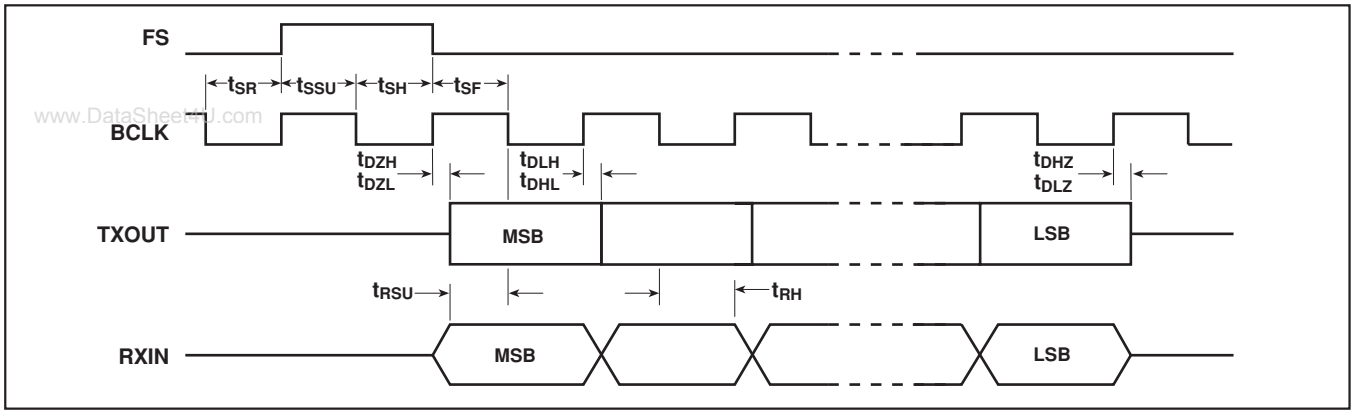


Fig. 4 PCM Interface timing diagram (expanded)

Parameter	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
FS to BCLK set-up time	t_{SSU}	10			ns		2
FS to BCLK hold time	t_{SH}	15			ns		2
BCLK to FS rising time	t_{SR}	25			ns		2
FS falling to BCLK time	t_{SF}	25			ns		2
Output delay from Z to high	t_{DZH}			25	ns		2
Output delay from Z to low	t_{DZL}			25	ns		2
Output delay from high to Z	t_{DHZ}			25	ns		2
Output delay from low to Z	t_{DLZ}			25	ns		2
Output delay from high to low	t_{DHL}			30	ns		2
Output delay from low to high	t_{DLH}			30	ns		2
RXIN set-up time	t_{RSU}	10			ns		2
RXIN hold time	t_{RH}	15			ns		2

Table 3 PCM Interface timings (see Fig. 4)

NOTE 2. Not production tested

codes can be found in CCITT G711.

In both codes positive values are represented by a sign bit of 1. The A-Law data is alternate digit inverted (ADI) and the μ-Law magnitude data is in effect inverted. These techniques are used to ensure that there are sufficient data transitions for good clock recovery (not performed by the MV3100) on the Received side of the digital trunk lines when the channel is quiet.

CONTROL INTERFACE (SEE FIGS. 5 AND 6))

The Control Interface essentially has two sections. Firstly the serial/parallel input shift and address decode section, which controls the control registers. This is the Control Interface proper. Secondly, the reset section which generates a digital chip reset from the combination of 'hard' (i.e., power-on/pin generated) and 'soft' (i.e., programmed into the control registers) resets.

The data is serially clocked into the DATA input by the CLOCK input. The first 5 bits are the data to be stored and the second 3 bits identify which register is to be addressed. After the data has been clocked in, a separate ENABLE pulse stores the data in the appropriate register.

The Control Interface has four inputs:

CLOCK	Control Interface clock
DATA	Serial data input for the control registers
ENABLE	Control Interface enable Signal
$\overline{\text{RESET}}$	See below

The $\overline{\text{RESET}}$ input is used to provide a full chip reset. The general rule is that, on reset, the chip is set to handset operation, minimum gain settings and all parts powered down, with the exception of the PLL and the V_{REF} (CR0<1>) which is powered up.

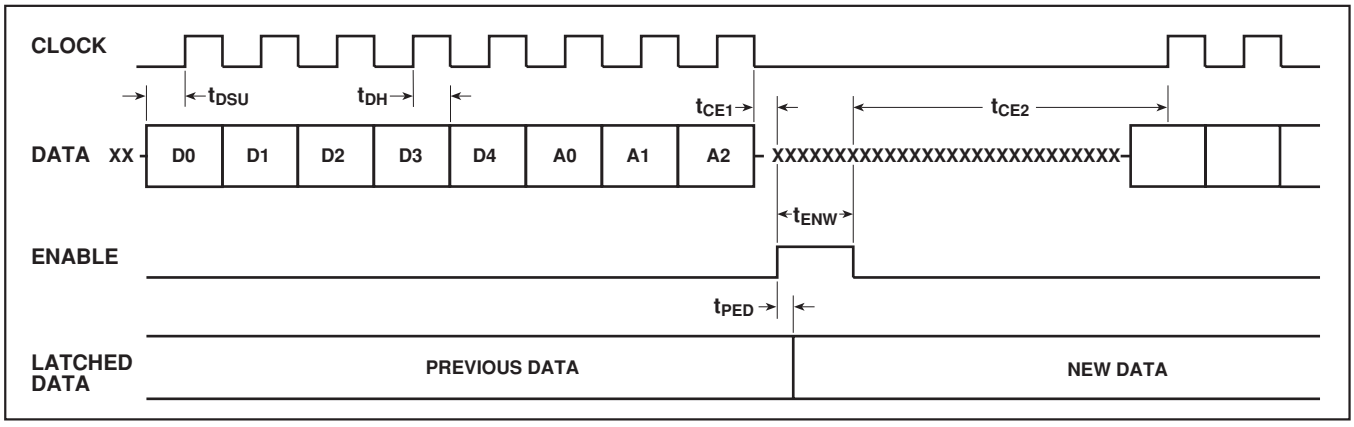


Fig. 5 Control Interface timing diagram

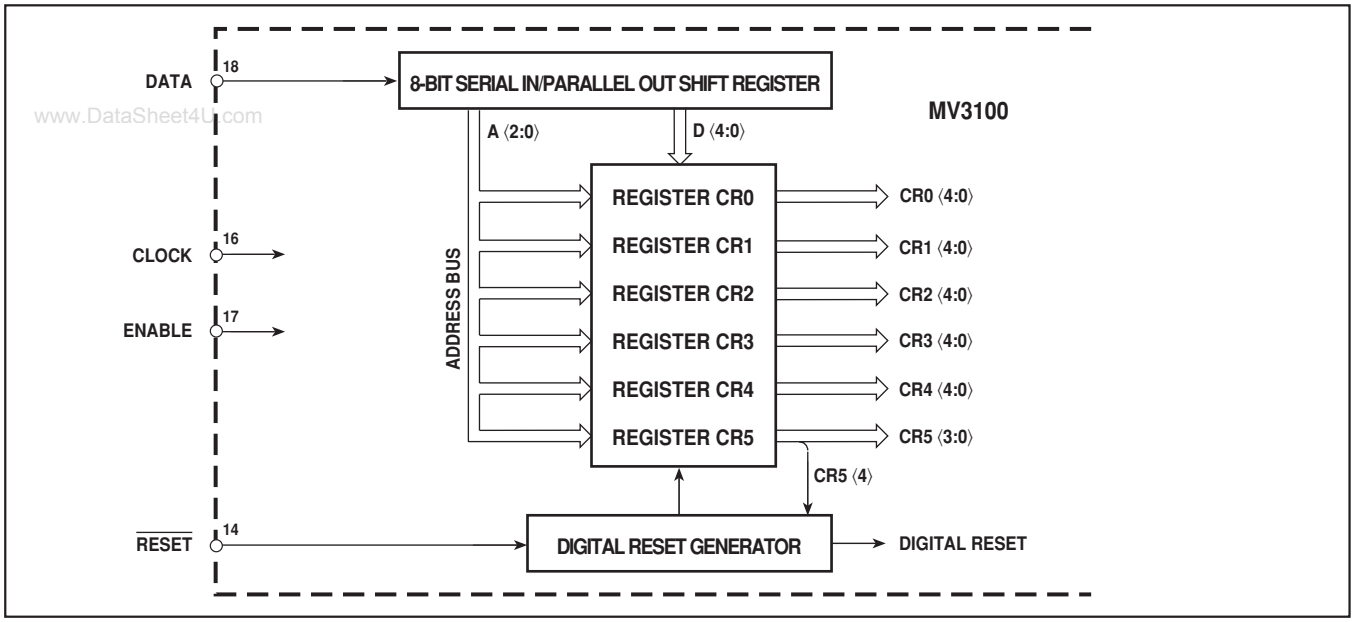


Fig. 6 Control Interface timing diagram

Parameter	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
CLOCK frequency	f_{CK}	32		2048	kHz		
CLOCK rise time	t_{CKR}		5		ns		
CLOCK fall time	t_{CKF}		5		ns		
CLOCK high time	t_{CKH}	200			ns		
CLOCK low time	t_{CKL}	200			ns		
DATA set-up time	t_{DSU}	3			ns		2
DATA hold time	t_{DH}	10			ns		2
CLOCK low to ENABLE high time	t_{CE1}	20			ns		2
ENABLE low to CLOCK high time	t_{CE2}	10			ns		2
ENABLE pulse width	t_{ENW}	200			ns		

Table 4 Control Interface timings

NOTES
3. CLOCK must be low during the ENABLE pulse, otherwise false data will be stored.
4. It is not strictly necessary for the clock pulses to be identical. So long as t_{DSU} , t_{DH}, and min. t_{CKH}/t_{CKL} are met for every data bit, the waveform could actually be irregular.

CONTROL REGISTER FUNCTIONS (Tables 5 to 10)

Address	Bit	Function	Bit state		Reset value
			0	1	
000	0	Digital circuitry	Active	Standby	1
	1	PLL/V_{REF}	Active	Standby	0
	2	Microphone amplifier	Active	Standby	1
	3	Loudspeaker amplifier	Active	Standby	1
	4	Auxiliary amplifier	Active	Standby	1

Table 5 Control register CR0 functions

Address	Bit	Function	Bit state		Reset value
			0	1	
001	0	Undefined			1
	1	Undefined			1
	2	Undefined			1
	3	Undefined			1
	4	Base Station mode	Off	On	0

Table 6 Control register CR1 functions

CONTROL REGISTER FUNCTIONS (continued)

Address	Bit	Function	Bit state 0	Bit state 1	Reset value
010	0	Microphone amplifier (Transmit) gain setting bits ⟨3:0⟩ (See Table 14)			0
	1				0
	2				0
	3				0
	4	Reserved		Note 4	0

Table 7 Control register CR2 functions

NOTE 4: Not allowed

Address	Bit	Function	Bit state 0	Bit state 1	Reset value
011	0	Loudspeaker amplifier (Receive) gain setting bits ⟨4:0⟩ (See Table 21)			0
	1				0
	2				0
	3				0
	4				0

Table 8 Control register CR3 functions

Address	Bit	Function	Bit state 0	Bit state 1	Reset value
100	0	Sidetone gain bits ⟨1:0⟩ (See Table 26)			1
	1				1
	2	Sidetone path	On	Off	1
	3	PLL clock enable	On	Off	1
	4	Auxiliary input	On	Off	1

Table 9 Control register CR4 functions

Address	Bit	Function	Bit state 0	Bit state 1	Reset value
101	0	Transmit mute	Normal	Mute	1
	1	Receive mute	Normal	Mute	1
	2	PCM mode	Compand	Linear	1
	3	A/μ-Law	A-Law	μ-Law	1
	4	Digital reset	Normal	Reset	0

Table 10 Control register CR5 functions

DETAILED SPECIFICATION

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{DD} = 2·7V to 3·6V, T_{AMB} = −30°C to +70°C (see note 5)

DC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Supply voltage	V_{DD}	2·7		3·6	V		8
Operating temperature	T_{AMB}	−30		+70	°C		
Active power dissipation	P_{OP}		25	30	mW	V_{DD} = 2·7V	
			40	48	mW	V_{DD} = 3·6V	
Standby power dissipation	P_{SB}		3·8	4·0	mW	V_{DD} = 2·7V	9
			6·5	6·8	mW	V_{DD} = 3·6V	9
Powered down dissipation	P_{DN}		25	30	µW	V_{DD} = 2·7V	
			30	50	µW	V_{DD} = 3·6V	

Table 11

NOTES
5. All electrical testing is performed at T_{AMB} = 25°C.
6. All detailed specification parameters apply for Linear PCM, A-Law PCM and µ-Law PCM modes.
7. Typical values shown are for the MV3100 operating in Linear mode only.
8. All ground pins (pins 5, 10, 31 and 40) must be connected together to mimimise any voltage difference between them. Similarly, all V_{DD} pins (pins 1, 11, 25 and 39) must be connected together.
9. The Standby mode is with the PLL and V_{REF} powered up only.

DIGITAL CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Input low voltage	V_{IL}			0·2	V_{DD}		
Input high voltage	V_{IH}	0·75			V_{DD}		
Low level input current	I_{IL}			5	µA		10
High level input current	I_{IH}			5	µA		11
Output low voltage (TXOUT)	V_{OL}		0·2	0·4	V		
Output high voltage (TXOUT)	V_{OH}	0·75	0·9		V_{DD}		
Tristate leakage current (TXOUT)	I_{OZ}			<10	µA		
Input capacitance	C_{IN}		5		pF		12
Output capacitance	C_{OUT}		5		pF		12

Table 12

NOTES
10. All digital input pins except $\overline{\text{RESET}}$, which has a 10kΩ pull up resistor giving I_{IL} max = 400µA.
11. All digital input pins.
12. Not production tested.

Master Clock Input

The PLL Master Clock input (FIN, pin 38) will be capable of accepting a clock with jitter to the following specification:
1. Over a defined 2ms period there will be exactly 64 cycles of the 32kHz clock.
2. The maximum error between the ideal and actual clock edges will be three periods of 1·44MHz (2·1µs).

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0·3V to +6V
Input voltage	−0·3V to V_{DD}+0·3V
Operating temperature	−40°C to +85°C
Storage temperature	−55°C to +125°C

TRANSMIT CHARACTERISTICS

Transmit gain = nominal (see Table 14)

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Gain (MICIN to TXOUT)	A_{VTX}		34·8		dBm0/dBV	1kHz	
Gain (MICIN to AUXOUT)	A_{VTA}		19·9		dB	1kHz	
Gain variation with temperature	A_{VT}	−1·0		+1·0	dB	−30°C to +70°C	13
Gain variation with supply	A_{VST}	−0·5		+0·5	dB	2·7V to 3·6V	
Clipping level distortion	D_{CLT}			1	%	Output = 3dBm0	13
Wide band noise	N_{WBT}			−69	dBm0p		14
Narrow band noise	N_{NBT}			−76	dBm0		13, 15
Power supply rejection ratio	PSRR	60			dB		13, 16
MICIN input impedance	Z_{IN}		20		kΩ		13
AUXOUT load resistance	R_{LA}	30			kΩ		
AUXOUT load capacitance	C_{LA}			20	pF		
MICIN common mode rejection ratio	CMRR	40			dB		17

Table 13

NOTES
13. Not production tested.
14. Bandwidth 300Hz to 3400Hz, psophometrically weighted.
15. Any 10Hz band centred over the frequency range 305Hz to 3395Hz.
16. 20mVp-p sinewave at 500Hz applied to the positive supply.
17. 20mVp-p sinewave at 500Hz applied to both microphone input pins.

TRANSMIT GAIN CONTROL RANGE

Nominal gain is highlighted

Control Word 2					Main path (dBm0/dBV)			Auxiliary path (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.	Min.	Typ.	Max.
X	0	0	0	0	22·6	22·8	23	7·7	7·9	8·1
X	0	0	0	1	23·6	23·8	24	8·7	8·9	9·1
X	0	0	1	0	24·6	24·8	25	9·7	9·9	10·1
X	0	0	1	1	25·6	25·8	26	10·7	10·9	11·1
X	0	1	0	0	26·6	26·8	27	11·7	11·9	12·1
X	0	1	0	1	27·6	27·8	28	12·7	12·9	13·1
X	0	1	1	0	28·6	28·8	29	13·7	13·9	14·1
X	0	1	1	1	29·6	29·8	30	14·7	14·9	15·1
X	1	0	0	0	30·6	30·8	31	15·7	15·9	16·1
X	1	0	0	1	31·6	31·8	32	16·7	16·9	17·1
X	1	0	1	0	32·6	32·8	33	17·7	17·9	18·1
X	1	0	1	1	33·6	33·8	34	18·7	18·9	19·1
X	1	1	0	0	34·6	34·8	35	19·7	19·9	20·1
X	1	1	0	1	35·6	35·8	36	20·7	20·9	21·1
X	1	1	1	0	36·6	36·8	37	21·7	21·9	22·1
X	1	1	1	1	37·6	37·8	38	22·7	22·9	23·1

Table 14

TRANSMIT GAIN VARIATION WITH AMPLITUDE

Frequency = 700Hz to 1100Hz

Input amplitude		Relative gain (dB)		
dBV	mVrms	Min.	Typ.	Max.
−89·4	0·034	−1·6		+1·6
−84·4	0·06	−0·6		+0·6
−74·4	0·19	−0·3		+0·3
−64·4	0·6	−0·3		+0·3
−54·4	1·9	−0·3		+0·3
−44·4	6·0		0	
−34·4	19·0	−0·3		+0·3
−31·4	27·0	−0·3		+0·3

Table 15

TRANSMIT DISTORTION VARIATION WITH AMPLITUDE

Frequency = 1020Hz

Input amplitude		Signal to distortion (dBp)		
dBV	mVrms	Min.	Typ.	Max.
−79·4	0·11	24		
−74·4	0·19	29		
−64·4	0·6	35		
−54·4	1·9	35		
−44·4	6·0	35		
−34·4	19·0	35		

Table 16

TRANSMIT FREQUENCY RESPONSE - HANDSET MODE (SEE FIG. 7)

Response relative to 1kHz. Input signal level = −34·8dBV.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		−22·3	−20
200		−13	−3
300	−10	−7·4	−2
1000	−3	0	
3000	−4	0	3·5
3400	−6	0	4
4000		−3·0	2

Table 17

TRANSMIT FREQUENCY RESPONSE - BASE STATION MODE (SEE FIG. 8)

Response relative to 1kHz. Input signal level = −34·8dBV.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		−14·2	−12
200		−5·9	−2
300	−5	−1·9	0
500	−1	0	1
1000	−1	0	1
3000	−1	0	1
3400	−6	−0·1	1
4000		−3·0	0

Table 18

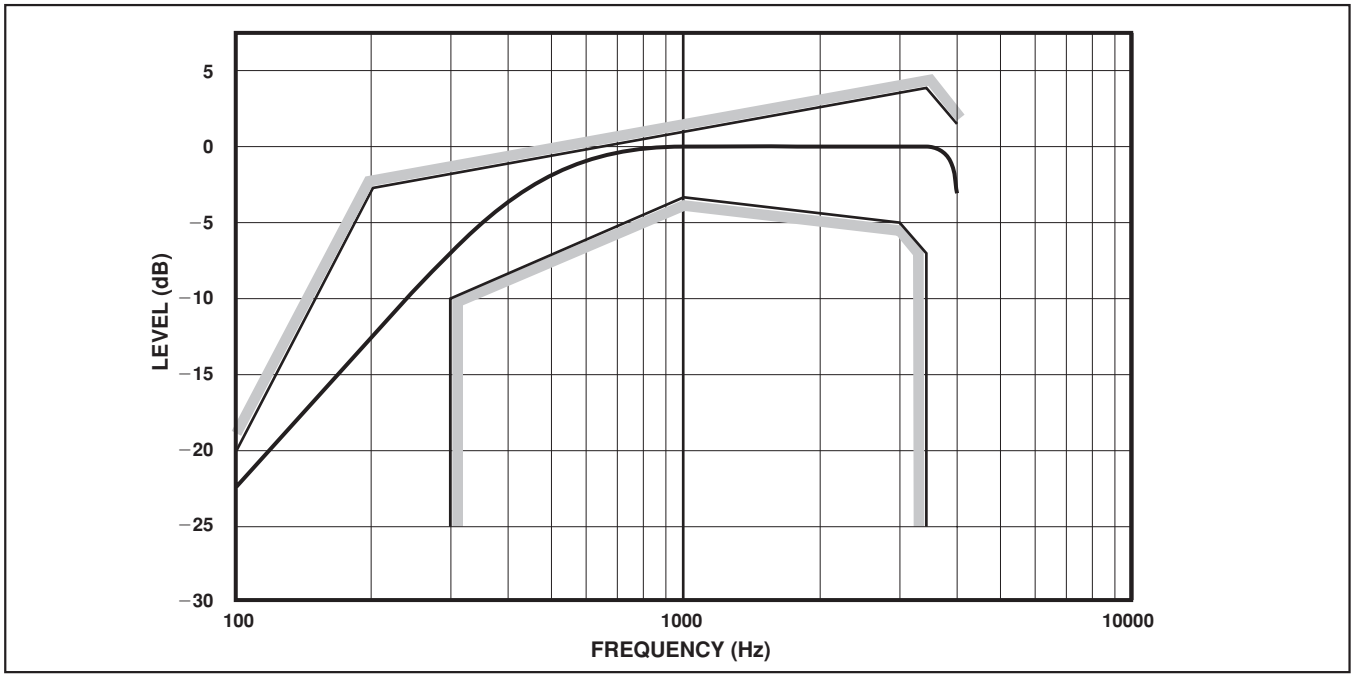


Fig. 7 Typical transmit frequency response - handset mode

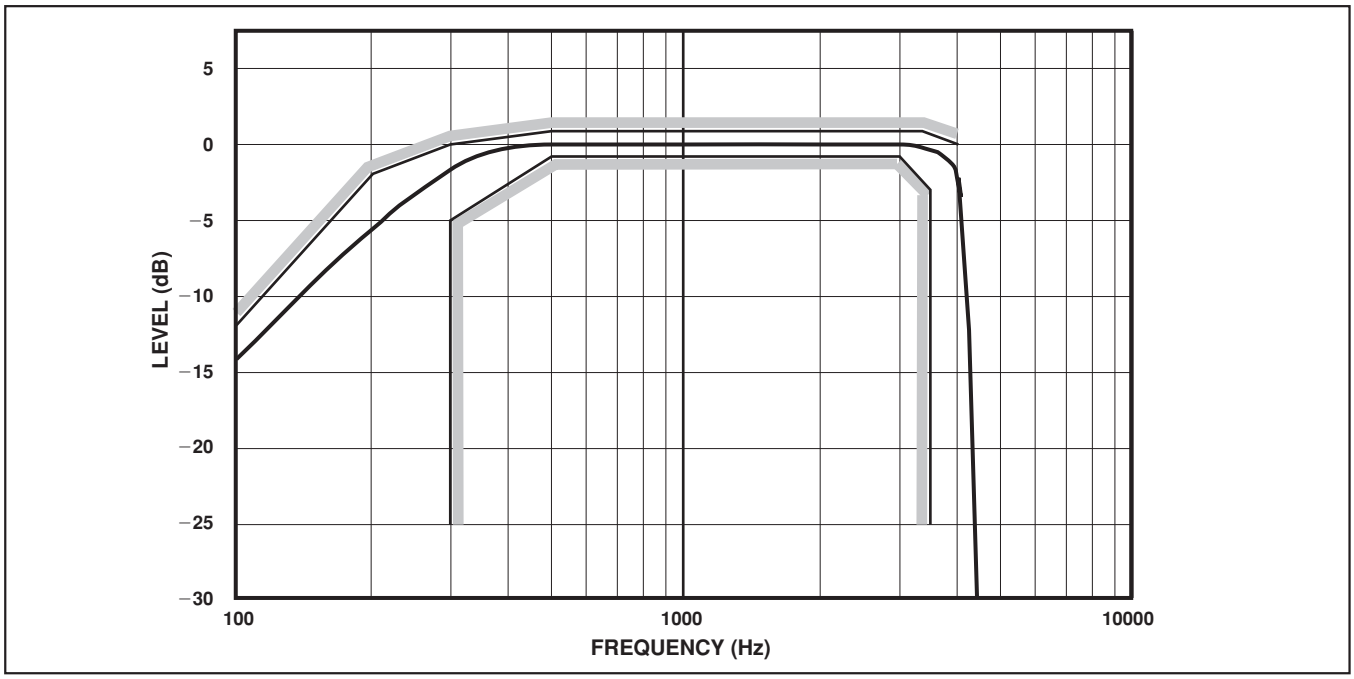


Fig. 8 Typical transmit frequency response - base station mode

TRANSMIT OUT-OF-BAND SIGNAL

Response relative to 1kHz. Input signal level = −34·8dBV.
Output is total power relative to that for 1kHz.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
4650			−30
5000			−31·5
6000			−35
6500			−36
7000			−37·5
7500			−39

Table 19

RECEIVE CHARACTERISTICS

Receive gain = nominal (see Table 21)

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Gain (RXIN to LSOPP/LSOPN)	A_{VRX}		−6·1		dBV/dBm0	1kHz	
Gain (AUXIN to LSOPP/LSOPN)	A_{VRA}		13·4		dB	1kHz	
Gain variation with temperature	A_{VTR}	−1·0		+1·0	dB	−30°C to +70°C	18
Gain variation with supply	A_{VSR}	−0·5		+0·5	dB	2·7V to 5·5V	
Clipping level distortion	D_{CLR}			<0·5	%	3dBm0, 1kHz	18
Wide band noise	N_{WBR}			−72	dBVp		19
Narrow band noise	N_{NBR}			−76	dB		18, 20
Signal out-of-band noise	N_{OBR}	45			dB		21
AUXIN input impedance	Z_{INA}		20		kΩ		
Sampling noise	N_S			−79	dBV	At 8kHz	
Power supply rejection ratio	PSRR	26			dB		18, 22
Louspeaker output load	Z_L		88	105	nF		

Table 20

NOTES
18. Not production tested.
19. Bandwidth 300Hz to 3400Hz psophometrically weighted.
20. Any 10Hz band centred over the frequency range 305Hz to 3395Hz.
21. For an input signal of 0dBm0 at 1kHz, the ratio between the signal at 1kHz and any signal between 4kHz and 8kHz at the loudspeaker.
22. 20mVp-p sinewave at 500Hz applied to the positive supply.

RECEIVE GAIN CONTROL RANGE

Nominal gain is highlighted

Control Word 3					Main path (dBV/dBm0)			Auxiliary path (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.	Min.	Typ.	Max.
0	0	0	0	0	−28·3	−28·1	−27·9	−8·8	−8·6	−8·4
0	0	0	0	1	−27·3	−27·1	−26·9	−7·8	−7·6	−7·4
0	0	0	1	0	−26·3	−26·1	−25·9	−6·8	−6·6	−6·4
0	0	0	1	1	−25·3	−25·1	−24·9	−5·8	−5·6	−5·4
0	0	1	0	0	−24·3	−24·1	−23·9	−4·8	−4·6	−4·4
0	0	1	0	1	−23·3	−23·1	−22·9	−3·8	−3·6	−3·4
0	0	1	1	0	−22·3	−22·1	−21·9	−2·8	−2·6	−2·4
0	0	1	1	1	−21·3	−21·1	−20·9	−1·8	−1·6	−1·4
0	1	0	0	0	−20·3	−20·1	−19·9	−0·8	−0·6	−0·4
0	1	0	0	1	−19·3	−19·1	−18·9	0·2	0·4	0·6
0	1	0	1	0	−18·3	−18·1	−17·9	1·2	1·4	1·6
0	1	0	1	1	−17·3	−17·1	−16·9	2·2	2·4	2·6
0	1	1	0	0	−16·3	−16·1	−15·9	3·2	3·4	3·6
0	1	1	0	1	−15·3	−15·1	−14·9	4·2	4·4	4·6
0	1	1	1	0	−14·3	−14·1	−13·9	5·2	5·4	5·6
0	1	1	1	1	−13·3	−13·1	−12·9	6·2	6·4	6·6
1	0	0	0	0	−12·3	−12·1	−11·9	7·2	7·4	7·6
1	0	0	0	1	−11·3	−11·1	−10·9	8·2	8·4	8·6
1	0	0	1	0	−10·3	−10·1	−9·9	9·2	9·4	9·6
1	0	0	1	1	−9·3	−9·1	−8·9	10·2	10·4	10·6
1	0	1	0	0	−8·3	−8·1	−7·9	11·2	11·4	11·6
1	0	1	0	1	−7·3	−7·1	−6·9	12·2	12·4	12·6
1	0	1	1	0	−6·3	−6·1	−5·9	13·2	13·4	13·6
1	0	1	1	1	−5·3	−5·1	−4·9	14·2	14·4	14·6
1	1	0	0	0	−4·3	−4·1	−3·9	15·2	15·4	15·6
1	1	0	0	1	−3·3	−3·1	−2·9	16·2	16·4	16·6
1	1	0	1	0	−2·3	−2·1	−1·9	17·2	17·4	17·6
1	1	0	1	1	−1·3	−1·1	−0·9	18·2	18·4	18·6
1	1	1	0	0	−0·3	−0·1	0·1	19·2	19·4	19·6
1	1	1	0	1	0·7	0·9	1·1	20·2	20·4	20·6
1	1	1	1	0	1·7	1·9	2·1	21·2	21·4	21·6
1	1	1	1	1	2·7	2·9	3·1	22·2	22·4	22·6

Table 21

RECEIVE GAIN VARIATION WITH AMPLITUDE

Frequency = 700Hz to 1100Hz

Input level (dBm0)	Relative gain (dB)		
	Min.	Typ.	Max.
−55	−1·6		+1·6
−50	−0·6		+0·6
−40	−0·3		+0·3
−30	−0·3		+0·3
−20	−0·3		+0·3
−10		0	
0	−0·3		+0·3
3	−0·3		+0·3

Table 22

RECEIVE DISTORTION VARIATION WITH AMPLITUDE

Frequency = 1020Hz

Input level (dBm0)	Signal to distortion (dBp)		
	Min.	Typ.	Max.
−45	24		
−40	29		
−30	35		
−20	35		
−10	35		
0	35		

Table 23

RECEIVE FREQUENCY RESPONSE (SEE FIG. 9)

Response relative to 1kHz. Signal level = −16dBm0.

Frequency (Hz)	Min. (dB)	Typ. (dB)	Max. (dB)
100		−22·2	−20
160		−11	−6
300	−5	−2	0
500	−1	0·2	1
1000		0	
3000	−1	0	1
3400	−6	0·2	1
4000		−3·0	0

Table 24

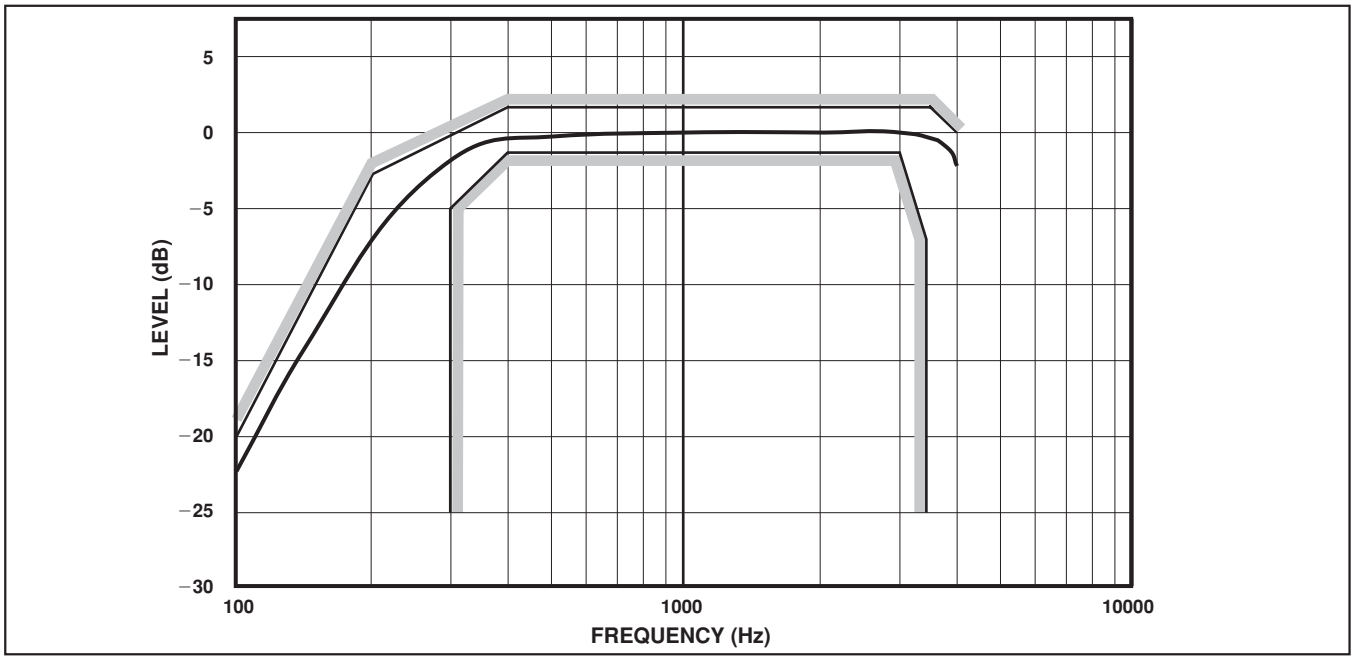


Fig. 9 Typical receive frequency response

BIDIRECTIONAL CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions	Notes
		Min.	Typ.	Max.			
Sidetone gain	A_S		25·7		dB		
Gain variation with temperature	A_{ST}	−2·0		+2·0	dB		23
Gain variation with supply	A_{SS}	−1·0		+1·0	dB		
Crosstalk, Tx to Rx	X_{TR}		−60		dB	No sidetone	
Crosstalk, Rx to Tx	X_{RT}		−60		dB		

Table 25

NOTE 23. Not production tested.

SIDETONE GAIN CONTROL RANGE

Nominal gain is highlighted

Control Word 4					Sidetone gain (dB)		
D4	D3	D2	D1	D0	Min.	Typ.	Max.
X	X	0	1	1	28·3	28·7	29·1
X	X	0	1	0	25·3	25·7	26·1
X	X	0	0	1	22·3	22·7	23·1
X	X	0	0	0	19·3	19·7	20·1
X	X	1	X	X			−35

Table 26

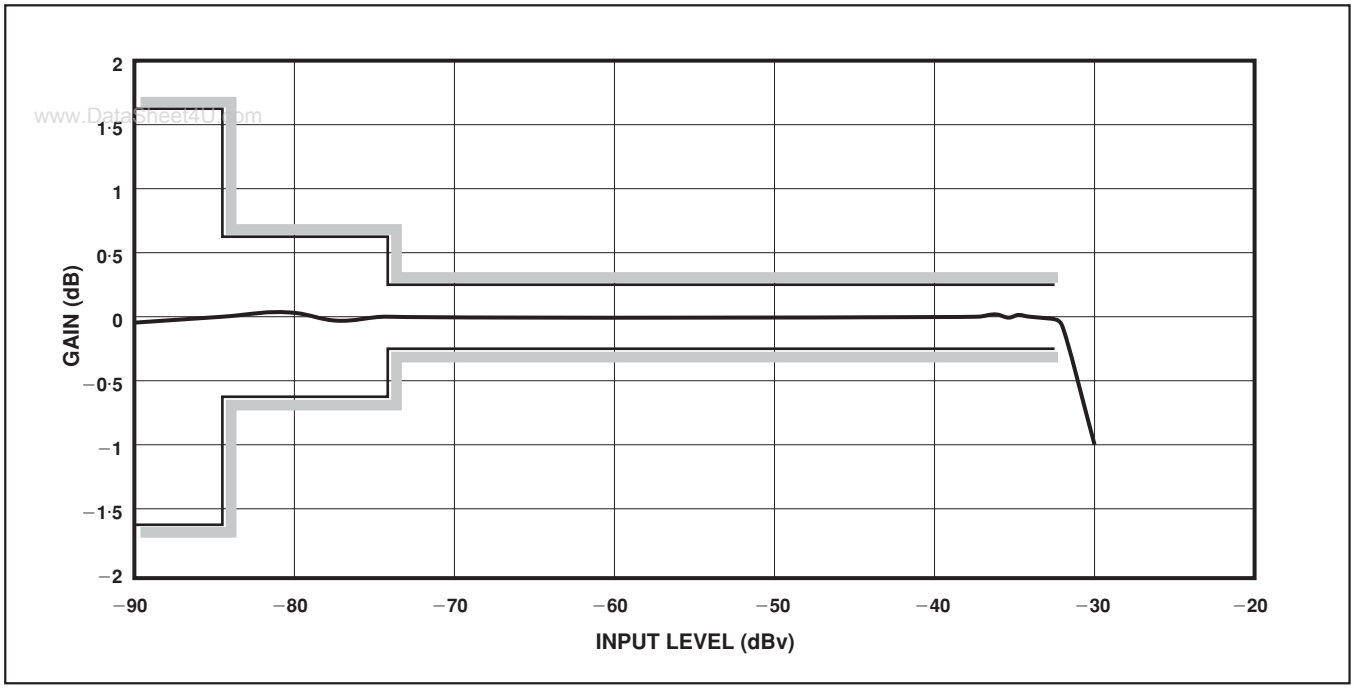


Fig. 10 Typical transmit path gain v. input level. Signal frequency = 1·0kHz

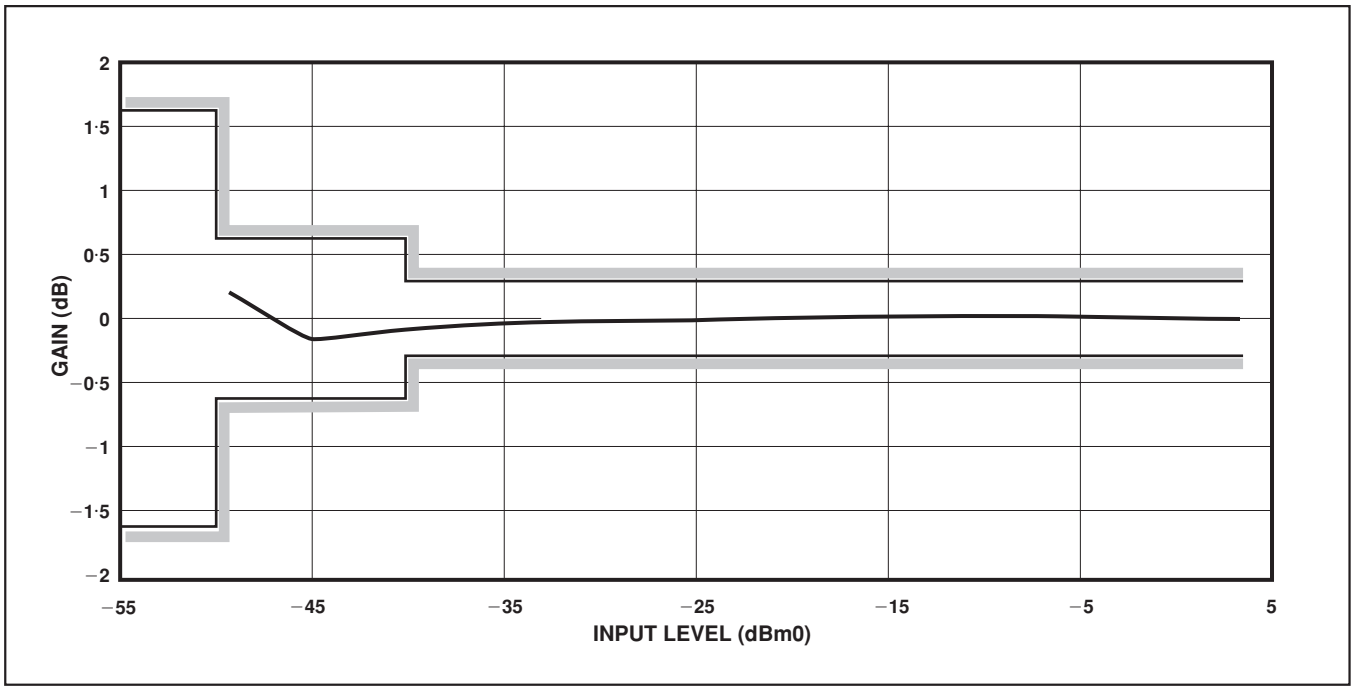


Fig. 11 Typical receive path gain v. input level. Signal frequency = 1·0kHz

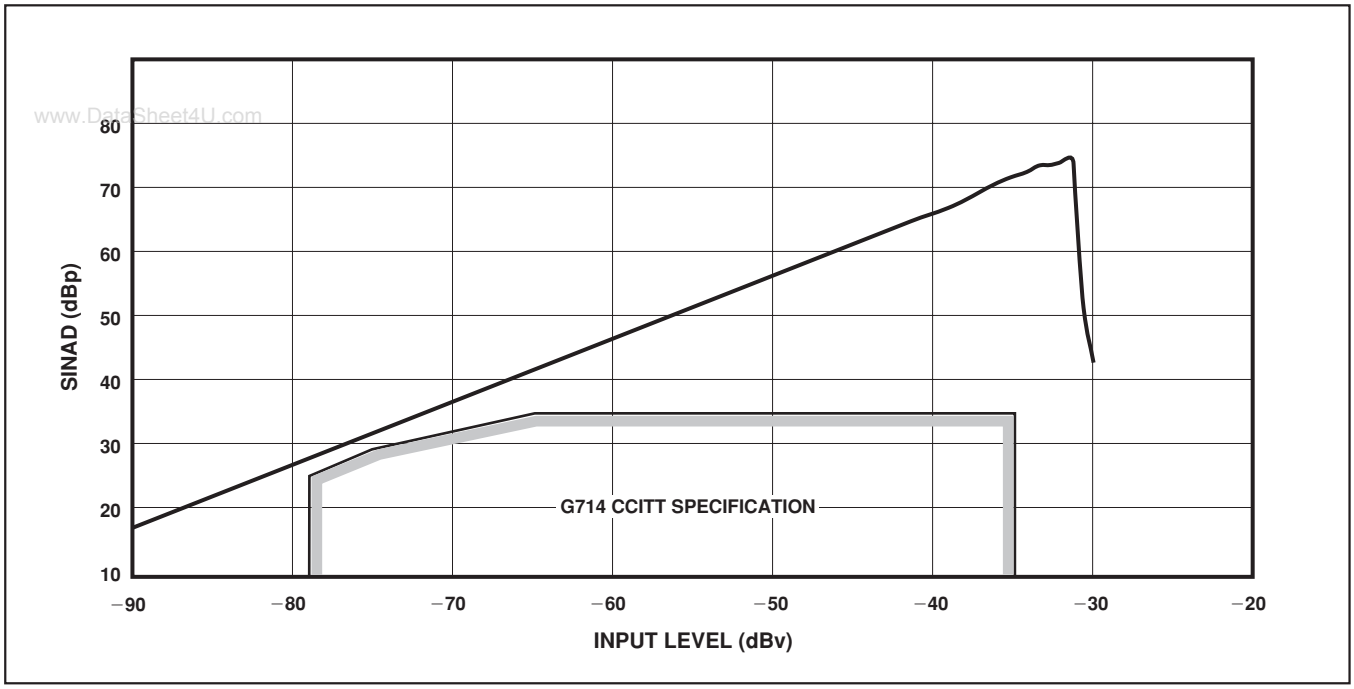


Fig. 12 Typical transmit path SINAD v. input level. Signal frequency = 1·0kHz

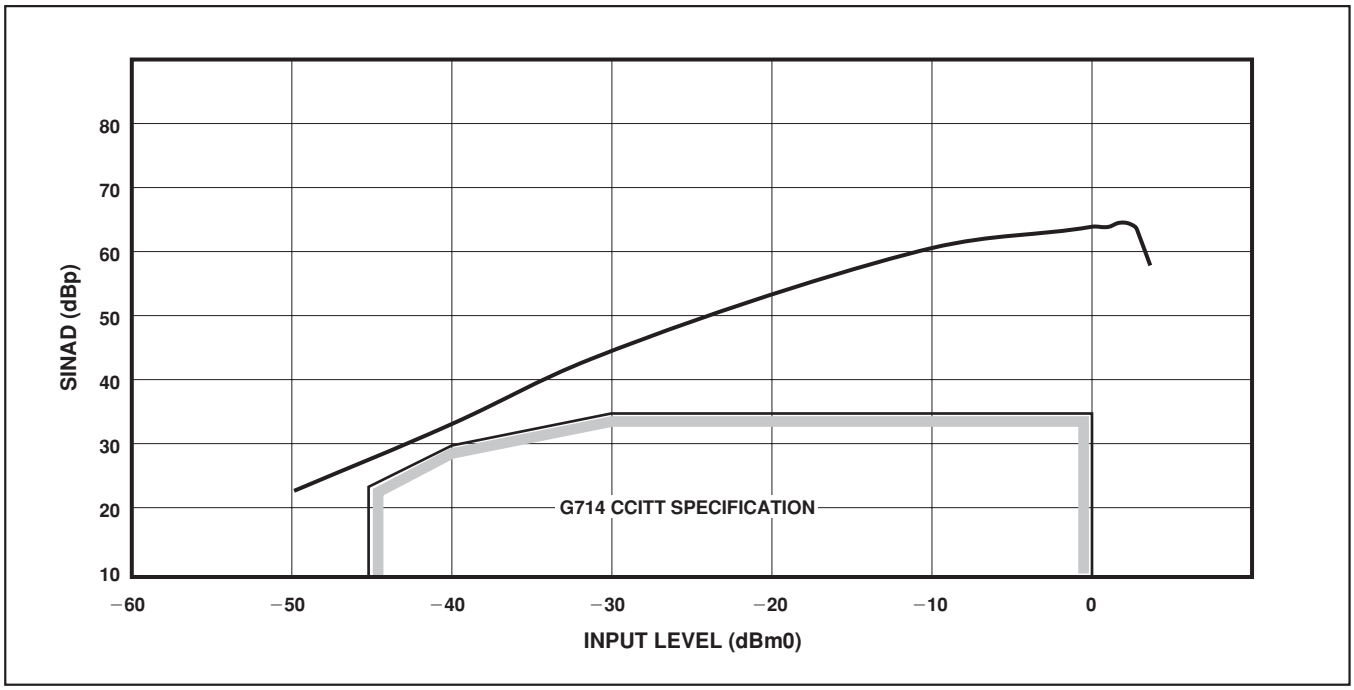


Fig. 13 Typical receive path SINAD v. input level, over full specification range. Signal frequency = 1·0kHz

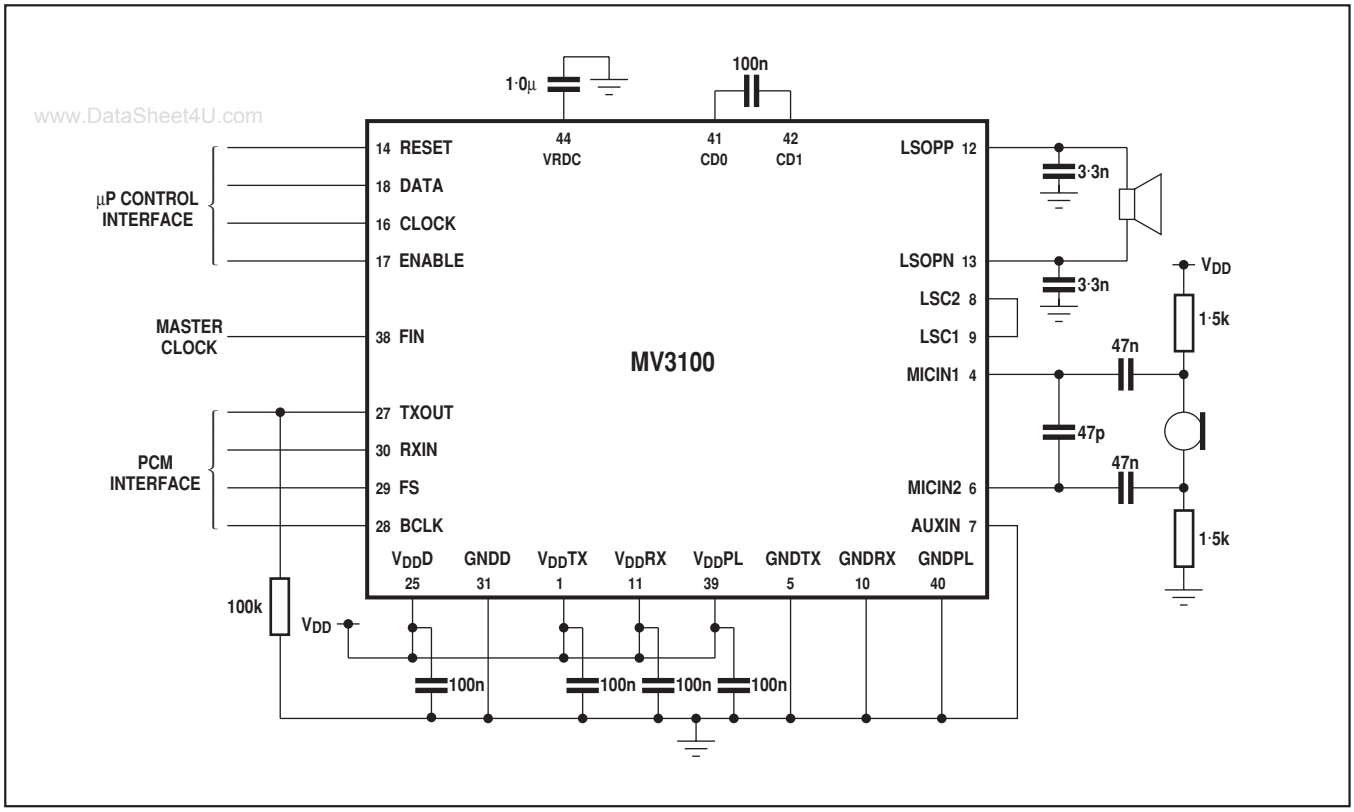
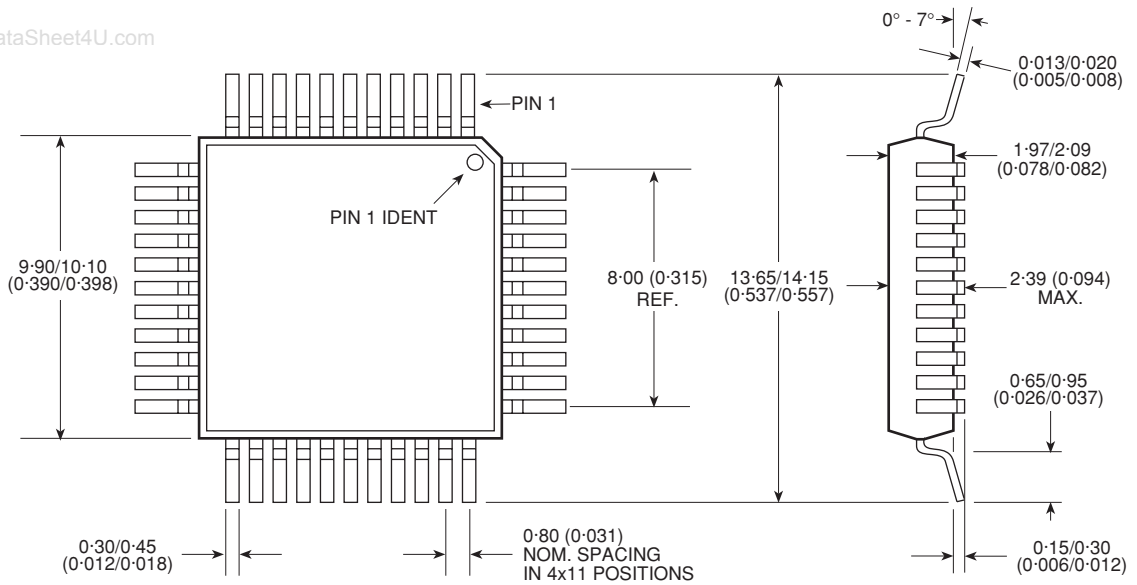


Fig. 14 Typical handset application circuit

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



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