PLESSEY Semiconductors — CMOS

MV3506 A-LAW CODEC WITH FILTER
MV3507 μ-LAW CODEC WITH FILTER
MV3507A μ-LAW CODEC WITH FILTER AND A/B SIGNALLING

The MV3506 and MV3507 are silicon gate CMOS Companding Encoder/Decoder integrated circuits designed to implement the per channel voice frequency Codecs used in PCM systems. The chips contain the band-limiting filters and the analogue to digital conversion circuits that conform to the desired transfer characteristic. The MV3506 provides the European A-Law companding and the MV3507 provides the North American μ-Law companding characteristic.

These circuits provide the interface between the analogue signals of the subscriber loop and digital signals of the PCM highway in a digital telephone switching system. The devices operates from dual power supplies of ±5V.

For a sampling rate of 8kHz, PCM input/output data rate can vary from 64kb/s to 2.1Mb/s. Separate transmit/receive timing allows synchronous or asynchronous operation.

In 22-pin packages (0.400in centres) the MV3506/MV3507 are ideally suited for PCM applications: Exchange, PABX, Channel Bank or Digital Telephone as well as fibre optic and other non-telephone uses. A 28 pin version, the MV3507A, provides standard μ-Law A/B signalling capability.

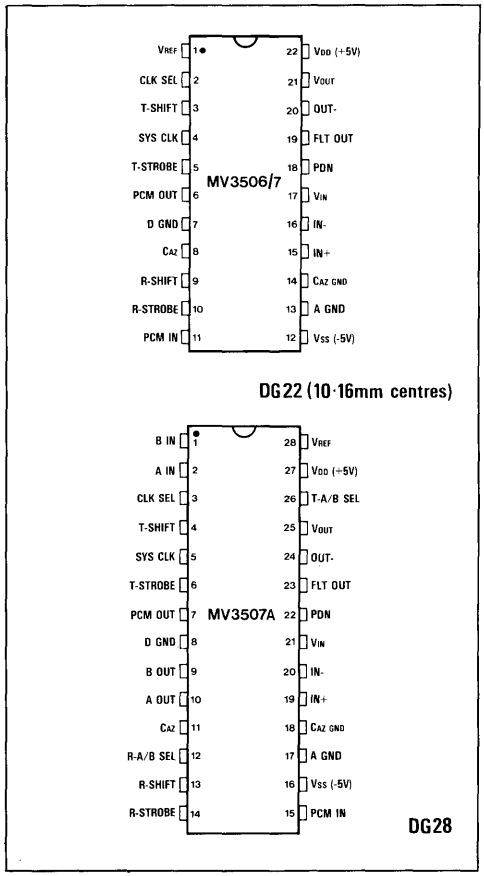


Fig.1 Pin connections - top view

FEATURES

- Independent Transmit and Receive Sections with 75dB Isolation
- Low power CMOS 80mW (Operating) 10mW (Standby)
- Stable Voltage Reference On-chip
- Meets or Exceeds AT&T D3, and CCITT G.711, G.712 and G.733 Specifications
- Input Analogue Filter Eliminates Need for External Anti-aliasing Prefilter
- Input/Output Op. Amps for Programming Gain
- Output Op. Amp Provides ±3.1V Into a 1200 Ohms load or Can Be Switched Off for Reduced Power (70mW)
- Special Idle Channel Noise Reduction Circuitry
- Encoder has Dual-speed Auto-zero Loop for Fast Acquisition on Power-up
- Low Absolute Group Delay = 410μsec. at 1kHz

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage V_{DD}: +6.0V
DC Supply Voltage V_{SS}: -6.0V
Operating Temperature: -40°C to +125°C
Storage Temperature: -65°C to +150°C
Power Dissipation at 25°C: 1000mW
Digital Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3
Analogue Input: V_{SS} -0.3≤V_{IN}≤V_{DD} -0.3

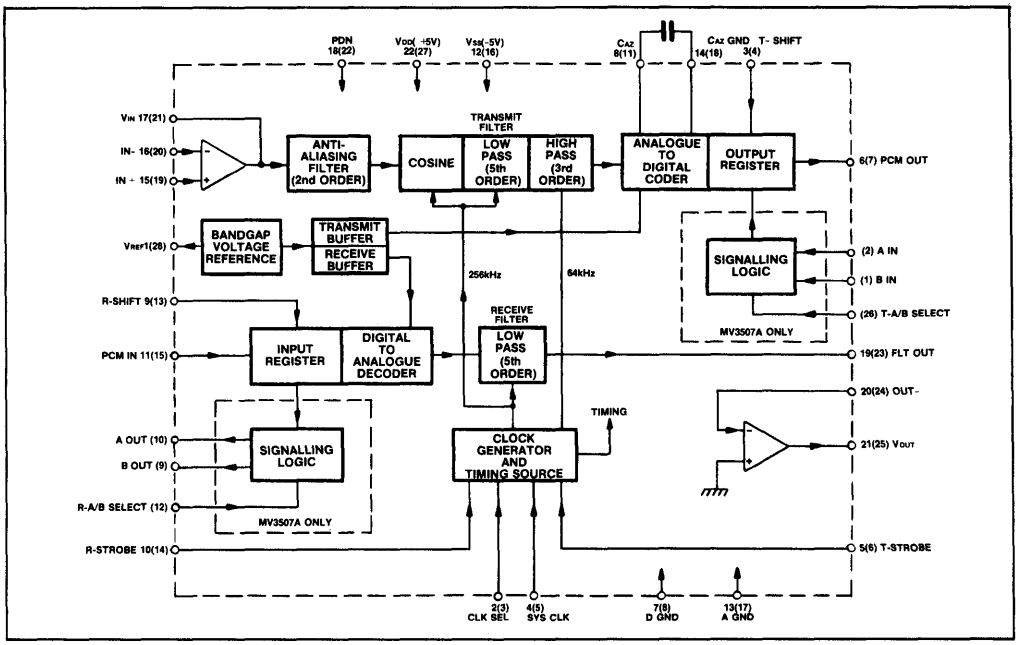


Fig.2 MV3506/MV3507/MV3507A block diagram. Pin numbers for the MV3507A are shown in brackets.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{amb} = 0°C to +70°C

Power Supply Requirements

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Positive supply	V_{DD}	4.75	5.0	5.25	V	
Negative supply	V_{SS}	-4.75	-5.0	-5.25	V	
Power dissipation (operating)	P_{OPR}		80	110	mW	V_{DD} = 5.0V, V_{SS} = -5.0V
Power dissipation (operating w/o output op. amp	P_{OPR}		70		mW	
Power dissipation (standby)	P_{STBY}		10	20	mW	

AC Characteristics (see Fig. 6)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
System clock duty cycle	D_{SYS}	40	50	60	%	At 1.544MHz or 2.048MHz
Shift clock frequency	f_{SC}	0.064		2.048	MHz	
Shift clock duty cycle	D_{SC}	40	50	60	%	
Shift clock rise time	t_{rc}			100	ns	
Shift clock fall time	t_{fc}			100	ns	
Strobe rise time	t_{rs}			100	ns	
Strobe fall time	t_{fs}			100	ns	
Shift clock to strobe (On) delay	t_{sc}	-100	0	200	ns	
Strobe width	t_{sw}	600ns		124.3μs		At 2.048MHz,700ns min at 1.544MHz
Shift clock to PCM out delay	t_{cd}		100	150	ns	
Shift clock to PCM in set-up time	t_{dc}	60			ns	
PCM output rise time C_L = 100pF	t_{rd}		50	100	ns	To 3V;510Ω to V_{DD}
PCM output fall time C_L = 100pF	t_{fd}		50	100	ns	To 0.4V;510Ω to V_{DD}
A/B select to strobe trailing edge	t_{dss}	100			ns	

DC Characteristics at V_{DD} = +5V, V_{SS} = -5V, V_{ref} = -3.075V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Analogue input resistance	R_{INA}	100			kΩ	
Input capacitance	C_{IN}		7	15	pF	All logic and analogue inputs
Logic input low current (Shift clock, PCM IN, System clock)	I_{INL}			1	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			1	μA	V_{IH} = 2.0V
Logic input low current (Strobe, A/B Sel, A IN B IN, PDN)	I_{INL}			600	μA	V_{IL} = 0.8V
Logic input high current	I_{INH}			600	μA	V_{IH} = 2.0V
Logic input 'low' voltage	V_{IL}			0.8	V	
Logic input 'high' voltage	V_{IH}	2.0			V	
Logic output 'low' voltage (PCM out)	V_{OL}			0.4	V	510Ω pull-up to V_{DD} + 2 LS TTL
Logic output 'low' voltage (A/B out)	V_{OL}			0.4	V	I_{OL} = 1.6mA
Logic output 'high' voltage	V_{OH}	2.6			V	I_{OH} = 40μA
Output load resistance V_{OUT}	R_L	1200			Ω	C_L = 50pF max.

Transmission Delays

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Encoder			125		μs	From T_{STROBE} to the start of digital transmitting
Decoder		30	8T+25		μs	T = Period in μs of R_{SHIFT} CLOCK
Transmit section filter				182	μs	At 1kHz
Receive section filter				110	μs	At 1kHz

MV3506 Single-Chip A-Law Filter/Codec Linear Characteristics

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		-85	-73	dBm0p	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			-78	dBm0p	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-30	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk $V_{IN-VOUT}$		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	R_L = 1.2kΩ
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

MV350(7)A Single-Chip μ-Law Filter/Codec Linear Characteristics

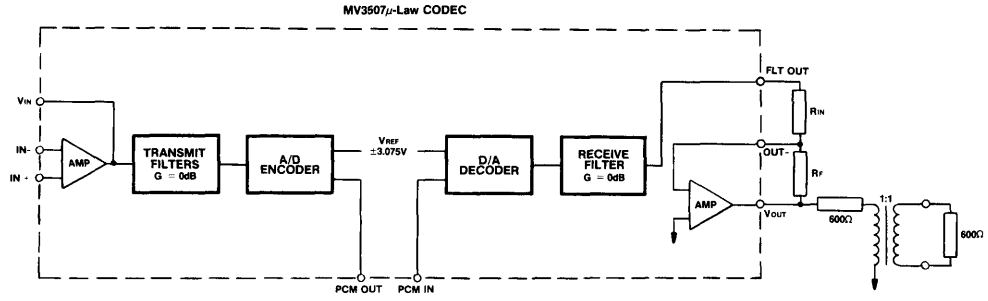
Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Idle channel noise (weighted noise)	ICN_W		5	17	dBrnc0	CCITT G.712 5.1
Idle channel noise (single frequency noise)	ICN_{SF}			-60	dBm0	CCITT G.712 5.2
Idle channel noise (receive section)	ICN_R			15	dBrnc0	CCITT G.712 5.3
Spurious out-of-band signals at the channel output				-28	dBm0	CCITT G.712 7.1
Intermodulation (2 tone method)	IMD_{2F}			-35	dBm0	CCITT G.712 8.1
Intermodulation (1 tone + power frequency)	IMD_{PF}			-49	dBm0	CCITT G.712 8.2
Spurious in-band signals at the channel output port				-40	dBm0	CCITT G.712 10
Inter-channel crosstalk V_{IN}-V_{OUT}		75	80		dB	CCITT G.712 12
Max.coding analogue input level	$V_{IN}(max)$		±3.1		V_{0pk}	
Max.coding analogue output level	$V_{OUT}(max)$		±3.1		V_{0pk}	R_L = 1.2kΩ
Gain variation with temperature and power supply	ΔG		±0.25		dB	
Transmit gain repeatability			±0.1	±0.2	dB	
Receive gain repeatability			±0.1	±0.2	dB	
Zero transmission level point (decoder) (see Fig. 3)	$0TLP_R$		+5.8		dBm	V_{OUT} Digital milliwatt response
Zero transmission level point (encoder)	$0TLP_T$		+5.8		dBm	V_{IN} to yield same as digital milliwatt response at decoder

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
SYS CLK	4	5	**System Clock** This pin is a TTL compatible input for either a 1.544MHz or a 2.048MHz clock that is divided down to provide the filter clocks. The status of CLK SEL pin must correspond to the provided clock frequency.
T-SHIFT	3	4	**Transmit Shift Clock** This TTL compatible input shifts PCM data out of the coder on the positive going edges after receiving a positive edge on the T-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
R-SHIFT	9	13	**Receive Shift Clock** This TTL compatible input shifts PCM data into the decoder on the negative going edges after receiving a positive edge on the R-STROBE input. The clocking rate can vary from 64kHz to 2.048MHz.
T-STROBE	5	6	**Transmit Strobe** This TTL compatible pulse input (8kHz) is used for analogue sampling and for initiating the PCM output from the coder. It must be synchronised with the T-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of this signal is not critical. An internal bit counter generates the necessary timing for PCM output.
R-STROBE	10	14	**Receive Strobe** This TTL compatible pulse input (typ. 8kHz) initiates clocking of PCM input data into the decoder. It must be synchronised with the R-SHIFT clock with its positive going edges occurring after the falling edge of the shift clock. The width of the signal is not critical. An internal bit counter generates necessary timing for PCM input.
CLK SEL	2	3	**Clock Select** This pin selects the proper divide ratios to utilise either 1.544MHz or 2.048MHz as the system clock. The pin is tied to V_{DD} (+5V) for 2.048MHz and to V_{SS} (-5V) for 1.544MHz operation. If this pin is connected to DGND, 256kHz may be used as the system clock.
PCM OUT	6	7	**PCM Output** This is a LS TTL compatible open-drain output. It is active only during transmission of PCM output for 8-bit periods of T-SHIFT clock signal following a positive edge on the T-STROBE input. Data is clocked out by the positive edge of the T-SHIFT clock into one 510Ω pull-up per system plus 2 LS TTL inputs.
PCM IN	11	15	**PCM Input** This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of T-SHIFT clock.

PIN/FUNCTION DESCRIPTIONS

Name	Pin		Description
	MV3506/ MV3507	MV3507A	
C_{AZ}	8	11	**Auto Zero Capacitor** A capacitor of 0.1μF ±20% should be connected between these pins for coder auto zero operation.
C_{AZ}GND	14	18	Sign bit of the PCM data is integrated and fed back to the comparator for DC offset cancellation.
V_{REF}	1	28	*Output of the internal* **Band-gap Reference Voltage** *(-3.075V) generator is* brought out to V_{REF} pin.
IN +	15	19	**Analogue input.** IN- and IN + are the inputs of a high input impedance op. amp and V_{IN} is the output of this op. amp. These three pins allow the user complete control over the input stage so that it can be connected as a unity gain amplifier, amplifier with gain, amplifier with adjustable gain of as a differential input amplifier. The adjustable gain configuration will facilitate calibration of the transmit channel. channel.
IN-	16	20	
V_{IN}	17	21	
FLT OUT	19	23	**Filter Out** This is the output of the low pass filter which represents the recreated analogue signal from the received PCM data words. The filter sample frequency of 256kHz is down 37dB at this point. This is a high impedance output which can be used by itself or connected to the output amplifier stage which has a low output impedance. It should not be loaded by less than 20kΩ.
OUT-	20	24	**Output and input of the uncommitted output amplifier stage.** Signal at the FLT OUT pin can be connected to this amplifier to realise a low output impedance with unity gain, increased gain or reduced gain. This allows easier calibration of the receive channel. The V_{OUT} pin has the capability of driving 0dBm into 600Ω load. (See Fig. 3.) If OUT- is connected directly to V_{SS} the op. amp will be powered down, reducing power consumption by 12mW, typically.
V_{OUT}	21	25	
V_{DD}	22	27	**Power supply pins.** V_{DD} and V_{SS} are positive and negative supply pins, respectively (typ. +5V, -5V).
V_{SS}	12	16	
A GND	13	17	**Analogue and Digital Ground pins** are separate for minimising crosstalk and digital interference.
D GND	7	8	
PDN	18	22	**Power Down** This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
A IN		2	The **Transmit A/B select** input (T-A/B SEL) selects the **A signal** input in a positive transition and the **B signal** input on the negative transition. These inputs are TTL compatible. The A/B signalling bits are sent in bit 8 of the PCM word in the frame following the frame in which T-A/B SEL input makes a transition. A common A/B select input can be used for all channels in a multiplex operation, since it is synchronised to the T-STROBE input in each device.
B IN		1	
T-A/B SEL		26	
A OUT		10	In the decoder the A/B signalling bits received in the PCM input word are latched to the respective outputs in the same frame in which the **Receive A/B select (R-A/B SEL)** input makes a transition. A bit is latched on a positive transition and B bit is latched on a negative transition. A common A/B select input can be used for all channels in a multiplex operation.
B OUT		9	
R-A/B SEL		12	



$$OTLP_{IN} = -\left[G - 20\log\left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= -\left[0 - 20\log\left(\frac{3.075}{1.58}\right)\right]$$

= +5.8dBm at the V_{IN} terminal

$$OTLP_{OUT} = \left[G + 20\log\left(\frac{V_{REF}}{1.58}\right)\right]$$

$$= \left[0 + 20\log\left(\frac{3.075}{1.58}\right)\right]$$

= +5.8dBm at the FLT_{OUT} terminal

(Note: The 1.58V value is that value of reference voltage that would allow the peak value of +3.17dBm as the maximum coded value, resulting in a OTLP of 0dBm. For A-Law it would be 1.57V for +3.14dBm.)

Since the output buffer amplifier is designed to drive 1200Ω, a 600Ω resistor in series with the 600Ω load divides the available voltage in half resulting in a $OTLP_{OUT}$ to the load of -0.2dBm.

For a system where OTLP is chosen to be 0dBm the input op. amp. should be configured for 5.8dB gain and the output op. amp. for 0.2dB gain. R_{IN} should be ⩾20kΩ.

Fig.3 MV3507 and MV3507A μ-law Codec input/output reference signal levels

Power Down Logic

Powering down the Codec can be done in several ways. The most direct is to drive the PDN pin to a low level. Stopping both the transmit strobe and the receive strobe will also put the chip into the stand-by mode. The strobes can be held high, low or disconnected.

Voltage Reference Circuitry

A temperature compensated band-gap voltage generator (-3.075V) provides a stable reference for the coder and decoder. Two amplifiers buffer the reference and supply the coder and decoder independently to minimise crosstalk. This reference voltage is trimmed to within ±27mV during assembly to ensure a minimum gain error of ±0.2dB due to all causes.

FUNCTIONAL DESCRIPTION

Figure 2 shows the simplified block diagram of the MV3506/MV3507. The device contains independent circuitry for processing transmit and receive signals. Switched capacitor filters provide the necessary bandwidth limiting of voice signals in both directions. Circuitry for coding and decoding operates on the principle of successive approximation, using charge redistribution in a binary weighted capacitor array to define segments and a resistor chain to define steps. A band-gap voltage generator supplies the reference level for the conversion process.

Transmit Section

Input analogue signals first enter the chip at the uncommitted op. amp terminals. This op. amp allows gain trim to be used to set 0TLP in the system. From the V_{IN} pin the signal enters the 2nd Order analogue anti-aliasing filter. This filter eliminates the need for any off-chip filtering as it provides attenuation of 34dB (typ) at 256kHz and 44dB (typ) at 512kHz. From the cosine filter the signal enters a 5th Order low-pass filter clocked at 256kHz, followed by a 3rd Order high-pass filter clocked at 64kHz. The resulting band-pass characteristics meet the CCITT G.711, G.712 and G.733 specifications. Some representative attenuations are 26dB (typ) from 0 to 60Hz and 35dB (typ) from 4.6kHz to 100kHz. The output of the high pass filter is sampled by a capacitor array at the sampling rate of 8kHz. The polarity of the incoming signal selects the appropriate polarity of the reference voltage. The successive approximation analogue-to-digital conversion process requires 9 1/2 clock cycles, or about 72μs. The 8 bit PCM date is clocked out by the transmit shift clock which can vary from 64kHz to 2.048MHz. A switched capacitor dual-speed, auto-zero loop using a small non-critical external capacitor (0.1μF) provides DC offset cancellation by integrating the sign bit of the PCM data and feeding it back to the non-inverting input of the comparator.

Included in the circuitry of the MV3507 is 'All Zero' code suppression so that negative input signal values between decision values numbers 127 and 128 are encoded as 00000010. This prevents loss of repeater synchronisation by TI line clock recovery circuitry as there are never more than 15 consecutive zeroes.

An additional feature of the Codec is a special circuit to eliminate any transmitted idle channel noise during quiet periods. When the input of the chip is such that for 250ms the only code words generated were +0, -0, +1 or -1, the output word will be a +0. The steady +0 state prevents alternating sign bits or LSB from toggling and thus results in a quieter signal at the decoder. Upon detection of a different value, the output resumes normal operation resetting the 250ms timer. This feature is a form of Idle Channel Noise 'Squelch' or 'Crosstalk Suppression'. It is of particular importance in the MV3506 A-Law version because the A-Law transfer characteristic has 'mid-riser' bias which enhances low level signals from crosstalk.

Receive Section

A receive shift clock, variable between the frequencies of 64kHz to 2.048MHz, clocks the PCM data into the input buffer register once every sampling period. A charge proportional to the received PCM data word appears on the decoder capacitor array. A sample and hold initialised to zero by a narrow pulse at the beginning of each sampling period integrates the charge and holds for the rest of the sampling period. A switched-capacitor 5th Order low-pass filter clocked at 256kHz smooths the sampled and held signal. It also performs the loss equalisation to compensate for the sin x/x distortion due to the sample and hold operation. The filter output is available for driving electronic hybrids directly as long as the impedance is greater than 20kΩ. When used in this fashion the low impedance output amp can be switched off for a considerable savings in power consumption. When it is required to drive a 600Ω load the output is configured as shown in Fig. 3 allowing gain trimming as well as impedance matching. With this configuration a transmission level of 0dBm can be delivered into the load with the +3.14dB or +3.17dB overload level being the maximum expected level.

Timing Requirements

The internal design of the Single-Chip Codec paid careful attention to the timing requirements of various systems. In North America, central office and channel bank designs follow the American Telephone and Telegraph Company's TI Carrier PCM format to multiplex 24 voice channels at a data rate of 1.544Mb/s. PABX designs, on the other hand, may use their own multiplexing formats with different data rates. Nevertheless, in digital telephone designs, Codec's may be used in a non-multiplexed form with a data rate as low as 64kb/s. The MV3507 and MV3507A fulfil these requirements.

In Europe, telephone exchange and channel bank designs follow the CCITT carrier PCM format to multiplex 30 voice channels at a data rate of 2.048Mb/s. The MV3506 is designed for this market and will also handle PABX and digital telephone applications requiring the A-Law transfer characteristics.

The timing format chosen for the Plessey Codec allows operation in both multiplexed or non-multiplexed form with data rates variable from 64kb/s to 2.048Mb/s. Use of separate internal clocks for filters and for shifting of PCM input/output data allows the variable data rate capability. Additionally, the MV3506/MV3507 does not require that the 8kHz transmit and receive sampling strobes be exactly 8 bit periods wide. The device has an internal bit counter that counts the number of data bits shifted. It is reset on the leading (+)edges of the strobe, forcing the PCM output in high impedance state after the 8th bit is shifted out. This allows the strobe signal to have any duty cycle as long as its repetition rate is 8kHz and transmit/receive shift clocks are synchronised to it. Figures 4 and 5 show the waveforms in typical multiplexed uses of the Codec.

System Clock

The basic timing of the Codec is provided by the system clock. This 2.048MHz or 1.544MHz clock is divided down internally to provide the various filter clocks and the timing for the conversions. In most systems this clock will also be used as the shift clock to clock in and out the data. However, the shift clock can actually be any frequency between 64kHz and 2.048MHz as long as one of the two system clock frequencies is provided. Independent strobes and shift clocks allow asynchronous operation of transmit and receive.

Signalling In μ-Law Systems

The MV3506 and MV3507 are compact 22-pin devices to meet the two worldwide PCM standards. In μ-Law systems there can be a requirement for signalling information to be carried in the bit stream with the coded analogue data. This coding scheme is sometimes called 7 5/6 bit rather than 8 bit because of the LSB every 6th frame being replaced by a signalling bit. This is referred to as A/B Signalling and if a signalling frame carries the 'A' bit, then 6 frames later the LSB will carry the 'B' bit. To meet this requirement, the MV3507A is available in a 28-pin package, as 6 more pins are required for the inputs and outputs of the A/B signalling.

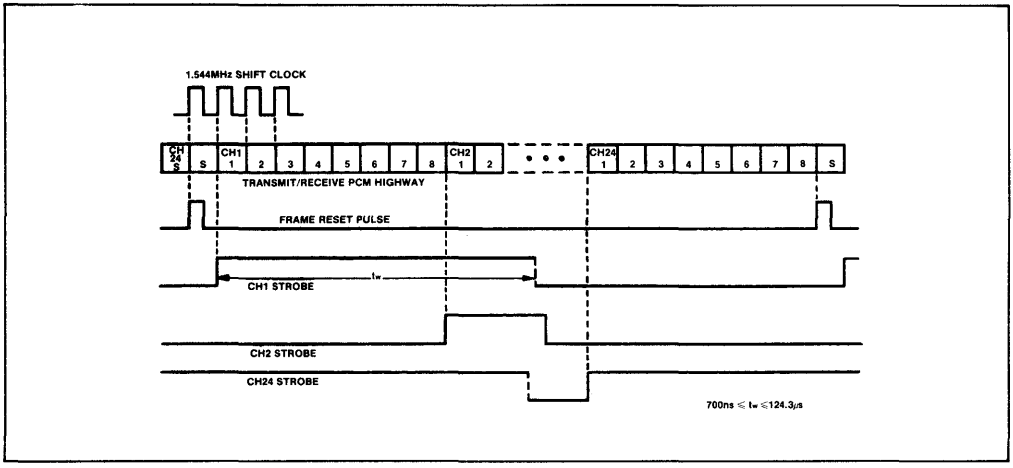


Fig.4 Waveforms in a 24 channel PCM system

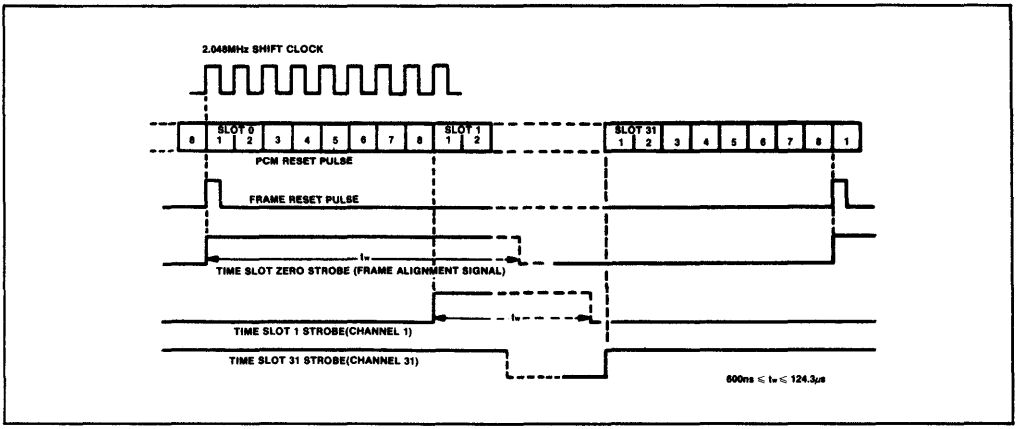
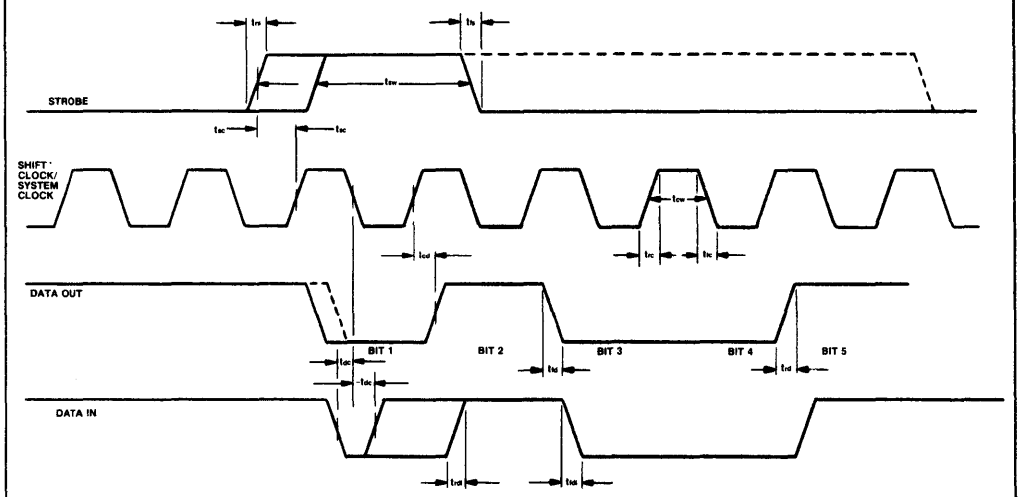


Fig.5 Waveforms in a 30 channel PCM system



*In this example the shift clock is the system clock (1.544 or 2.048MHz). In systems where the data shift rate is not the same the relationship of each to the strobe remains the same. The system clock and shift clock need not have coincident edges, but must relate to the strobe within the t_{sc}, timing requirements.
The effect of the strobe occurring after the shift clock is to shorten the first (sign) bit at the data output.
The length of the strobe is not critical. It must be at a logic state longer than one system clock cycle. Therefore, the minimum would be >488ns at 2.048 and the maximum <124.3μsec at 1.544MHz.

Fig.6 Waveform details

	Min.	Max.
t_{cw}	195nsec	9.38μsec
t_{rs}		100ns
t_{fs}		100ns
t_{sc}	-100ns	200ns**
t_{rc}		100ns
t_{fc}		100ns
t_{sw}	600ns*	124.3μsec
t_{cd}	100ns	150ns
t_{dc}	60ns	
t_{rdi}		100ns
t_{fdi}		100ns

*At 2.048MHz, 700ns at 1.544MHz
**That is, the strobe can produce the shift clock by 200ns, or follow it by as much as 100ns.

Signalling Interface

In the AT&T TI carrier PCM format an A/B signalling method conveys channel information. It might include the on-or-off hook status of the channel, dial pulsing (10 or 20 pulses per second), loop closure, ring ground, etc., depending on the application. Two signalling conditions (A and B) per channel, giving four possible signalling states per channel are repeated every 12 frames (1.5 milliseconds). The A signalling condition is sent in bit 8 of all 24 channels in frame 6. The B signalling conditions is sent in frame 12. In each frame, bit 193 (the S bit) performs the terminal framing function and serves to identify frames 6 and 12.

The MV3507A in a 28-pin package is designed to simplify the signalling interface. For example, the A/B select input pins are transition sensitive. The Transmit A/B select pin selects the A signal input on a positive transition and the B signal input on the negative transition. Internally, the device synchronises the A/B select input with the strobe signal. As a result, a common A/B select signal can be used for all 24 transmit channels in the channel bank. The A and B signalling bits are sent in the frame following the frame in which the A/B select input makes the transition. Therefore, A/B select input must go positive in the beginning of frame 5 and negative in the beginning of frame 11 (see Fig. 7).

The decoder uses a similar scheme for receiving the A and B signalling bits, with one difference. They are latched to the respective outputs in the same frame in which the A/B select input makes a transition. Therefore, the Receive A/B select input must go high at the beginning of frame 6 and go low at the beginning of frame 12.

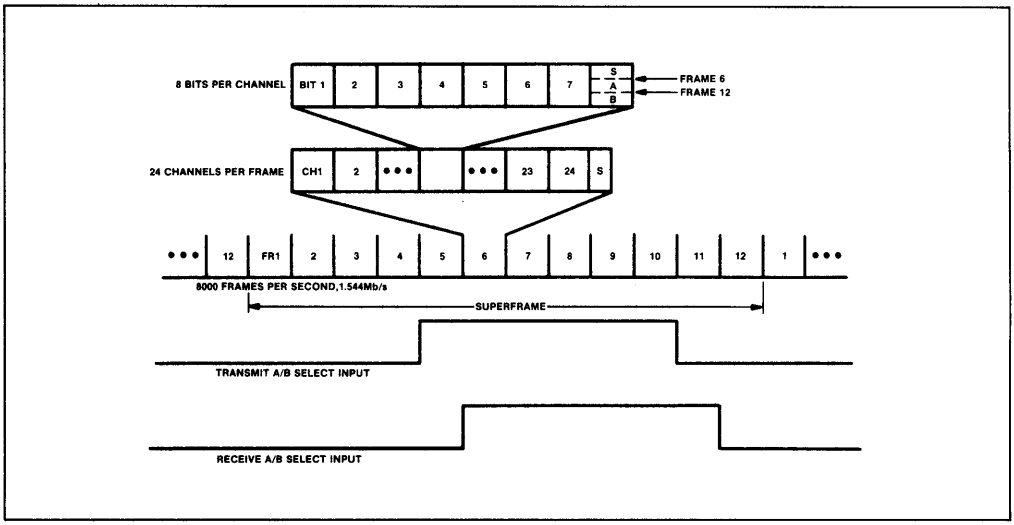


Fig.7 Signalling waveforms in a TI carrier system

In the TI carrier system, 24 voice channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel plus a framing bit called the S bit form a 193 bit frame. Since each channel is sampled 8000 times per second, the resultant data rate is 1.544Mb/s. Within the channel bank the transmit and receive channels of a Codec can occupy the same time slot for a synchronous operation or they can be independent of each other for asynchronous operation. Asynchronous operation helps minimise switching delays through the system. Since the timing interface for the coder and decoder sections is independent of each other in the MV3507A, it can be operated in either manner.

In the CCITT carrier system 30 voice channels and 2 framing and signalling channels are multiplexed to form the transmit and receive PCM highways, 8 data bits from each channel. Since each channel is sampled 8000 times per second, the resultant data rate is 2.048Mb/s.

The line supervision and control circuitry within each subscriber line interface can generate all the timing signals for the associated Codec under control of a central processor. Alternatively, a common circuitry within the channel bank can generate the timing signals for all channels. Generation of the timing signals for the MV3506 and MV3507A is straightforward because of the simplified timing requirements (see timing requirements for details). Figures 9 and 10 show design schemes for generating these timing signals in a common circuitry. Note that only three signals; a shift clock, a frame reset pulse (coincident with the S bit) and a superframe reset pulse (coincident with the S bit in Frame 1) are needed. These signals are generated by clock recovery circuitry in the channel bank. Since the Plessey Codec does not need channel strobes to be exactly 8-bit periods wide, extra decoding circuitry is not needed.

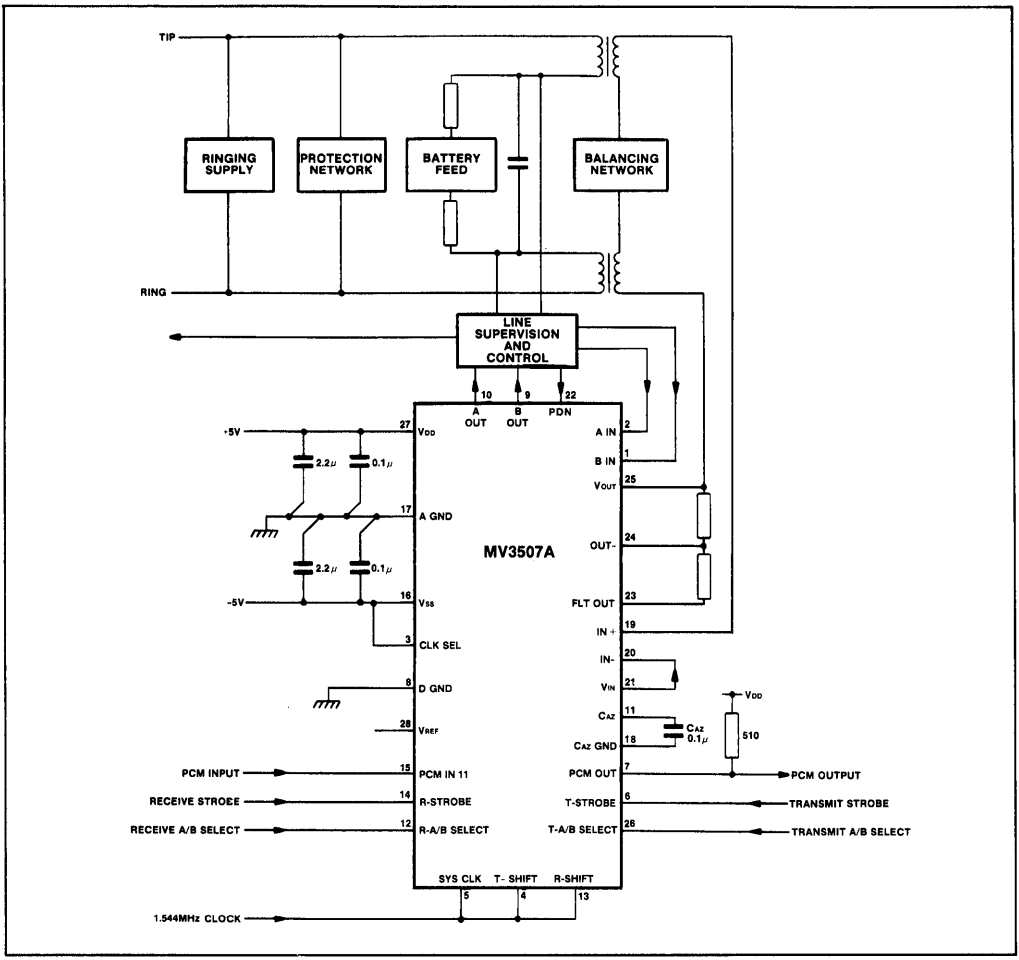


Fig.8 A subscriber line interface circuit

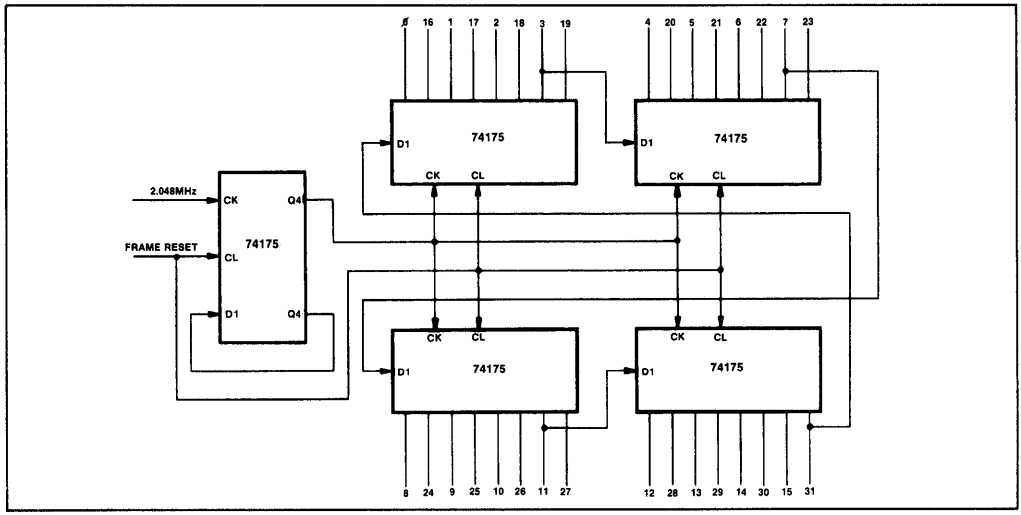


Fig.9 Generating timing signals in a CCITT carrier system (30 + 2 channels)

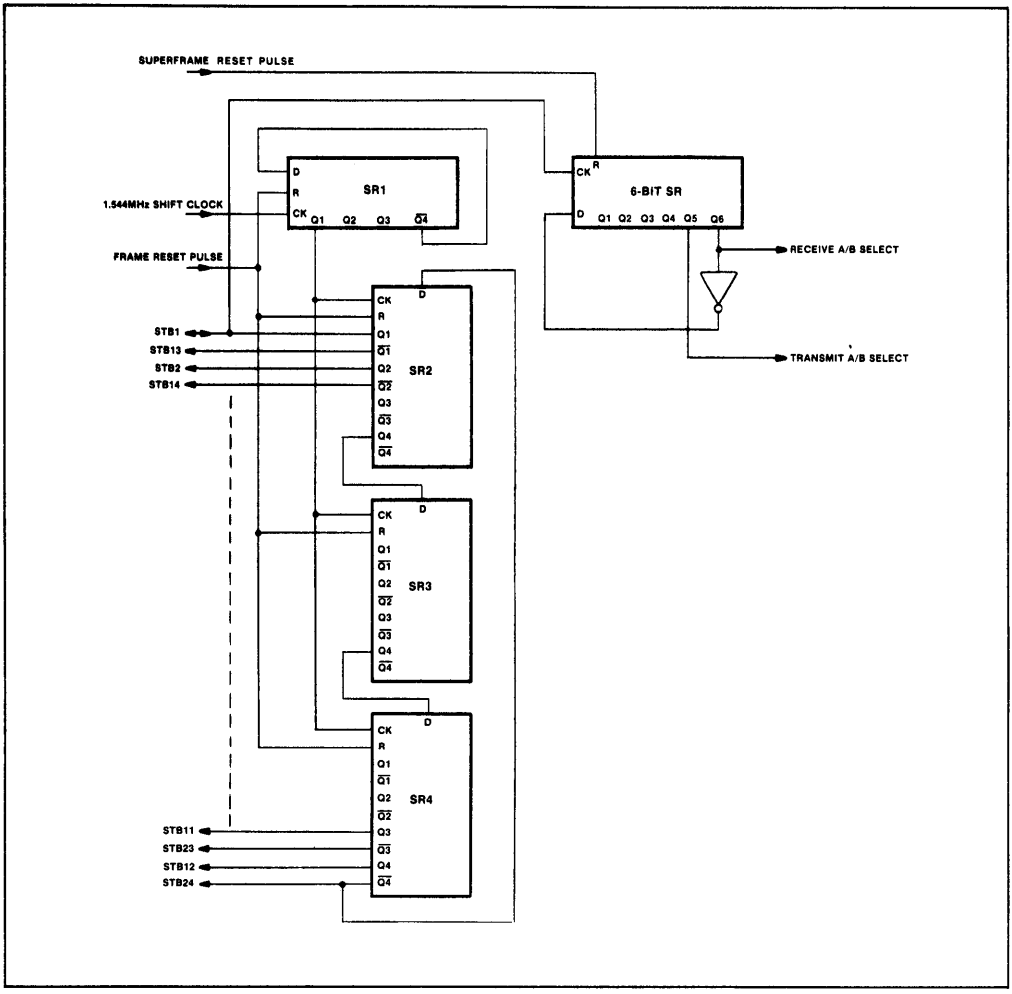


Fig.10 Generating timing signals in a TI carrier system

A Digital Telephone Application

Most new PABX designs are using PCM techniques for voice switching with an increasing trend toward applying them at the telephone level. The simplest form of a digital telephone design uses four wire pairs of interface to the switch. Two pairs carry transmit and receive PCM voice date. One pair supplies an 8kHz synchronising clock signal and the remaining pair supplies power to the telephone. More sophisticated techniques minimise the number of wire pairs. The Plessey Single-Chip Codec is ideally suited for this application because of the low component count and its simplified timing requirements. Figure 11 shows a schematic for a typical digital telephone design.

Since asynchronous operation is not necessary, transmit and receive timing signals are common. A phase-lock-loop derives the 2048kHz system clock and 64kHz shift clock from the 8kHz synchronising signal received from the switch. The synchronising signal also serves as the transmit/receive strobe signal since its duty cycle is not important for Codec operation. Microphone output directly feeds into the coder input while the decoder output drives the receiver through an impedance transformer to complete the design.

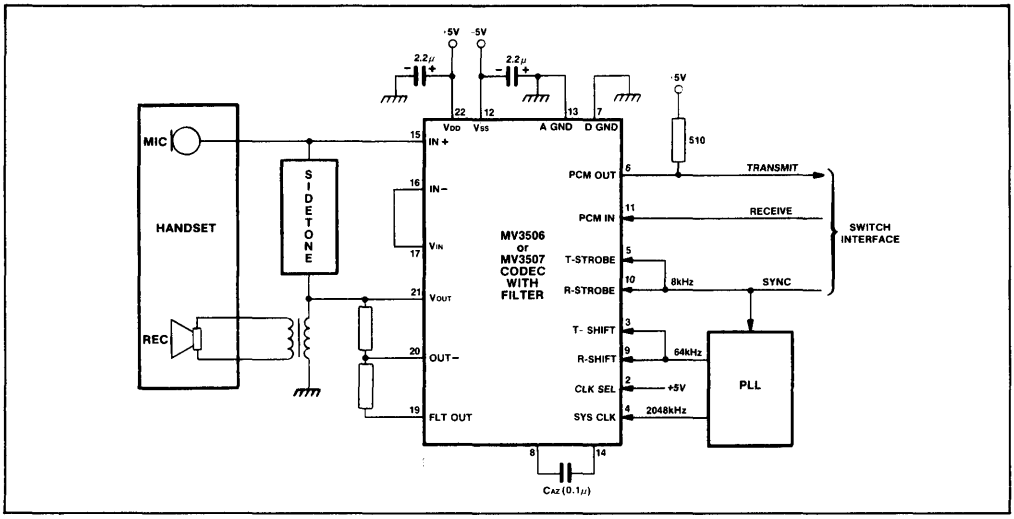


Fig.11 Voice processing in a digital telephone application