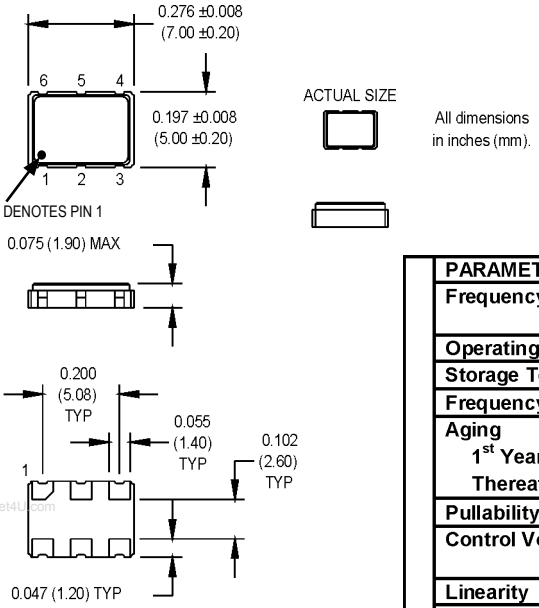
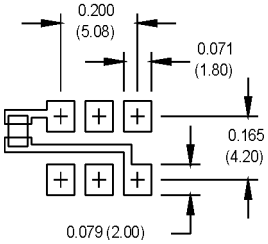
MV3 & MV5 Series

5x7 mm, 3.3 or 5.0 Volt, HCMOS, VCXO

- **General purpose VCXO with good performance at an affordable price**



SUGGESTED SOLDER PAD LAYOUT



Pin Connections

PIN	FUNCTION
1	Control Voltage
2	N/C or Tristate
3	Ground
4	Output
5	N/C
6	+Vdd

Ordering Information

MV3/MV5 | 1 | 3 | V | C | N | 00.0000 MHz

Product Series
MV3 = 3.3 Volt
MV5 = 5.0 Volt

Temperature Range
1: 0°C to +70°C **2:** -40°C to +85°C
6: -20°C to +70°C

Stability
3: ±100 ppm **4:** ±50 ppm
6: ±25 ppm* **8:** ±20 ppm*

Output Type
V: Voltage Controlled - no tristate
T: Voltage Controlled - tristate

Symmetry/Logic Compatibility
C: 45/55 CMOS **G:** 40/60 CMOS

Package/Lead Configurations
N: Leadless Ceramic

Frequency (customer specified)

*Consult Factory for availability

Electrical Specifications

PARAMETER	Symbol	Min.	Typ.	Max	Units	Condition/Notes
Frequency Range	F	1.544		167	MHz	MV3 See Note 4
		1.544		45	MHz	MV5 See Note 4
Operating Temperature	T_A	(See ordering information)				
Storage Temperature	T_S	-45		+95	°C	
Frequency Stability	ΔF/F	(See ordering information)				
Aging						
1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
Pullability		±80			ppm	Over control voltage
Control Voltage	Vc	0.3	1.65	3.0	V	MV3
		0.5	2.5	4.5	V	MV5
Linearity				15	%	Positive Monotonic Slope
Modulation Bandwidth	fm	10			kHz	-3 dB bandwidth
Input Impedance	Zin	50k			Ohms	
Input Voltage	Vdd	3.135	3.3	3.465	V	MV3
		4.5	5.0	5.5	V	MV5
Input Current	Idd					
1.544 to 36 MHz				20	mA	MV3
36 to 167 MHz				50	mA	MV3
1.544 to 50 MHz				35	MA	MV5
Output Type						HCMOS
Load				15	pF	See Note 1
Symmetry (Duty Cycle)		(See ordering information)				50% Vdd Level
Logic "1" Level	Voh	90			% Vdd	HCMOS load
Logic "0" Level	Vol			10	% Vdd	HCMOS load
Rise/Fall Time	Tr/Tf					See Note 2
1.544 to 60 MHz				5	ns	MV3
60 to 167 MHz				2	ns	MV3
1.544 to 50 MHz				5	ns	MV5
Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z				
Start up Time			4		ms	
Phase Jitter	ΦJ					See Note 3
20 – 45 MHz			0.5	1.0	ps RMS	Integrated 12 kHz - 20 MHz
45 – 167 MHz			3.0	5.0	ps RMS	Integrated 12 kHz - 20 MHz
Phase Noise (Typical)	**10 Hz**	**100 Hz**	**1 kHz**	**10 kHz**	**100 kHz**	**Offset from carrier**
@ 19.44 MHz	-70	-100	-132	-140	-150	dBc/Hz

1. See load circuit diagram #2.
2. Rise/Fall times are measured between 10% Vdd and 90% Vdd with HCMOS load.
3. Contact factory for non-standard jitter requirements.
4. Contact factory for frequencies outside of the ranges shown.

MtronPTI Lead Free Solder Profile