PLESSEY Semiconductors — CMOS

MV4325

PROGRAMMABLE KEYPAD PULSE DIALLER

The MV4325 Keypad Pulse Dialler contains all the logic necessary to interface a 2 of 7 keypad and convert this key information to control and mute pulses simulating a telephone rotary dial. The MV4325 has programmable access pause capability to provide automatic interruption of dialling needed when accessing the toll network, WATS line or public network. The device is fabricated using Plessey Semiconductors' ISO-CMOS technology which enables the device to function down to 2.0V making it ideal for long loop operation.

The MV4325 will accept up to 20 digits and access pauses and will redial stored information at a later time by activation of # key. Device current in standby is less than 1μA at 1.0V.

The MV4325 is available in Ceramic DIL (DG, -40°C to +85°C).

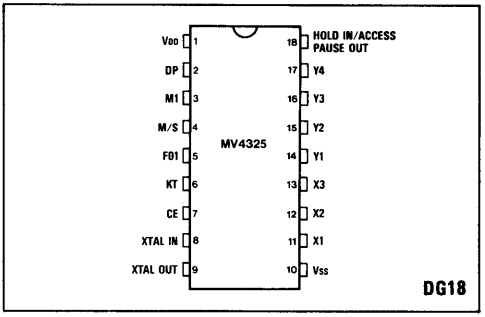

Fig.1 Pin connections (top view)

APPLICATIONS

- Pushbutton Telephones with Last Number Redial
- Repertory Dialers
- Tone to Pulse Converters

FEATURES

- Last Number Redial
- Multiple Access Pause Programming
- Any Valid Keypad Input or HOLD IN Causes Exit from Access Pause
- Oscillator Start Up Controlled from Keypad Input
- Oscillator Power Down whilst not Dialling
- 300 Hz Key Tone indicates Valid Key
- 2.0V to 7.0V Supply Voltage Operating Range
- Stores up to 20 Digits and Access Pauses
- Digit Memory Retained down to 1.0V at 1μA
- Selectable Mark/Space Ratio 66⅔ : 33⅓ or 60 : 40
- 10Hz Dialling Speed (932Hz Fast Test) :)

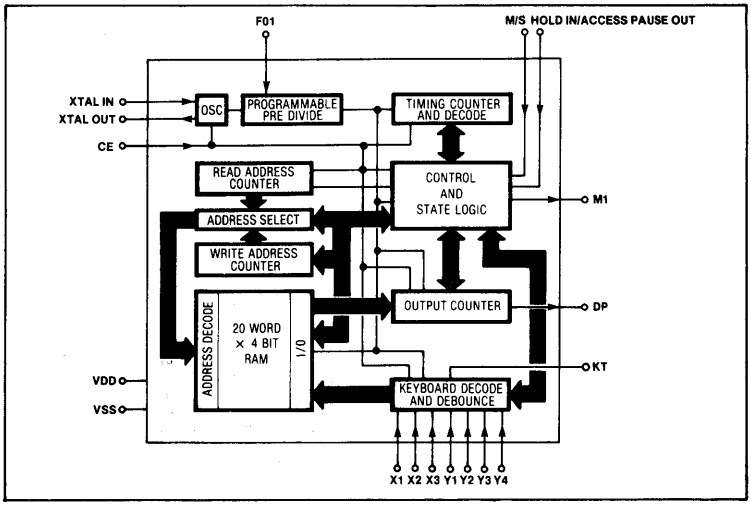

Fig.2 MV4325 function diagram

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

	MIN	MAX		MIN	MAX
$V_{DD}-V_{SS}$	-0.3V	10V			
Voltage on any pin	V_{SS}-0.3V	V_{DD} + 0.3V			
Current at any pin		10mA			
Operating Temperature	-40°C	+85°C	Power Dissipation		1000mW
Storage Temperature	-65°C	+ 150°C			

* Derate 16mW/°C above 75°C. All leads soldered to PC board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C, f_{CLK} = 3.579545MHz; V_{DD} = +3.0V
All voltages wrt V_{SS}

		CHARACTERISTIC		SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS	
1	SUPPLY	Supply Voltage Operating Range		V_{DD}	2.0		7.0	V		
2		Standby Supply Current		I_{DDS}			1.0	μA	CE = M/S = F01 = HOLD IN = V_{SS}, V_{DD} = 1.0V	
3		Operating Supply Current		I_{DD}		100	150	μA	3.579545 MHz Crystal, $C_{XTALOUT}$ = 12pF	
4	INPUT	Pull-Up Transistor Source Current		I_{IL}	-0.5	-3.0	-12	μA	$V_{IN} = V_{SS}$	X_1, X_2, X_3
5		Input Leakage Current		I_{IH}		0.1		nA	$V_{IN} = V_{DD}$	Y_1, Y_2, Y_3, Y_4
6		Input Leakage Current		I_{IL}		-0.1		nA	$V_{IN} = V_{SS}$	M/S, F01
7		Pull-Down Transistor Sink Current		I_{IH}	0.5	3.0	8.0	μA	$V_{IN} = V_{DD}$	
8		Input Low Level Voltage		V_{IL}			0.9	V	All inputs	
9		Input High Level Voltage		V_{IH}	2.1			V		
10	OUTPUT	Voltage Levels	Low-Level	V_{OL}		0	0.01	V	No Load	
11			High-level	V_{OH}	2.99	3		V		
12		Drive Current	N-Channel	I_{OL}	0.8	2.0		mA	V_{OUT} = 2.3V	DP, M_1, M_2, KT
13				I_{OL}	0.2	0.5		mA	V_{OUT} = 0.5V	
14			P-Channel Source	I_{OH}	-0.8	-2.0		mA	V_{OUT} = 0.7V	
15				I_{OH}	-0.2	-0.5		mA	V_{OUT} = 2.5V	
16	IN/OUTPUT	Input Low Level Voltage		V_{IL}			0.9	V		
17		Input High Level Voltage		V_{IH}	2.1			V		
18		Output Low Level Current		I_{OL}		15		μA	V_{OUT} = 0.5V	CE,
19		Output High Level Current		I_{OH}		-12		μA	V_{OUT} = 2.5V	HOLD IN/ACCESS
20		Input Force High Current (from V_{OL})		I_{FH}		55		μA	V_{IN} = 2.5V	PAUSE OUT
21		Input Force Low Current (from V_{OH})		I_{FL}		-70		μA	V_{IN} = 0.5V	

* Typical parametric values are for Design Aid Only, not guaranteed and not subject to production testing. Timing waveforms are subject to production functional test.

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

$T_{amb} = +25°C$; $f_{CLK} = 3.579545\,MHz$; $V_{DD} = +3.0V$

		CHARACTERISTIC	SYMBOL	MIN	TYP*	MAX	UNITS	TEST CONDITIONS
1	DYNAMIC	Output Rise Time	t_R		1.0		µs	DP, M_1
2		Output Fall Time	t_F		1.0		µs	C_L = 50pF
3		Maximum Clock Frequency	f_{CLK}	3.58			MHz	3.579545 MHz Crystal
4		Mark to Space Ratio	M/S		2:1			M/S = O/C (V_{SS})
5					3:2			M/S = V_{DD}
6		System Clock Frequency (Internal)			300		Hz	F01 = V_{SS}
7		Impulsing Rate = I/T			10		Hz	F01 = V_{SS}
8		Fast Test Impulsing Rate			14.9		Hz	F01 = V_{DD}
9		Clock Start Up Time	t_{on}		1.5	4	ms	Timed from CE ↑ '1'
10		Input Capacitance	C_{in}		5.0		pF	Any Input

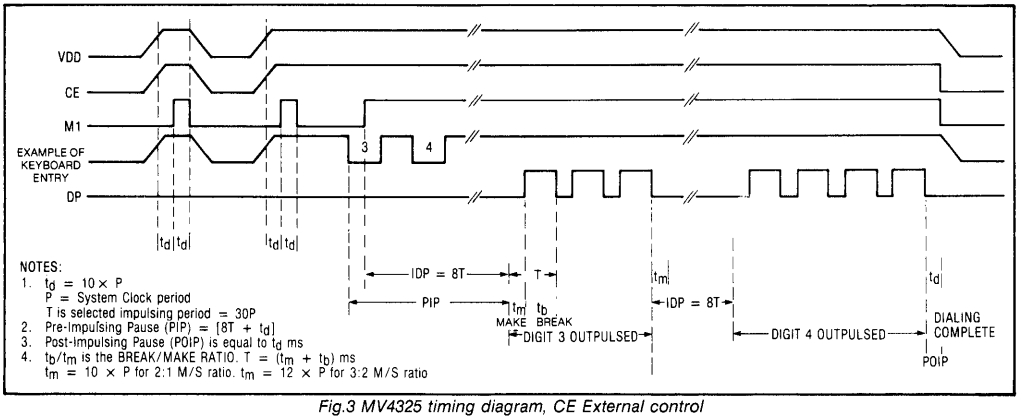

Fig.3 MV4325 timing diagram, CE External control

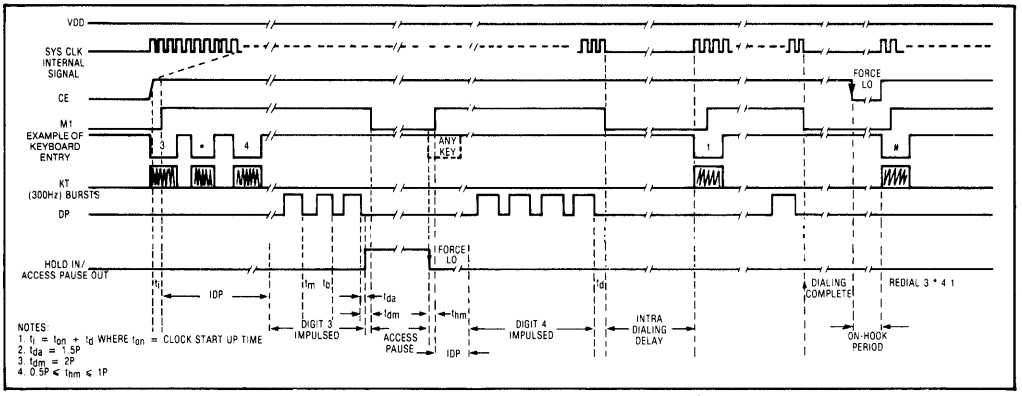

Fig.4 MV4325 timing diagram, CE Internal control

PIN FUNCTIONS

V_{DD}	Positive voltage supply				
DP	Dial Pulsing Output Buffer				
M1	Mute Output Buffer				
M/S	Mark/Space (Break/Make) Ratio select. On-chip pull-down transistor to V_{SS}. Note: O/C = Open Circuit			O/C	2:1
				V_{DD}	3:2
F01	Impulsing Rate Selection. On-chip pull-down transistor to V_{SS}. * Assumes f_{CLK} = 3.579545MHz.	F01	Nominal Impulsing Rate	Actual* Inpulsing Rate	System Clock frequency
		O/C	10Hz	10.13Hz	303.9Hz
		V_{DD}	932Hz	932.17Hz	27,965.1Hz
CE	Chip Enable. An active input. Control is internal via static keyboard decode, or by external forcing.				
XTAL IN	Crystal Input. Active, clamped low if CE = '0', high impedance if CE = '1'.				
XTAL OUT	Crystal Output. Buffer to drive crystal. Capacitive load on-chip.				
V_{SS}	System ground				
X_1,X_2,X_3	Column keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
Y_1,Y_2,Y_3,Y_4	Row keyboard Inputs. On-chip pull-up transistors to V_{DD}. Active LOW.				
HOLD IN/	INPUT/OUTPUT	O/C	Normal Operation		
ACCESS	INPUT	V_{DD}	No impulsing. If activated during impulsing, hold occurs when the current digit is complete.		
PAUSE OUT	OUTPUT	V_{DD}	Logic "1" level output indicates access pause condition.		
KT	300Hz	Square wave bursts indicate valid keypad input.			

No. of O/P Pulses	Digit	KEYPAD INPUT CODE Y_1	Y_2	Y_3	Y_4	X_1	X_2	X_3
1	1	0	1	1	1	0	1	1
2	2	0	1	1	1	1	0	1
3	3	0	1	1	1	1	1	0
4	4	1	0	1	1	0	1	1
5	5	1	0	1	1	1	0	1
6	6	1	0	1	1	1	1	0
7	7	1	1	0	1	0	1	1
8	8	1	1	0	1	1	0	1
9	9	1	1	0	1	1	1	0
10	0	1	1	1	0	1	0	1
RE-DIAL		1	1	1	0	1	1	0
ACCESS PAUSE		1	1	1	0	0	1	1

Table 1

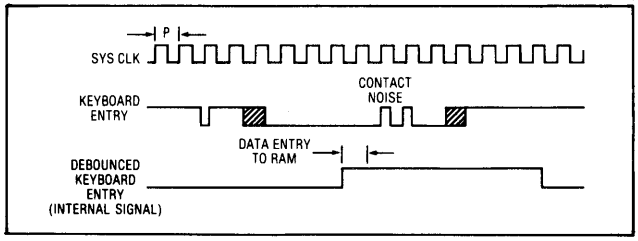

Fig.5 Keypad input debounce timing diagram

OPERATING NOTES

The MV4325 programmable keypad pulse dialer is optimized for use in key operated pulse dialling telephone sets and contains features which make it particularly suitable for applications where redial of last number dialled and repertory dial facilities are required.

Keypad information is accepted directly from a dual contact keypad having two single pole switches per key: one switch common to the column and one switch common to the row. The common row contacts are connected Y1 to Y4 and the common column contacts connected X1 to X3. The other side of each switch is connected to a common VSS line. The keypad code is shown in Table 1.

The MV4325 will accept up to 20 digits and access pauses, e.g. 18 digits plus 2 access pauses or alternately 19 digits plus 1 access pause. Prior to a keypad input being accepted contact bounce is eliminated by a circuit which ensures that any input which is valid for less than 10ms is rejected and any input valid for greater than 17ms is accepted as a valid key input. This circuit operates similarly on the trailing edge of a valid key input preventing multiple digit recognition in the presence of noise. Debounce operation is shown in Fig.5.

The first key entered in any dialling sequence initiates the oscillator on the MV4325 by internally taking CE high. Digits may be entered asynchronously from the keypad. Dialling and mute functions are output as shown in Fig.3 and Fig.4. Fig.3 shows use of the MV4325 with external control of CE. This mode is useful if a bistable latching relay is used to mute and switch the complete pulse dialer circuit. In this mode the pulse occurring on M1 when CE is taken high with no keypad input can be used to initiate the bistable latching relay.

Fig.4 shows the timing diagram of the MV4325 including access pause and redial mode. Initially CE is low and goes high on recognition of the first valid key input. Keypad data is entered asynchronously and dialling commences after recognition of the leading edge of the first valid key input. When an access pause is reached M1 goes low and Hold In/Access Pause Out goes high indicating the device is in an access pause. This output signal can be used to enable an external dial tone recognition circuit. Exit from the access pause is achieved by one of two methods. One method is by the next valid key operation. If a valid digit is entered, the digit will be entered in the next consecutive storage location in the digit memory. If the key # is activated, redialling of the number in memory will occur only if the device is in the redial mode. The alternative method to exit from an access pause is to pulse Hold In/Access Pause Out low, resetting the output latch associated with this input/output pin.

Fig.4 shows a pause in dialling between the completion of dialling digit 4 and keying digit 1. In this condition, the oscillator powers down to minimize power consumption and interfering signals, whilst CE remains high. On recognition of the next digit, the digit is entered in the next consecutive memory location and dialling resumes.

The end of a key entry sequence is indicated to the MV4325 by externally pulsing or clamping CE low. This causes the on-chip latch holding CE high to reset.

If the first key entered after a CE low period is #, redial of the last number dialled will occur. Access pause operation is as previously described. In the standby condition the MV4325 dissipates less than 1.0μW.

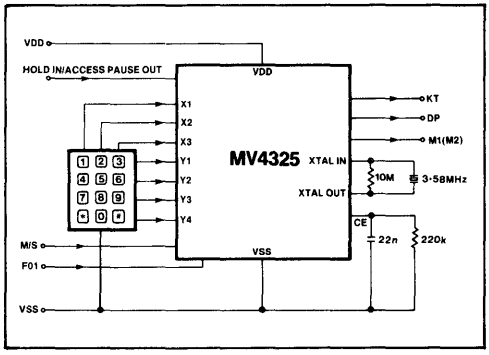

Fig.6 Application diagram