PLESSEY Semiconductors — ADVANCE INFORMATION CMOS

Advance information is issued to advise Customers of new additions to the Plessey Semiconductors range which, nevertheless, still have *'pre-production'* status. Details given may, therefore, change without notice although we would expect this performance data to be representative of *'full production'* status product in most cases. Please contact your local Plessey Semiconductors Sales Office for details of current status.

MV4330 MV4332

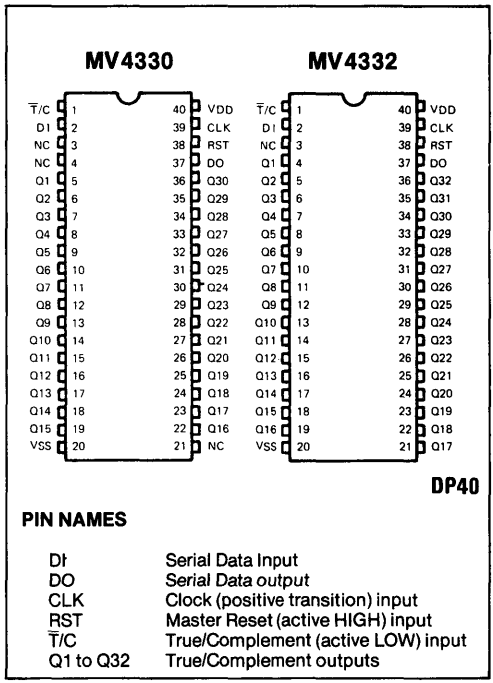
CMOS/LSI 30/32-BIT STATIC SHIFT REGISTERS WITH PARALLEL TRUE/COMPLEMENT OUTPUTS

The MV4330 and MV4332 are CMOS/LSI 30 and 32-bit static shift registers incorporating selectable true/complement outputs for each bit. These devices are well suited to drive LCD readouts directly since the AC signals required for the display may be generated simply by applying a low frequency signal directly to the True-Complement input pin and to the backplane of the display. One of these devices can drive four 7-segment displays or two 14-segment alpha-numeric displays plus decimal points or two 16-segment alpha-numeric displays directly.

The devices are available in 40-pin plastic DIL (DP) package.

FEATURES

- Direct LCD Drive
- CMOS Low Power (1 μA)
- 3 to 18 Volt Operation
- On-Chip Wave-Shaping
- High Speed (Typ. 3 MHz) Shift Register



PIN NAMES

DI	Serial Data Input
DO	Serial Data output
CLK	Clock (positive transition) input
RST	Master Reset (active HIGH) input
T/C	True/Complement (active LOW) input
Q1 to Q32	True/Complement outputs

Fig.1 Pin connections (top view)

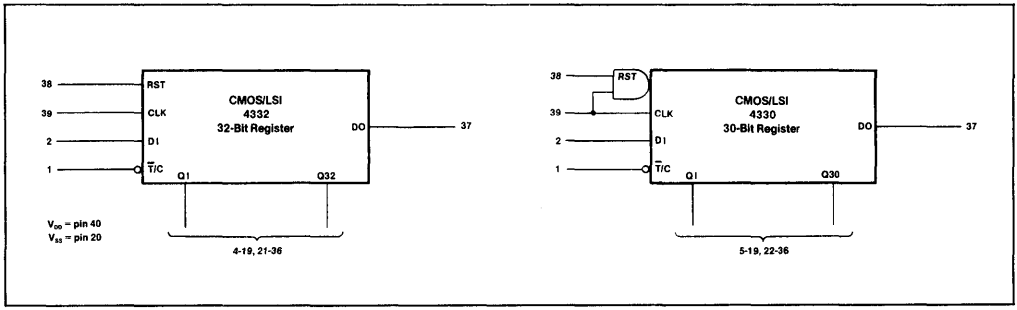


Fig.2 Block diagrams

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$

CHARACTERISTIC		SYMBOL	TEST CONDITIONS	VO Volts	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Quiescent Device Current		I_L			5	–	0.5	50	uA
					10	–	1	100	
Output Voltage	Low-Level	V_{OL}			5	–	0	0.01	V
					10	–	0	0.01	
	High-Level	V_{OH}			5	4.99	5	–	
					10	9.99	10	–	
Noise Immunity (Any Input)		V_{NL}		0.8	5	1.5	2.25	–	V
				1.0	10	3	4.5	–	
		V_{NH}		4.2	5	1.5	2.25	–	
				9.0	10	3	4.5	–	
Output Drive Current	D OUT	I_{DN}	N-Channel	0.5	5	0.8	1.7	–	mA
				0.5	10	1.0	3.0	–	
		I_{DP}	P-Channel	4.5	5	−0.35	−0.9	–	
				9.5	10	−0.8	−1.9	–	
	Q OUT	I_{DN}	N-Channel	0.5	10	50	250	–	uA
		I_{DP}	P-Channel	9.5	10	−50	−250	–	
Input Current		I_I				–	10	–	pA

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb} = +25°C$, $C_L = 50pF$
All input rise and fall times = 20ns

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	VDD Volts	LIMIT Min.	LIMIT Typ.	LIMIT Max.	UNIT
Propagation Delay Time	tPHL tPLH		10	–	300	–	ns
Transition Time	tTHL	D OUT (CL=50pF)	10	–	70	130	ns
	tTLH	Q OUT (CL=15pF)	10	–	300	–	ns
Maximum Clock Frequency	fCL		10	1.0	3.0	–	MHz
Minimum Clock Pulse Width	tWL tWH		10	–	200	–	ns
Minimum Reset Pulse Width	tWH(R)		10	–	200	–	ns
Input Capacitance	CI	Any Input		–	5	–	pF

Note 1.Voltages with respect to V_{SS}
Note 2.Typical temperature coefficient for all values = 0.3%/°C

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

PARAMETER	SYMBOL	LIMIT	UNIT
DC Supply Voltage	VDD	-0.5 to 18	V
Input Voltage	VIN	-0.5 to VDD+0.5	V
DC Current Drain per Pin	I	10	mA
Operating Temperature Range	TA	0 to 70	°C
Storage Temperature Range	Ts	-65 to 125	°C

OPERATING NOTES

The MV4330 and MV4332 accept a serial input DI which is shifted into the register on the positive transition of the clock (CLK) input. A feature of these devices is that the clock input and the true/complement control (T/C) input have wave-shaping circuits (Fig.3) to ensure fast edges on-chip regardless of the shape of the incoming signals.

The MV4330 also has the reset (RST) input gated with the clock input for synchronous reset on the positive transition of the clock. The MV4332 has asynchronous reset (RST) inputs which are active HIGH.

The parallel outputs of the shift registers are available in either true or complementary form dependent on the state of the true/complement control input. When input is logic-level LOW, the true form is available at all parallel outputs and when the input goes HIGH, the parallel outputs immediately revert to the complementary form of the data stored in each register. This action is independent of the clock input condition. A serial data (DO) output is provided for applications using longer shift registers, etc. This output is the true form of the last stage of the register.

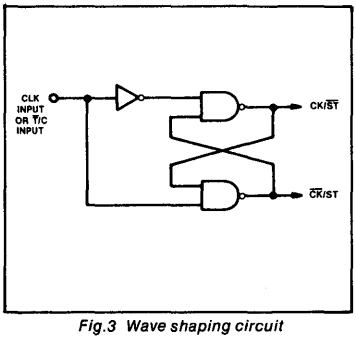


Fig.3 Wave shaping circuit

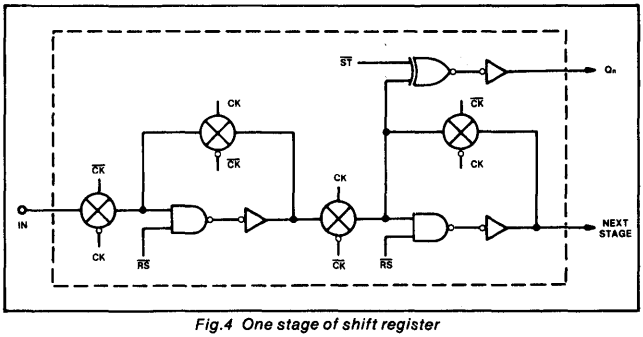


Fig.4 One stage of shift register

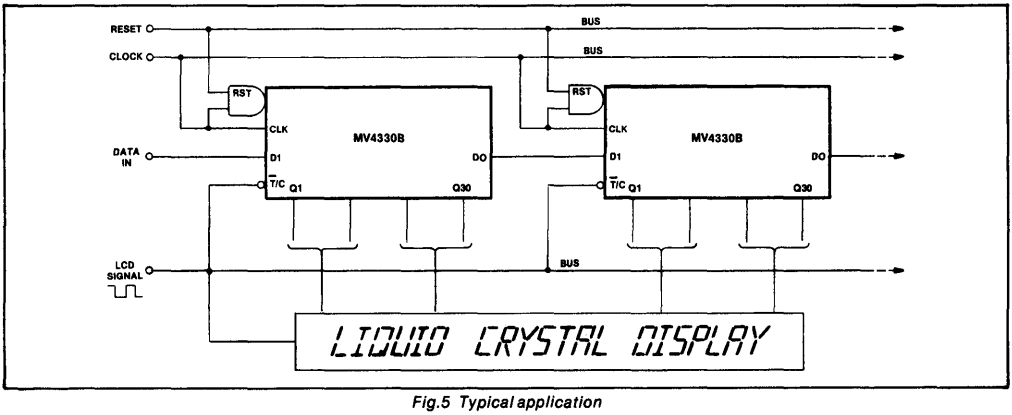


Fig.5 Typical application