PLESSEY Semiconductors — CMOS

MV8865

DTMF FILTER

The MV8865 contains both the high group and low group filtering and comparator functions required to implement a Dual Tone Multi Frequency tone receiver using a DTMF Digital Detector (i.e. MV8860/62/63). Switched capacitor techniques are used to implement the filters and the device is fabricated using Plessey Semiconductors' high density ISO/CMOS technology. The filter clocks are derived from an on-chip oscillator requiring only a low cost TV crystal as an external component. The MV8865 offers single supply operation over a wide supply voltage range and incorporates a logical power down facility.

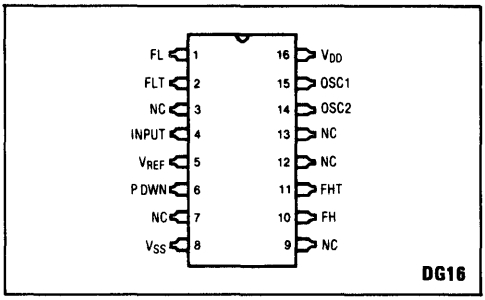

Fig.1 Pin connections (top view)

FEATURES

- Provides DTMF High and Low Group Filtering
- Hard Limiting on Filter Outputs
- 6 Pole Band Pass High and Low Group Filters
- 38 dB Intergroup Attenuation
- Dial Tone Suppression
- +5 to +12 V Single Supply Operation
- Logical Power Down
- Uses Inexpensive 3.58 MHz Crystal
- Wide Dynamic Range 30 dB
- Equivalent to MT8865X

APPLICATIONS

In DTMF Receivers for:

- End to End Signalling
- Control Systems
- PABX
- Central Office
- Mobile Radio
- Key Systems
- Tone to Pulse Converters

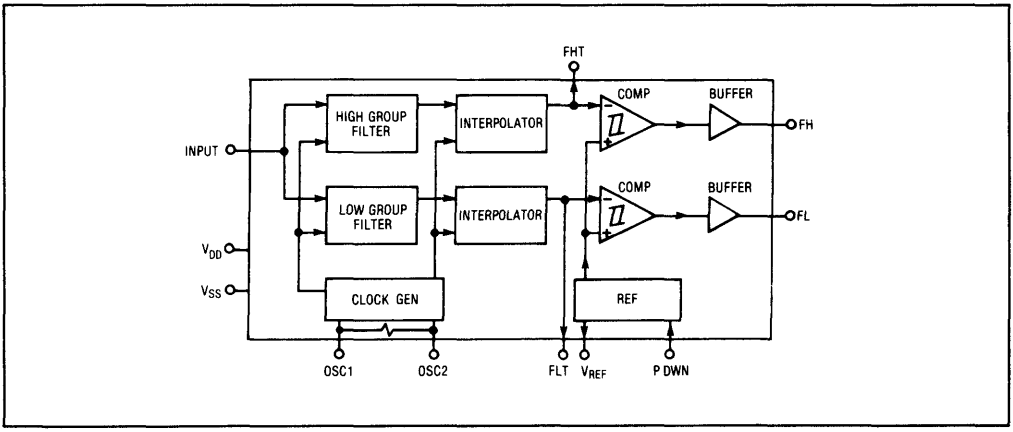

Fig.2 MV8865X functional block diagram

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
T_{amb} = +25°C; f_{CLK} = 3.579545 MHz
All voltages wrt V_{SS}

		Characteristic			Symbol	V_{DD} = 5V			V_{DD} = 12V			Unit	Test Conditions
						Min	Typ	Max	Min	Typ	Max		
1	SUPPLY	Operating Supply Voltage			V_{DD}	4.75					13	V	
2	SUPPLY	Operating Supply Current			I_{DD}		1.2	2.5		5	7.5	mA	PDWN = V_{SS}
3	SUPPLY	Standby Supply Current			I_{DDS}		100	150			400	µA	PDWN = V_{DD}
4	SUPPLY	Operating Power Consumption			P_O		6			60		mW	PDWN = V_{SS} Fig. 6(c)
5	SUPPLY	Standby Power Consumption			P_S		0.5			1.5		mW	PDWN = V_{DD} C = 15pF
6	INPUTS	Low Level Input Voltage		PDWN & OSC 1	V_{IL}			1.5			3.5	V	
7	INPUTS	High Level Input Voltage		PDWN & OSC 1	V_{IH}	3.5			8.5			V	
8	INPUTS	Pull Down Sink Current		PDWN	I_{IH}		3	6		12	24	µA	
9	INPUTS	Input Current		OSC 1	I_I		±2.5			±6		µA	
10	OUTPUTS	Low Level Output Voltage		FL, FH	V_{OL}			0.1			0.1	V	No load
11	OUTPUTS	High Level Output Voltage		OSC 2	V_{OH}	4.9			11.9			V	
12	OUTPUTS	Output Drive Current	N Channel Sink	FL, FH	I_{OL}	0.2			0.5			mA	V_{OL} = 0.4V (5V)
13	OUTPUTS			OSC 2		0.1			0.25			mA	V_{OL} = 1.2V (12V)
14	OUTPUTS		P Channel Source	FL, FH	I_{OH}	0.2			0.5			mA	V_{OH} = 4.6V (5V)
15	OUTPUTS			OSC 2		0.1			0.25			mA	V_{OH} = 10.8V (12V)

ABSOLUTE MAXIMUM RATINGS

The absolute maximum ratings are limiting values above which operating life may be shortened or specified parameters may be degraded.

Parameter		Min	Max		Parameter		Max
V_{DD} - V_{SS}			15	V	Power Dissipation	DG package[1]	850mW
Voltage on any pin		V_{SS} − 0.3	V_{DD} + 0.3	V			
Max. current at any pin			10	mA	[1]Derate 16mW/°C above 75°C		
Operating Temperature		40°C	+85	°C			
Storage Temperature	DG package	−65°C	+150	°C			

AC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
t_{amb} = +25°C; f_c = 3.579545 MHz; V_{DD} = 4.75 V to 13 V

		Characteristic		Symbol	Min	Typ	Max	Unit	Test Conditions	
1		Dynamic Range			30		36	dB		
2		Valid Input Signal Levels					$V_{DD}/2$	V_{pp}		
3		(Each tone of composite signal)			27.9		883	mVrms	V_{DD} = 5V	
4					67.5		2120	mVrms	V_{DD} = 12V	
5		Input Impedance		Z_I	10			MΩ		
6		Low Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
7		Low Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
8	F	High Group Sensitivity (1)			-28.85			dBm	V_{DD} = 5V	
9	L	High Group Sensitivity (1)			-21.25			dBm	V_{DD} = 12V	
10	T	Intergroup	Low Group with	IR_{L1209}	34	45		dB	1209Hz	w.r.t.
11	E		High Tone	IR_{L1477}	36	40		dB	1477Hz	770Hz
12	R	Rejection	High Group with	IR_{H941}	38	45		dB	941Hz	w.r.t.
13			Low Tone	IR_{H770}	36	40		dB	770Hz	1336Hz
14		Dial Tone	Low Group	DR_{L440}		60		dB	440Hz	w.r.t
15				DR_{L350}		30		dB	350Hz	770Hz
16		Rejection	High Group	DR_{H440}		60		dB	440Hz	w.r.t.
17				DR_{H350}		50		dB	350Hz	1336Hz
18		FHT FLT Maximum Permissible Load		R_{LFT}	250			KΩ		
19				C_{LFT}			2000	pF		
20	L	Output Rise Time	FL, FH	t_{TLHO}		90	150	ns	10% to	
21	I M	Output Fall Time		t_{THLO}		60	100	ns	90% V_{DD}	
22		Crystal/Clock Freq.	OSC 1, OSC 2	f_c	3.5759	3.5795	3.5831	MHz		
23		Clock	Rise Time	t_{LHCI}			110	ns	10% to	Externally
24	C	Input	Fall Time	t_{HLCI}			110		90% V_{DD}	Applied
25	L O	(OSC 1)	Duty Cycle	DC_{CI}	40	50	60	%		Clock
26	C K	Clock Output OSC 2	Capacitive Load	C_{LOC}			30	pF	Unbalanced load, see Operating Notes	
27		Capacitance Any Input		C_i		5	7.5	pF		

NOTES
1. The sensitivity characteristic specifies correct operation of the post-comparator outputs at minimum input signal levels. It is valid for each of the four DTMF tones in each passband.

PIN FUNCTIONS

DIP Pin	Name	Description	
1	FL	Low group limiter output.	
2	FLT	Test output. Monitors low group filter output. Decouple to V_{SS} with 680pF capacitor.	
3	NC	Not connected.	
4	INPUT	Tone signal input (single ended).	
5	V_{REF}	Internal reference, can be used to bias input via 2MΩ resistor.	
6	PDWN	Power down active high. Internal pull down transistor. A high level signal powers down the device and inhibits the oscillator.	
7	NC	Not connected.	
8	V_{SS}	Negative (0V) power supply.	
9	NC	Not connected.	
10	FH	High group limiter output.	
11	FHT	Test output. Monitors high group filter output. Decouple to V_{SS} with 680pF capacitor.	
12	NC	Not connected.	
13	NC	Not connected.	
14	OSC 2	Clock Output.	3.58MHz crystal connected between these pins completes internal oscillator.
15	OSC 1	Clock Input.	
16	V_{DD}	Positive power supply.	

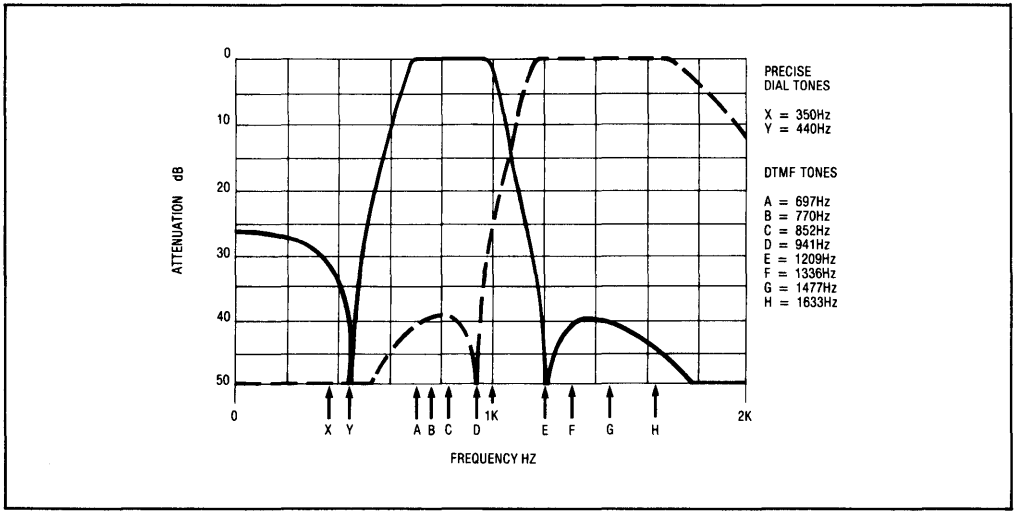

Fig.3 Typical filter characteristics

OPERATING NOTES

The MV8865 separates the high group and low group components of the dual tone signal and limits the resulting pair of sine waves, to produce square waves having the same frequencies as the individual input tones. These limited low group and high group tones appear at the FL and FH outputs respectively. To implement a complete DTMF receiver the FL and FH outputs are connected to the FL and FH inputs of one of Plessey Semiconductors' range of DTMF Digital Decoders (MV8860/62/63), see Fig.4.

Separation of the low group and high group tones is achieved by applying the dual tone signal simultaneously to the inputs of two sixth order switched capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low group and high group tones. The frequency characteristic of each filter (see Fig.3) also incorporates a notch at 440 Hz to provide dial tone rejection. Each filter output is followed by a single order switched capacitor section which operates as an interpolator smoothing the signals prior to limiting.

The limiting functions are performed by high gain comparators which are provided with hysteresis to prevent detection of unwanted low level signals and noise. The comparator outputs are buffered to drive the FL and FH output pins and detector device inputs. The MV8865 has a single ended input allowing connection either to a PCM decoder, radio receiver (Fig.4) or via a differential buffer to a telephone line (Fig.5). The signal input (Pin 4) should be biased at $V_{DD}/2$. With the input capacitively coupled, this is achieved by connecting the signal input to V_{REF} (Pin 5) via a 2 MΩ resistor.

FLT and FHT allow the filter outputs to be monitored prior to limiting, and should each be decoupled to V_{SS} by 680 pF capacitors.

Unbalanced Loads

Presenting a high unbalanced capacitive load to the oscillator crystal can cause attenuation of the oscillator output signal and increased supply current (see Fig.6). Where the MV8865 oscillator is required to drive a high capacitive load such as a number of other MV8865/8860s it is desirable to connect a capacitor between OSC1 and Vss, the value of this capacitor being equal to the capacitive loading at OSC2.

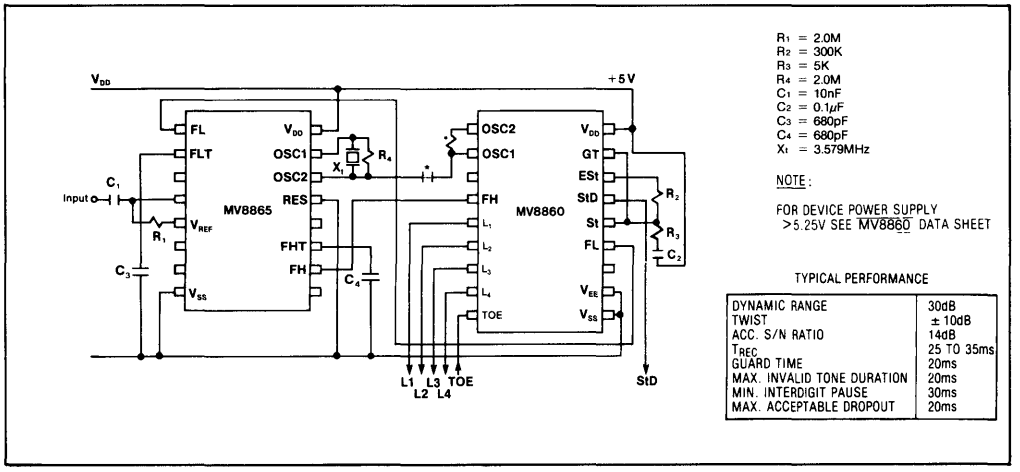

Fig.4 Single-ended input receiver using the MV8860 (5 V operation)

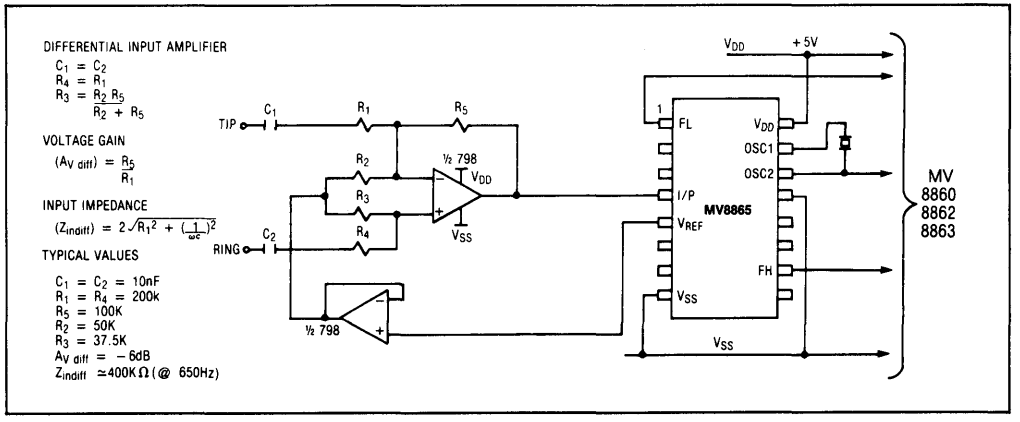

Fig.5 Connection to a telephone line

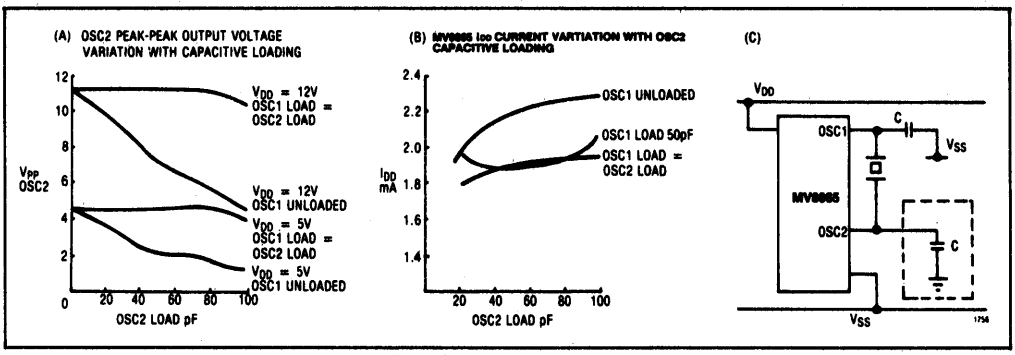

Fig.6 Crystal oscillator loading