PLESSEY
Semiconductors

PRELIMINARY INFORMATION

MV8870EXP

DTMF RECEIVER

The MV8870 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated on Plessey Semiconductors' double-poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high- and low- group filters and dial-tone rejection; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimised by on-chip provision of a differential input amplifier, clock oscillator and latched 3-state bus interface.

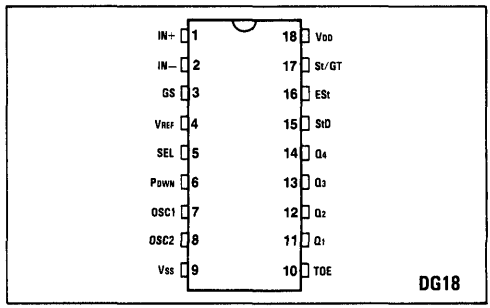


Fig.1 Pin connections (top view)

APPLICATIONS

- PABX
- Central Office
- Key Systems
- Mobile Radio
- Remote Control
- Remote Data Entry

FEATURES

- Full Receiver in Single 18-Pin Package
- Central Office Quality
- Lower Power Consumption
- Adjustable Acquisition and Release Times

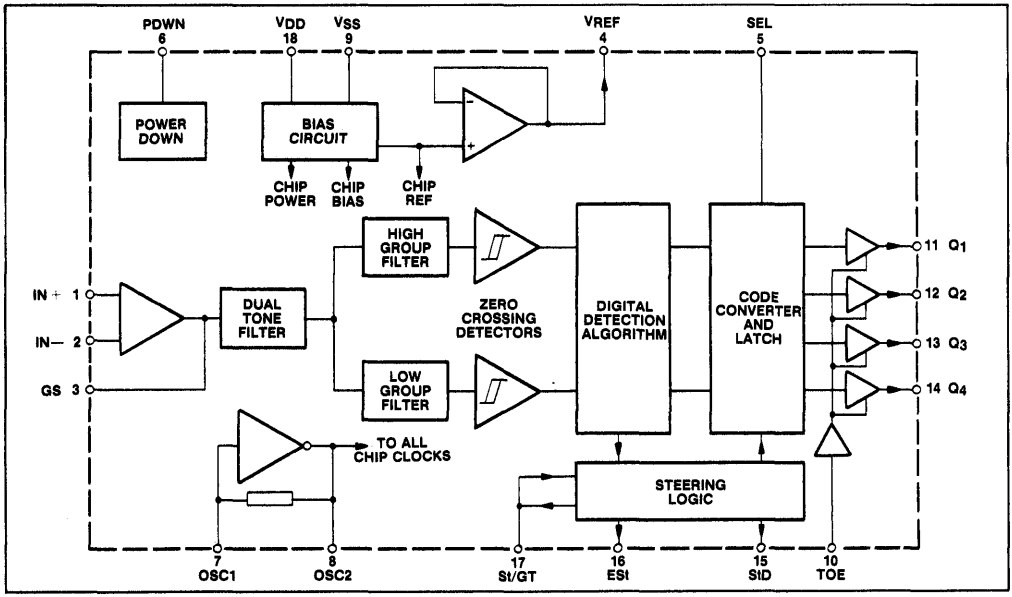


Fig.2 Functional block diagram

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Parameter	Min.	Max.	Unit
Power supply voltage V_{DD} - V_{SS}		6	V
Voltage on any pin	V_{SS} -0.3	V_{DD} +0.3	V
Current at any pin		10	mA
Operating temperature	-40	+85	°C
Storage temperature	-65	+150	°C
Package power dissipation (Note 2)		1000	mW

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Derate above 75°C at 16mW/°C. All leads soldered to board.

DC ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Operating supply voltage	V_{DD}	4.75		5.25	V	
Operating supply current	I_{DD}		3.0	7	mA	
Power consumption	P_O		15	35	mW	f = 3.579MHz
Low level input voltage	V_{IL}			1.5	V	
High level input voltage	V_{IH}	3.5			V	
Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
Pull up source current	I_{SO}		7.5	15.0	μA	TOE (Pin 10) = 0V
Input impedance (pins 1 & 2)	R_{IN}		10		MΩ	At 1kHz
Steering threshold voltage	V_{TSt}	2.2	2.35	2.5	V	
Low level output voltage	V_{OL}		0.03		V	No load
High level output voltage	V_{OH}		4.97		V	No load
Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT} = 0.4V
Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6V
Output voltage, pin 4	V_{REF}	2.4		2.7	V	No load
Output resistance, pin 4	R_{OR}		10		kΩ	

OPERATING CHARACTERISTICS, GAIN SETTING AMPLIFIER

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25° C

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input leakage current	I_{IN}		±100		nA	$V_{SS} < V_{IN} < V_{DD}$
Input resistance	R_{IN}		10		MΩ	
Input offset voltage	V_{OS}		±25		mV	
Power supply rejection	PSRR		60		dB	1kHz
Common mode rejection	CMRR		60		dB	V_{IN} = V_{REF} ±1.3V
DC open loop voltage gain	A_{VOL}		65		dB	
Open loop unity gain bandwidth	f_c		1.5		MHz	
Output voltage swing	V_O		4.5		V p-p	$R_L \geqslant$ 100kΩ to V_{SS}
Tolerable capacitive load (GS)	C_L		100		pF	
Tolerable resistive load (GS)	R_L		50		kΩ	
Common mode range	V_{cm}		3.0		V p-p	No load

AC CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD} = +5V, V_{SS} = 0V, T_{amb} = +25°C, f_{CLK} = 3.579545MHz, using test circuit of Fig.3.

Characteristic		Symbol	Value			Unit	Notes
			Min.	Typ.	Max.		
Valid input signal level (each tone of composite signal)	Min.				-29	dBm	1,2,3,5,6,9
					27.5	mVRMS	1,2,3,5,6,9
	Max.		+1			dBm	1,2,3,5,6,9
			883			mVRMS	
Twist accept limit	Positive			10		dB	2,3,6,9
	Negative			10		dB	2,3,5,9
Freq. deviation accept limit					±1.5% ±2Hz	Nom.	2,3,5,9
Freq. deviation reject limit			±3.5%			Nom.	2,3,5
Third tone tolerance				-16		dB	2,3,4,5,9,10
Noise tolerance				-12		dB	2,3,4,5,7,9,10
Dial tone tolerance				+18		dB	2,3,4,5,8,9,10
Tone present detection time		t_{DP}	5	11	14	ms	Refer to Fig.5
Tone absent detection time		t_{DA}	0.5	4	8.5	ms	
Tone duration accept		t_{REC}			40	ms	(User adjustable) Refer to 'Guard Time Adjustment'
Tone duration reject		t_{REC}	20			ms	
Interdigit pause accept		t_{ID}			40	ms	
Interdigit pause reject		t_{DO}	20			ms	
Propagation delay (St to Q)		t_{PQ}		8	11	µs	TOE = V_{DD}
Propagation delay (St to StD)		t_{PStD}		12		µs	
Output data set up (Q to StD)		t_{QStD}		3.4		µs	
Propagation delay (TOE to Q)	Enable	t_{PTE}		50	60	ns	R_L = 10kΩ
	Disable	t_{PTD}		300		ns	C_L = 50pF
Crystal/clock frequency		f_{CLK}	3.5759	3.5795	3.581	MHz	
Clock output (OSC2)	Capacitive load	C_{LO}			30	pF	

NOTES
1. dBm = decibels above or below a reference power of 1mW into a 600 ohm load.
2. Digit sequence consists of all 16 DTMF tones.
3. Tone duration = 40ms. Tone pause = 40ms.
4. Nominal DTMF frequencies are used.
5. Both tones in the composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5% ±2Hz.
7. Bandwidth limited (0 to 3kHz) Gaussian Noise.
8. The precise dial tone frequencies are 350Hz and 440Hz ±2%.
9. For an error rate of better than 1 in 10,000.
10. Reference to lowest level frequency component in DTMF signal.

INPUT CONFIGURATION

The input arrangement of the MV8870 provides a differential input operational amplifier as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail.

Provision is made for connection of a feedback register to the op-amp output (GS) for adjustment of gain.

In a single-ended configuration the input pins are connected as shown in Fig.3 with the op-amp connected for unity gain and V_{REF} biasing the input at 1/2 V_{DD}. Fig.4 shows the differential configuration, which permits the adjustment of gain with the feedback resistor Rs.

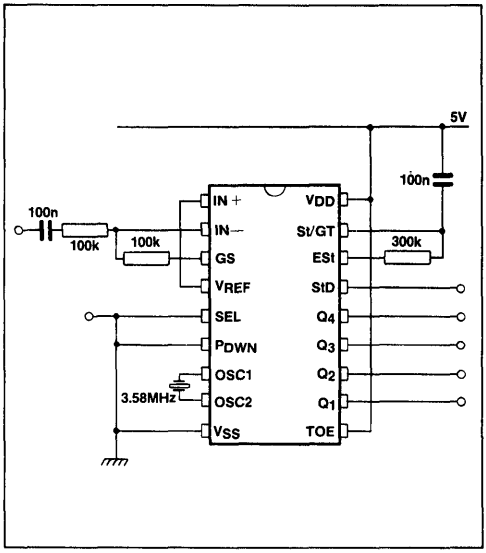


Fig.3 Single ended input configuration

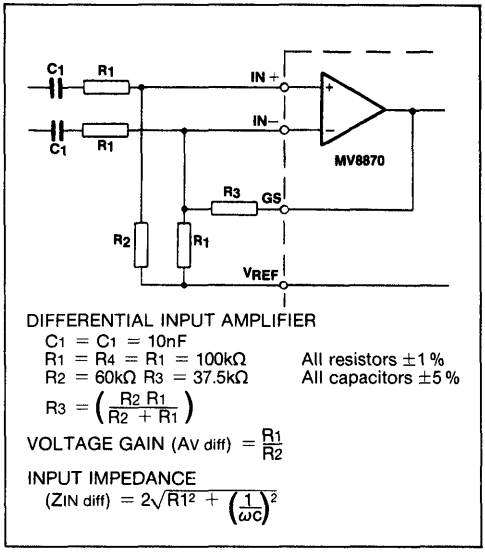
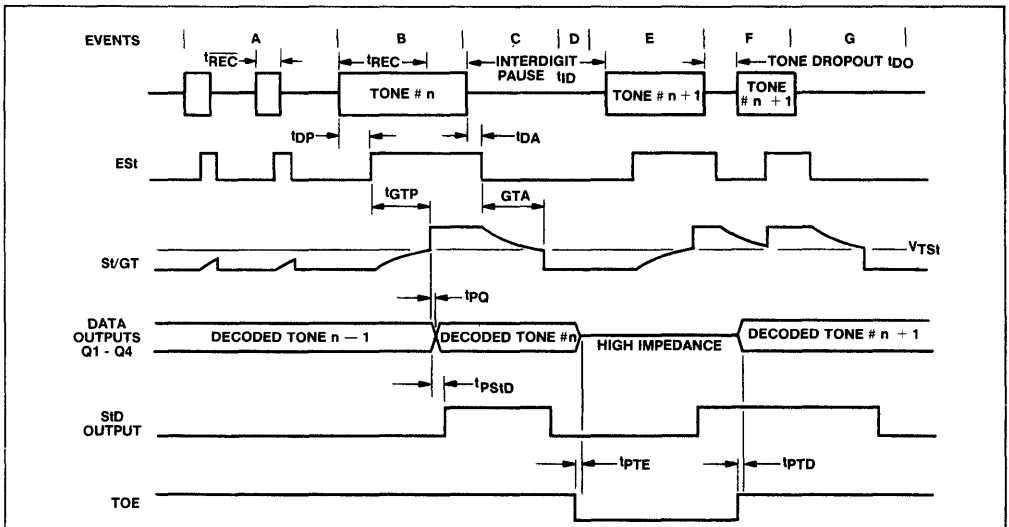


Fig.4 Differential input configuration



A. Short tone bursts detected; tone durations invalid. **B.** Tone #n detected; tone duration valid; decoded to outputs. **C.** End of tone #n detected and validated. **D.** 3-state outputs disabled (high impedance). **E.** Tone (#n + 1) detected; tone duration valid; decoded to outputs. **F.** 3-state outputs enabled; acceptable drop-out of tone (#n + 1) does not register at outputs. **G.** End of tone (#n + 1) detected and validated.

Fig.5 Timing diagram

PIN DESCRIPTIONS

Pin	Name	Description	
1	IN+	Non-inverting input	Connections to the front-end differential amplifier
2	IN−	Inverting input	
3	GS	Gain select. Gives access to output of front-end differential amplifier for connections of feedback resistor.	
4	V_{REF}	Reference voltage output, nominally $V_{DD/2}$. May be used to bias the inputs at mid-rail (see application diagram).	
5	SEL	Logic '1' or '0' selects one of two truth tables (see Table 1).	
6	P_{DWN}	Power down active high, internal pulldown resistor. A high level signal powers down and inhibits the oscillator.	
7	OSC1	Clock input	3.579545MHz crystal connected between these pins completes internal oscillator.
8	OSC2	Clock output	
9	V_{SS}	Negative power supply, normally connected to 0V.	
10	TOE	3-state output enable (input). Logic high enables the outputs Q1 - Q4. Internal pull-up.	
11	Q1	3-state data outputs. When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1).	
12	Q2		
13	Q3		
14	Q4		
15	StD	Delayed steering output presents a logic high when a received tone-pair has been registered and the output high latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.	
16	ESt	Early steering output. Presents a logic high immediately when the digital algorithm detects a recognisable tone-pair (signal conditions). Any momentary loss of signal condition will cause ESt to return to a logic low.	
17	St/GT	Steering input/guard time output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone-pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone-pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St (see Table 1).	
18	V_{DD}	Positive power supply.	

FUNCTIONAL DESCRIPTION

The MV8870 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low tones of a received pair, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high-group tones is achieved by applying the dual-tone signal to the inputs of two sixth-order switched-capacitor bandpass filters, the bandwidths of which correspond to the bands enclosing the low-group and high-group tones (see Fig.6).

The filter section also incorporates notches at 350Hz and 440Hz for exceptional dial-tone rejection. Each filter output is followed by a single-order switched capacitor section to smooth the signals prior to limiting.

Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals and noise; the outputs of the comparators provide full-rail logic swings at the frequencies of the incoming tones.

Decoder Section

The decoder uses digital counting techniques to determine the frequencies of the limited tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals, such as voice, while providing tolerance to small frequency deviations and variations. The averaging algorithm has been developed to ensure an optimum combination of immunity to 'talk-off' and tolerance to the presence of interfering signals ('third tones') and noise. When the detector recognises the simultaneous presence of two valid tones (referred to as 'signal condition' in some industry specifications), it raises the 'Early Steering' flag (ESt). Any subsequent loss of signal condition will cause ESt to fall.

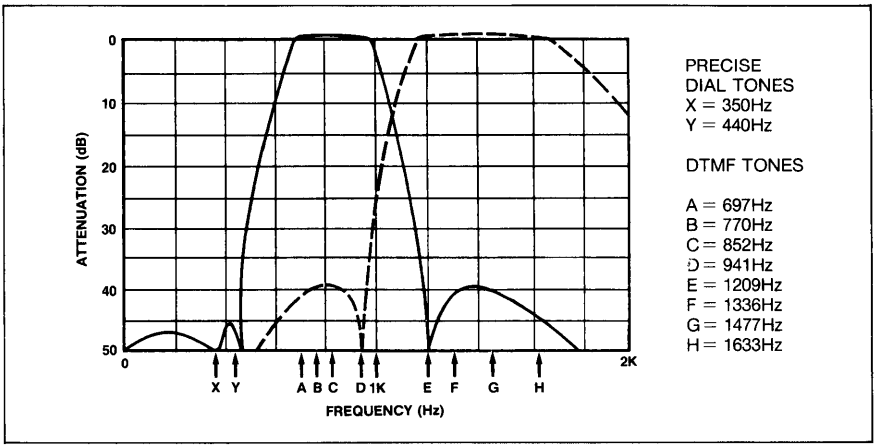


Fig.6 Typical filter characteristic

F_{LOW}	F_{HIGH}	KEY	TOE	SEL	Q_4	Q_3	Q_2	Q_1
697	1209	1	H	L	0	0	0	1
697	1336	2	H	L	0	0	1	0
697	1477	3	H	L	0	0	1	1
770	1209	4	H	L	0	1	0	0
770	1336	5	H	L	0	1	0	1
770	1477	6	H	L	0	1	1	0
852	1209	7	H	L	0	1	1	1
852	1336	8	H	L	1	0	0	0
852	1477	9	H	L	1	0	0	1
941	1336	0	H	L	1	0	1	0
941	1209	*	H	L	1	0	1	1
941	1477	#	H	L	1	1	0	0
697	1633	A	H	L	1	1	0	1
770	1633	B	H	L	1	1	1	0
852	1633	C	H	L	1	1	1	1
941	1633	D	H	L	0	0	0	0
697	1209	1	H	H	0	0	0	1
697	1336	2	H	H	0	0	1	0
697	1477	3	H	H	0	0	1	1
770	1209	4	H	H	0	1	0	0
770	1336	5	H	H	0	1	0	1
770	1477	6	H	H	0	1	1	0
852	1209	7	H	H	0	1	1	1
852	1336	8	H	H	1	0	0	0
852	1477	9	H	H	1	0	0	1
941	1336	0	H	H	0	0	0	0
941	1209	*	H	H	1	0	1	0
941	1477	#	H	H	1	0	1	1
697	1633	A	H	H	1	1	0	0
770	1633	B	H	H	1	1	0	1
852	1633	C	H	H	1	1	1	0
941	1633	D	H	H	1	1	1	1
		ANY	L	ANY	Z	Z	Z	Z

L = Logic low, H = Logic high, Z = High impedance

Table 1 Functional decode table

STEERING CIRCUIT

Before registration of a decoded tone-pair, the receiver checks for a valid signal duration (referred to as 'character recognition condition'). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes V_C (see Fig.7) to rise as the capacitor discharges. Provided signal-condition is maintained (ESt remains high) for the validation period (t_{GTP}), V_C reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point, the GT output is activated and drives V_C to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the 'delayed steering' output flag, StD, goes high, signalling that a received tone pair has been registed. The contents of the output latch are made available on the 4-bit output bus by raising the 3-state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions ('drop-out') too short to be considered a valid pulse. The facility, together with the capability of selecting the steering time-constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

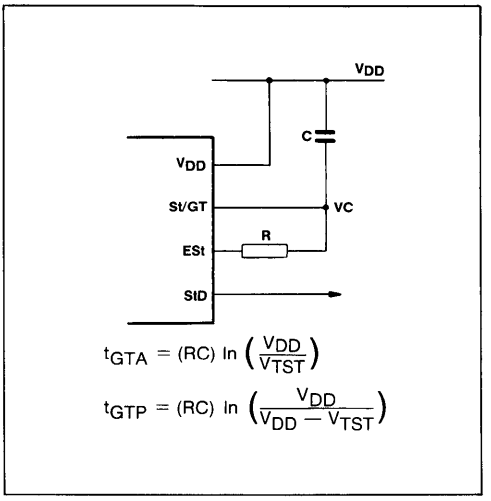


Fig.7 Basic steering circuit

Guard Time Adjustments

In many situations not requiring independent selection of receive and pause, the simple steering circuit of Fig.7 is applicable. Component values are chosen according to the following formulae:

$$t_{REC} = t_{DP} + t_{GTP}$$

$$t_{ID} = T_{DA} + t_{GTA}$$

The value of t_{DP} is a parameter of the device (see AC Characteristics) and t_{REC} is the minimum signal duration to be recognised by the receiver. A value for C of 0.1μF is recommended for most applications, leaving R to be selected by the designer. For example, a suitable value of R for a t_{REC} of 40ms would be 300kΩ.

Different steering arrangements may be used to select independently the guard times for tone-present (t_{GTP}) and tone-absent (t_{GTA}). This may be necessary to meet system specification which place both accept and reject limits on both tone duration and interdigital pause.

Guard time adjustment also allows the designer to tailor system parameters such as talk-off and noise immunity. Increasing t_{REC} improves talk-off performance, since it reduces the probability that tones simulated by speech will maintain signal condition for long enough to be registered. On the other hand, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to drop-outs would be requirements. Design information for guard time adjustment is shown in Fig.8.

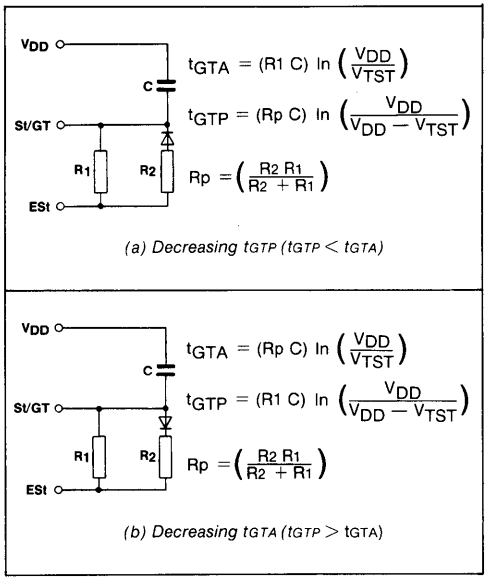


Fig.8 Guard time adjustment