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MV95308
30MHz 8-BIT CMOS VIDEO DAC

The MV95308 is a CMOS 8-bit, 30MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifier and reference voltage source on chip.

The device contains a data input register and registered video controls ($\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{SYNC}}$). These control inputs and associated internal circuitry allows the MV95308 to be used in video graphics systems by providing the necessary video pedestal levels. The $\overline{\text{STRDAC}}$ input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate R_{SET} external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

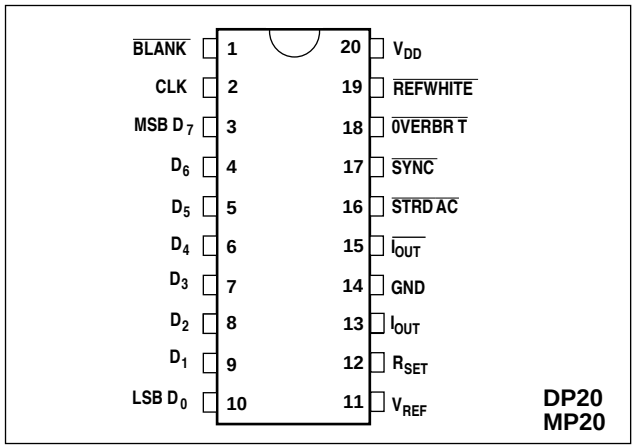

Fig.1 Pin connections - top view

FEATURES

- Low Power Consumption (180mW Typ)
- 30MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Consumer TV
- Instrumentation

ORDERING INFORMATION

MV95308 ADG (Military - Ceramic DIL Package)
MV95308 CDP (Commercial - Plastic DIL Package)
MV95308 CMP (Commercial - Miniature Plastic DIL Package)

ABSOLUTE MAXIMUM RATINGS (Reference to GND)

DC Supply Voltage, V_{DD}		-0.3 to +7V
Digital Input Voltage		-0.3 to V_{DD} +0.3V
Analog Output Short Circuit Duration		Indefinite
Ambient Operating Temperature	A grade	-55°C to +125°C
	C grade	0°C to + 70°C
Storage Temperature Range		-55°C to +125°C

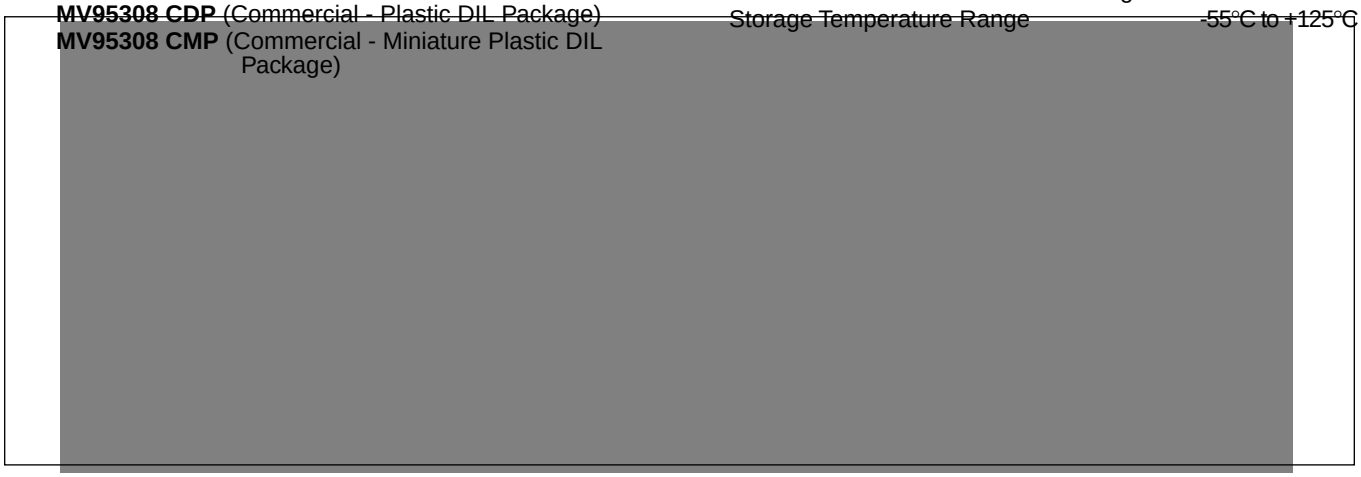

Fig.2 Block diagram of MV95308

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):
As specified in recommended operating conditions. Full temperature range: A grade = -55°C to +125°C, C grade = 0 to 70°C

DC CHARACTERISTICS

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Resolution		Full	8			Bits	
Integral linearity error	INL	25		±0.5		LSB	
		Full			±1	LSB	
Differential linearity error	DNL	25		±0.5		LSB	
		Full			±1	LSB	
Gain error		25		±1%	±5%	%	Of full scale
Analog output							
Grey scale current range		25		8.8		mA	75Ω singly terminated load R_{SET} = 1.8kΩ (graphics mode)
				255		LSB	
10% Over Bright level relative to White level		25	26	27 10	28	LSB IRE	
White level relative to Blank level		25	275	276	277	LSB	
				100		IRE	
Black level relative to Blank level		25	20	21	22	LSB	
				7.5		IRE	
White level relative to Black level		25		255 92.5		LSB IRE	
Blank level		25	107	111 40	115	LSB IRE	
Sync level		25		0		LSB	
LSB size	LSB	25		2.58		mV	
Output compliance	V_{OC}	25	-0.3		+1.5	V	
Digital inputs							
High level I/P voltage	V_{IH}	25	3		V_{DD}+0.3	V	
Low level I/P voltage	V_{IL}	25	GND-0.3		1.2	V	
High level I/P current	I_{IH}	25			+1	µA	
Low level I/P current	I_{IL}	25			-1	µA	
Internal voltage reference (V_{REF})	V_{REF}	25	0.95	1.0	1.05	V	
		Full	0.90		1.10	V	
V_{REF} temperature coefficient				40		ppm/°C	

AC CHARACTERISTICS (Refer to Fig. 3)

Parameter	Symbol	Temp (°C)	Value Min.	Value Typ.	Value Max.	Units	Conditions
Max clock rate	f_{MAX}	Full	30			MHz	maximum guaranteed freq.
Clock high time	t_{CLKH}	25	10			ns	
Clock low time	t_{CLKL}	25	10			ns	
Data and control setup time	t_{SU}	25	8			ns	
Data and control hold time	t_H	25	2			ns	
Analog output delay	t_{DLY}	25		10		ns	
Analog output rise/fall time	t_{RF}	25		3	6	ns	
Analog output settling time	t_S	25		15		ns	
Glitch energy		25		100		pV-sec	
V_{DD} supply current	IDD	25		30		mA	fc = 15MHz
				36		mA	fc = 30MHz

THERMAL CHARACTERISTICS

Thermal Resistance	DP	MP	
Chip to case θ_{jC}	20	30	°C/W
Chip to ambient θ_{jA}	75	93	°C/W

RECOMMENDED OPERATING CONDITIONS

R_{LOAD} (I_{OUT} and $I_{\overline{OUT}}$)	75Ω
V_{DD}	5.0V ± 0.5V
R_{SET} (graphics applications)	1.8kΩ
R_{SET} (straight DAC applications)	1.2kΩ

CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95308 contains an 8-bit D-to-A converter, input registers, a loop amplifier and a voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8-bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{SYNC}$ and $\overline{BLANK}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$, $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95308 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95308 eliminates the need for precision component ratios by using segmented architecture in which equal weight bit currents are either routed to I_{OUT} or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95308 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor R_{SET}. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

Fig.3 Timing diagram

Description	$\overline{STRDAC}$	$\overline{SYNC}$	$\overline{BLANK}$	$\overline{REFWHITE}$	$\overline{OVERBRT}$	OUTPUT DATA	I_{OUT} (LSB)
REFWHITE + 10%	1	1	1	0	0	X	414
REFWHITE	1	1	1	0	1	X	387
FULL WHITE	1	1	1	1	1	$FF	387
OVERBRIGHT	1	1	1	1	0	DATA	DATA + 132 + 27
FULL BLACK	1	1	1	1	1	$00	132
BLANK	1	1	0	X	X	X	111
DATA-SYNC	1	0	1	1	1	DATA	DATA + 21
SYNC	1	0	0	X	X	X	0
STRDAC MODE	0	X	1	1	X	DATA	DATA

Table 1: Video output truth table

Pin	Name	Description
2	CLK	**The clock input.** The falling edge of the clock latches the $\overline{DATA}$, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{OVERBRT}$ and $\overline{REFWHITE}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output.
3-10	D_7-D_0	**The data inputs.** D_0 is the least significant bit (LSB). The coding is in straight binary only.
13,15	I_{OUT}, $I_{\overline{OUT}}$	**The current output and its complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V.
14	GND	**Analog ground for the DAC.**
20	V_{DD}	**Analog power for the DAC**
11	V_{REF}	**The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor.
12	R_{SET}	**The full scale adjust control.** The R_{SET} resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the R_{SET} resistor so that the voltage across the resistor is equal to the V_{REF} voltage. This reference current has a weighting equal to 16 LSB's.
1	$\overline{BLANK}$	**The composite blank control input.** A logical zero on this input removes the Black pedestal from the I_{OUT} output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high.
17	$\overline{SYNC}$	**The composite sync control input.** A logical zero on this input removes the Blank pedestal from the I_{OUT} output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{SYNC}$ input does not override any other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high.
19	$\overline{REFWHITE}$	**The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{BLANK}$ input will override this input. If left open circuit this input is internally tied high.
18	$\overline{OVERBRT}$	**The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the I_{OUT} output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{BLANK}$ input overrides this input. If left open circuit this input is internally tied high.
16	$\overline{STRDAC}$	**The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both I_{OUT} and $I_{\overline{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the R_{SET} resistor value, see application notes. The $\overline{BLANK}$ the $\overline{REFWHITE}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{STRDAC}$ pin held low the output current can be calculated from: Output current = Data x 1 LSB Where 1 LSB= $\frac{V_{REF}}{16 \times R_{SET}}$ Full scale = 255 LSB V_{REF} = 1.0V typ. The exact value of 1 LSB must be calculated from the full scale output. If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from: Output current = (DATA + 21 + 111) x 1 LSB V_{REF} = 1.0V typ.

APPLICATIONS INFORMATION

RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig.4) it is recommended that a singly terminated 75Ω load be used with an R_{SET} resistor value of approximately 1.82kΩ

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used but in association with an R_{SET} value of approximately 1.29kΩ to provide the increased voltage range.

Non-Video Applications

The MV95308 may be used in non-video applications as explained in the pin description for $\overline{STRDAC}$ mode.The relationship between R_{SET} and the full scale output current has been explained previously and for a singly terminated 75Ω load an R_{SET} resistor value of approximately 1.19kΩ should be used.

PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95308 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pick-up, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.

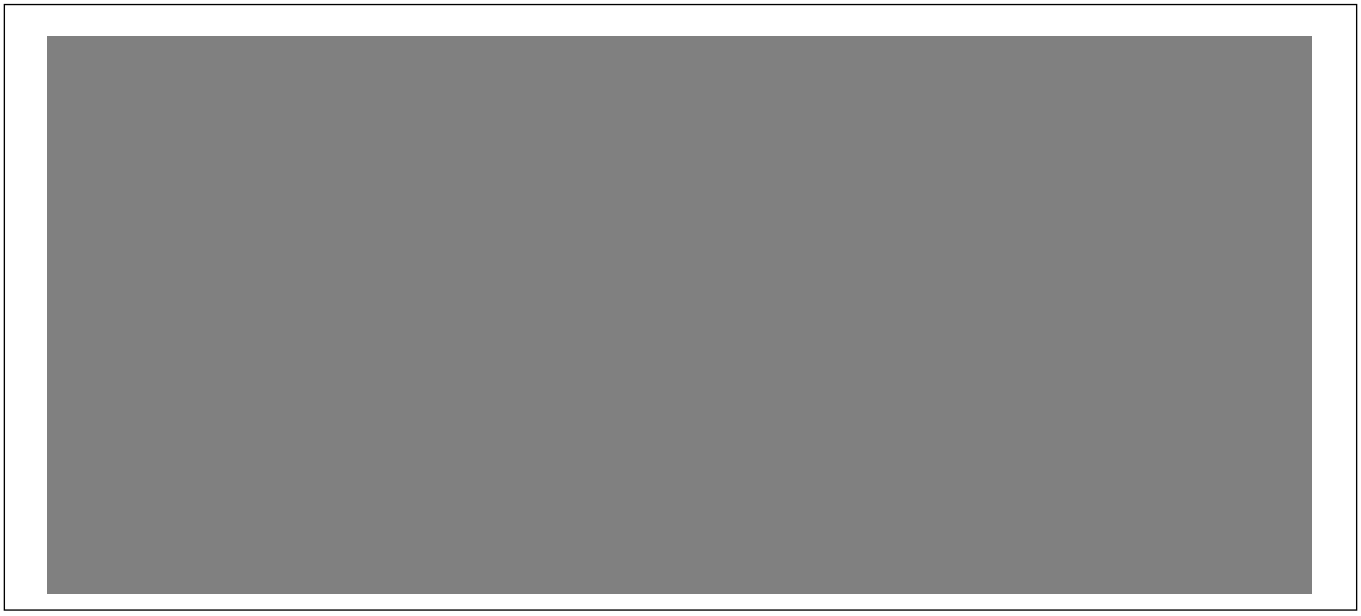

Fig.4 Composite video output waveform

Fig.5 Applications/test board

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