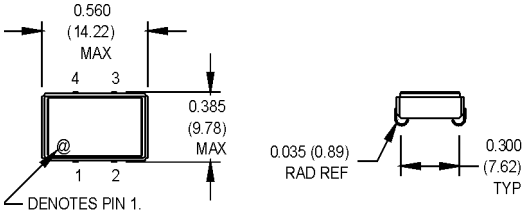
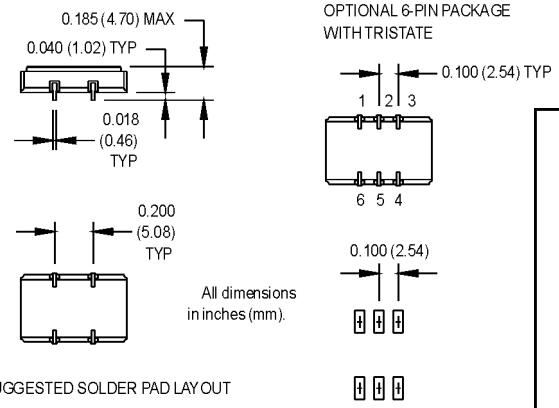
MVS Series

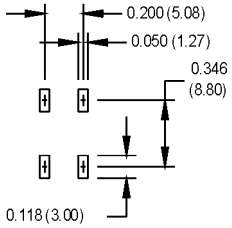
9x14 mm, 5.0 Volt, HCMOS/TTL, VCXO

- General purpose VCXO for Phase Lock Loops (PLL), Clock Recovery, Reference Signal Tracking and Synthesizers
- Frequencies up to 160 MHz and tri-state option





SUGGESTED SOLDER PAD LAYOUT



Pin Connections

FUNCTION	4 Pin Pkg.	6 Pin Pkg.
Control Voltage	1	1
Tristate		2
Circuit/Case Ground	2	3
Output	3	4
N/C		5
+Vdd	4	6

Ordering Information

MVS 1 3 V 2 C J -R 00.0000 MHz

Product Series

Temperature Range
- 1: 0°C to +70°C
- 2: -40°C to +85°C
- 6: -20°C to +70°C

Stability
- 1: ±1000 ppm
- 2: ±500 ppm
- 3: ±100 ppm
- 4: ±50 ppm
- 5: ±35 ppm
- 6: ±25 ppm
- *8: ±20 ppm

Output Type
- V: Voltage Controlled
- T: Tristate

Pull Range (Vc = .5 to 4.5 V)
- 1: ±50 ppm min.
- 2: ±100 ppm min. (Up to 70.000 MHz)

Symmetry/Logic Compatibility
- A: 40/60 CMOS/TTL
- C: 45/55 HCMOS

Package/Lead Configurations
- J: J Lead

RoHS Compliance
- Blank: non-RoHS compliant part
- -R: RoHS compliant part

Frequency (customer specified)

*Contact factory for availability.

Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
	Frequency Range	F	1.544		160	MHz	See Note 1
	Operating Temperature	TA	(See Ordering Information)				
	Storage Temperature	Ts	-55		+125	°C	
	Frequency Stability	ΔF/F	(See Ordering Information)				
	Aging						
	1st Year		-3/-5		+3/+5	ppm	< 52 MHz / ≥ 52 MHz
	Thereafter (per year)		-1/-2		+1/+2	ppm	< 52 MHz / ≥ 52 MHz
	Pullability/APR		(See Ordering Information)				Over control voltage
	Control Voltage	Vc	0.5	2.5	4.5	V	
	Linearity				10	%	Positive Monotonic Slope
	Modulation Bandwidth	fm	10			kHz	
	Input Impedance	Zin	50k			Ohms	
	Input Voltage	Vdd	4.75	5.0	5.25	V	
	Input Current	Idd		25	35	mA	1.544 to 24.999 MHz
				35	60	mA	25 to 69.999 MHz
				55	90	mA	70 to 160 MHz
	Output Type						HCMOS/TTL
	Load						See Note 2
	1.544 to 60 Mhz		10 TTL or 50 pF				
	60.001 to 160 MHz		5 TTL or 30 pF				
	Symmetry (Duty Cycle)		(See Ordering Information)				See Note 3
	Logic "1" Level	Voh	90% Vdd			V	HCMOS load
			Vdd -0.5			V	TTL Load
	Logic "0" Level	Vol			10% Vdd	V	HCMOS load
					0.5	V	TTL load
	Rise/Fall Time	Tr/Tf		3	10	ns	See Note 4
	Tristate Function		Input Logic "1" or floating: output active Input Logic "0": output disables to high-Z				
	Start up Time			4		ms	
	Phase Jitter @ 155.52 MHz	ϕ J		10	15	ps RMS	Integrated 12 kHz - 20 MHz
	Phase Noise (Typical)	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	Offset from carrier
	@ 155.52 MHz	-62	-93	-113	-115	-114	dBc/Hz

1. Frequencies above 90 MHz utilize a PLL design. Fundamental and PLL designs are available at other frequencies. Contact factory.
2. TTL load - see load circuit diagram #1. HCMOS load - see load circuit diagram #2.
3. Symmetry is measured at 1.4 V with TTL load, and at 50% Vdd with HCMOS load.
4. Rise/Fall times are measured between 0.5 V and 2.4 V with TTL load, and between 10% Vdd and 90% Vdd with HCMOS load.