

The RF Line

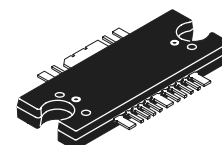
RF LDMOS Wideband Integrated Power Amplifiers

The MW4IC915MB/GMB wideband integrated circuit is designed for GSM and GSM EDGE base station applications. It uses Motorola's newest High Voltage (26 to 28 Volts) LDMOS IC technology and integrates a multi-stage structure. Its wideband On Chip design makes it usable from 750 to 1000 MHz. The linearity performances cover all modulations for cellular applications: GSM, GSM EDGE, TDMA, N-CDMA and W-CDMA.

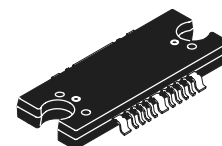
- Typical GSM/GSM EDGE Performances: 26 Volts, $I_{DQ1} = 60$ mA, $I_{DQ2} = 240$ mA, 869-894 MHz and 921-960 MHz
 Output Power — 3 Watts Avg.
 Power Gain — 31 dB
 Efficiency — 19%
 Spectral Regrowth @ 400 kHz Offset = -65 dBc
 Spectral Regrowth @ 600 kHz Offset = -83 dBc
 EVM — 1.5%
- Typical Performance: 860-960 MHz, 26 Volts
 Output Power — 15 Watts CW
 Power Gain — 30 dB
 Efficiency — 44%
- On Chip Matching (50 Ohm Input, >3 Ohm Output)
- Integrated Temperature Compensation Capability with Enable/Disable Function
- Integrated ESD Protection
- Capable of Handling 5:1 VSWR, @ 26 Vdc, $f = 921$ MHz,
 $P_{out} = 15$ W CW, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA
- Can Be Bolted or Soldered through a Hole in the Circuit Board for Maximum Thermal Performance
- Also Available in Gull Wing for Surface Mount
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MW4IC915MBR1 MW4IC915GMBR1

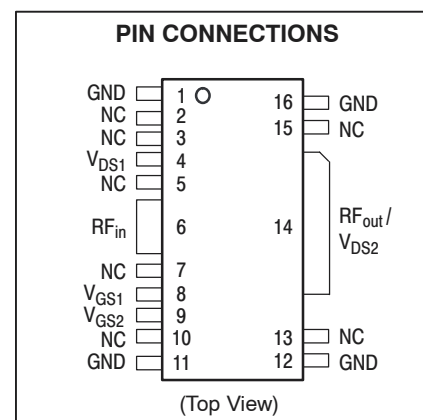
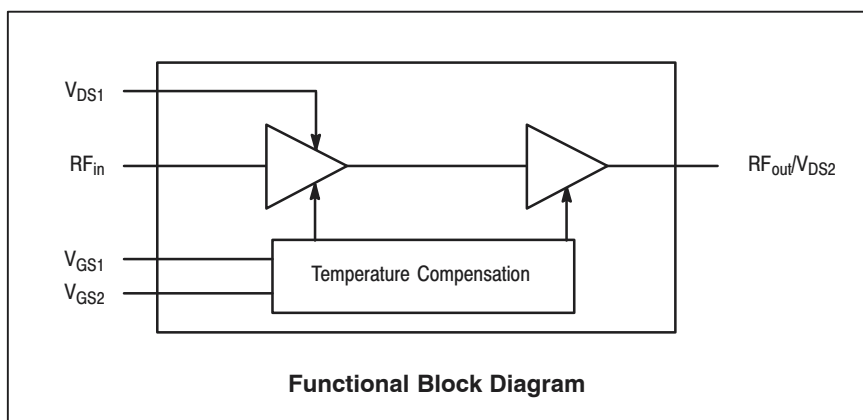
**GSM/GSM EDGE,
N-CDMA, W-CDMA
860 - 960 MHz, 15 W, 26 V
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS**



**CASE 1329-09
TO-272 WB-16
PLASTIC
MW4IC915MBR1**



**CASE 1329A-03
TO-272 WB-16 GULL
PLASTIC
MW4IC915GMBR1**



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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	65	Vdc
Gate-Source Voltage	V_{GS}	-0.5. +15	Vdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Operating Junction Temperature	T_J	175	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
GSM Application ($P_{out} = 15$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.48	
GSM EDGE Application ($P_{out} = 7.5$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.59	
CDMA Application ($P_{out} = 3.75$ W CW)	Stage 1, 26 Vdc, $I_{DQ} = 60$ mA Stage 2, 26 Vdc, $I_{DQ} = 240$ mA	1.63	

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M3 (Minimum)
Charge Device Model	C2 (Minimum)

MOISTURE SENSITIVITY LEVEL

Test Methodology	Rating
Per JESD 22-A113	3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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TWO-TONE FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)

Two-Tone Common-Source Amplifier Power Gain ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	G_{ps}	29	31	—	dB
Drain Efficiency ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	η	29	31	—	%
Third Order Intermodulation Distortion ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	IMD3	—	-40	-29	dBc
Input Return Loss ($V_{DS} = 26$ Vdc, $P_{out} = 15$ W PEP, $I_{DQ1} = 90$ mA, $I_{DQ2} = 240$ mA, $f_1 = 869$ MHz, $f_2 = 869.1$ MHz and $f_1 = 960$ MHz and $f_2 = 960.1$ MHz)	IRL	—	-15	-10	dB

(continued)

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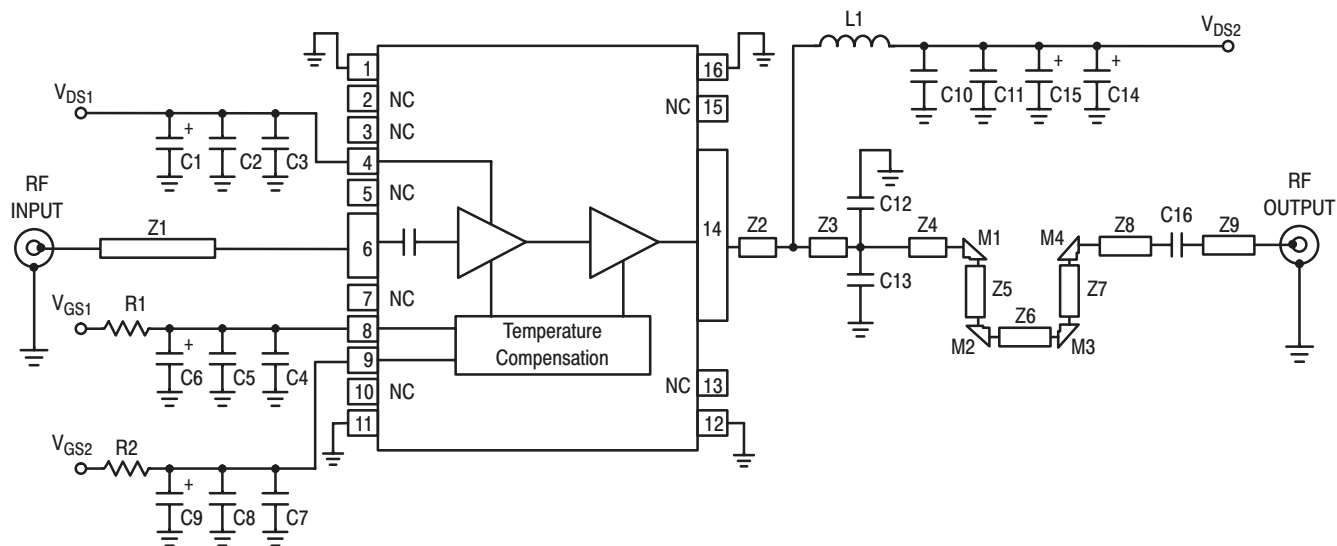
ELECTRICAL CHARACTERISTICS - continued (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
PERFORMANCE TESTS (In Motorola Reference Board) V _{DS} = 26 V, I _{DQ1} = 60 mA, I _{DQ2} = 240 mA					
Quiescent Current Accuracy over Temperature (-10 to 85°C) at Nominal Value	ΔI _{QT}	—	±5	—	%
Gain Flatness in 40 MHz Bandwidth @ P _{out} = 3 W CW (Characterize from 869-894 MHz and 920-960 MHz)	G _F	—	0.2	—	dB
Deviation from Linear Phase in 40 MHz Bandwidth @ P _{out} = 3 W CW (Characterize from 869-894 MHz and 920-960 MHz)	Φ	—	±0.6	—	°
Delay @ P _{out} = 3 W CW	Delay	—	2.5	—	ns
Insertion Phase Window @ P _{out} = 3 W CW	ΦΔ	—	±15	—	°

TYPICAL PERFORMANCE GSM/GSM EDGE (In Motorola Reference Board) V_{DS} = 26 V, I_{DQ1} = 60 mA, I_{DQ2} = 240 mA, 869-894 MHz and 921-960 MHz

Output Power at 1dB Compression Point	P1dB	—	20	—	Watts
Common-Source Amplifier Power Gain (P _{out} = 15 W CW)	G _{ps}	—	30	—	dB
Drain Efficiency (P _{out} = 15 W CW)	η	—	44	—	%
Input Return Loss (P _{out} = 15 W CW)	IRL	—	-15	—	dB
Error Vector Magnitude (P _{out} = 3 W Avg. including 0.6% rms source EVM)	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset (P _{out} = 3 W Avg.)	SR1	—	-65	—	dBc
Spectral Regrowth at 600 kHz Offset (P _{out} = 3 W Avg.)	SR2	—	-83	—	dBc

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Z1	0.086" , 50 Ω Microstrip	Z6	0.157" x 0.283" Microstrip
Z2	0.133" x 0.236" Microstrip	Z7	0.429" x 0.283" Microstrip
Z3	0.435" x 0.283" Microstrip	Z8	0.394" x 0.088" Microstrip
Z4	0.171" x 0.283" Microstrip	Z9	0.181" x 0.088" Microstrip
Z5	0.429" x 0.283" Microstrip	PCB	Taconic TLX8, 0.030", $\epsilon_r = 2.55$

Figure 1. Two-Tone 860-960 MHz Test Fixture Schematic

Table 1. Two-Tone 860-960 MHz Test Fixture Component Designations and Values

Designators	Description
C1, C6, C9, C14	22 μ F, 35 V Tantalum Chip Capacitors, AVX #TAJE226M035R
C2, C5, C8, C11	1000 pF Chip Capacitors, B Case, ATC #100B102JCA500X
C3, C4, C7, C10, C16	22 pF Chip Capacitors, B Case, ATC #100B220JCA500X
C12, C13	10 pF Chip Capacitors, B Case, ATC #100B100JCA500X
C15	10 μ F Tantalum Chip Capacitor, Kemet #T491X226K035AS4394
R1, R2	10 k Ω , 1/4 W Chip Resistor (1206)
L1	12.5 nH Inductor
M1, M2, M3, M4	0.283", 90° Mitered Microstrip Bends

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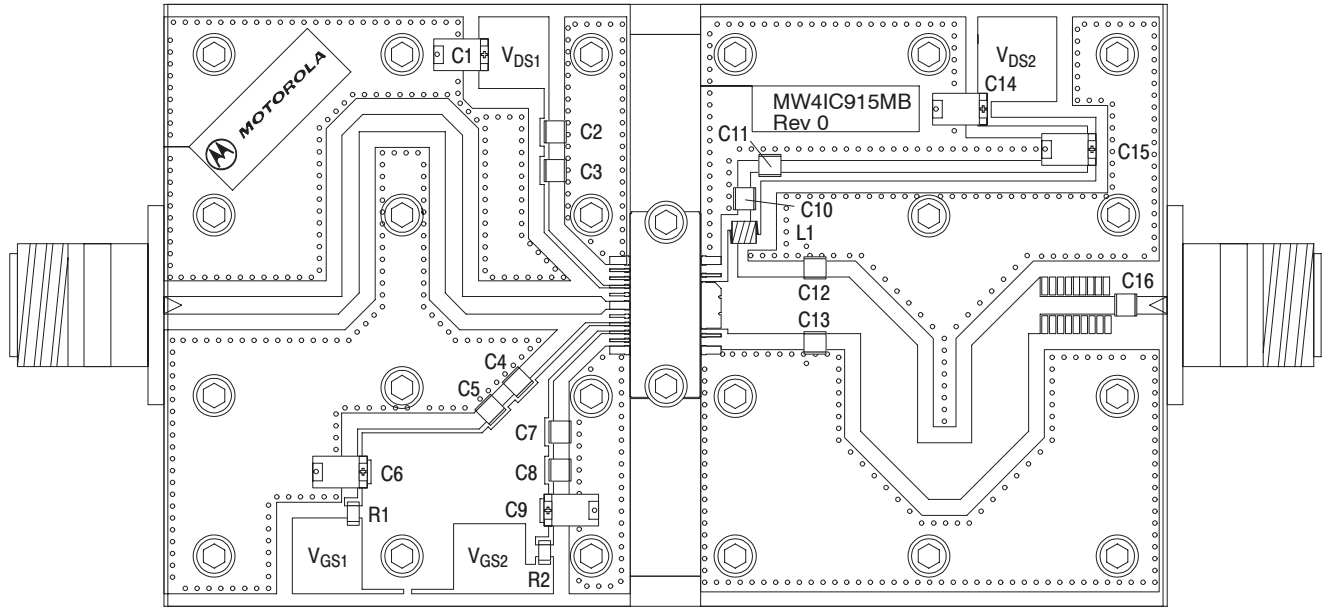
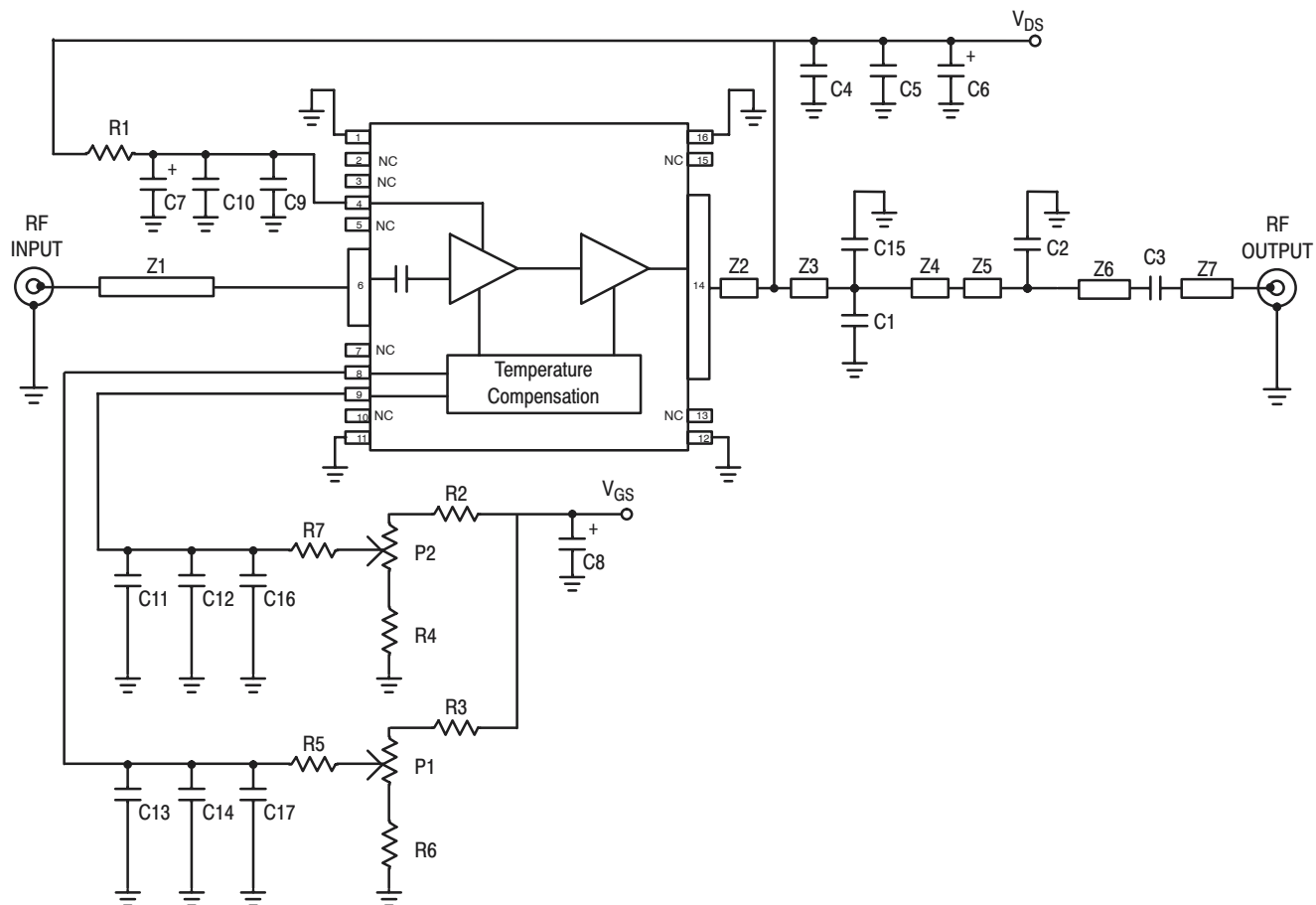


Figure 2. Two-Tone 860-960 MHz Test Fixture Component Layout

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Z1	0.681" x 0.039", 50 Ω Microstrip	Z5	0.566" x 0.043" Microstrip
Z2	0.157" x 0.228" Microstrip	Z6	0.165" x 0.043" Microstrip
Z3	0.468" x 0.157" Microstrip	Z7	0.078" x 0.043" Microstrip
Z4	0.220" x 0.157" Microstrip	PCB	Taconic RF35, 0.02", $\epsilon_r = 3.5$

Figure 3. 860-960 MHz Reference Board Schematic

Table 2. 860-960 MHz Reference Board Component Designations and Values

Designators	Description
C1, C15	10 pF Chip Capacitors (0805), ACCU-P AVX #08051J100GBT
C2	5.6 pF Chip Capacitor (0805), ACCU-P AVX #08051J5R6BBT
C3, C4, C9, C11, C13	33 pF Chip Capacitors (0805), ACCU-P AVX #08051J330GB
C5, C10, C12, C14	10 nF Chip Capacitors (0805), AVX #08055C103KAT
C6, C7, C8	22 μ F, 35 V Tantalum Capacitors, AVX #TAJE226M035R
C16, C17	100 nF Chip Capacitors (0805), AVX #08055C104KAT
P1, P2	5 k Ω Potentiometer CMS Cermet Multi-turn, Bourns #3224W
R1, R2, R3, R4, R5	0 Ω , 1/8 W Chip Resistors (0805)
R6, R7	10 k Ω , 1/4 W Chip Resistors (1206)

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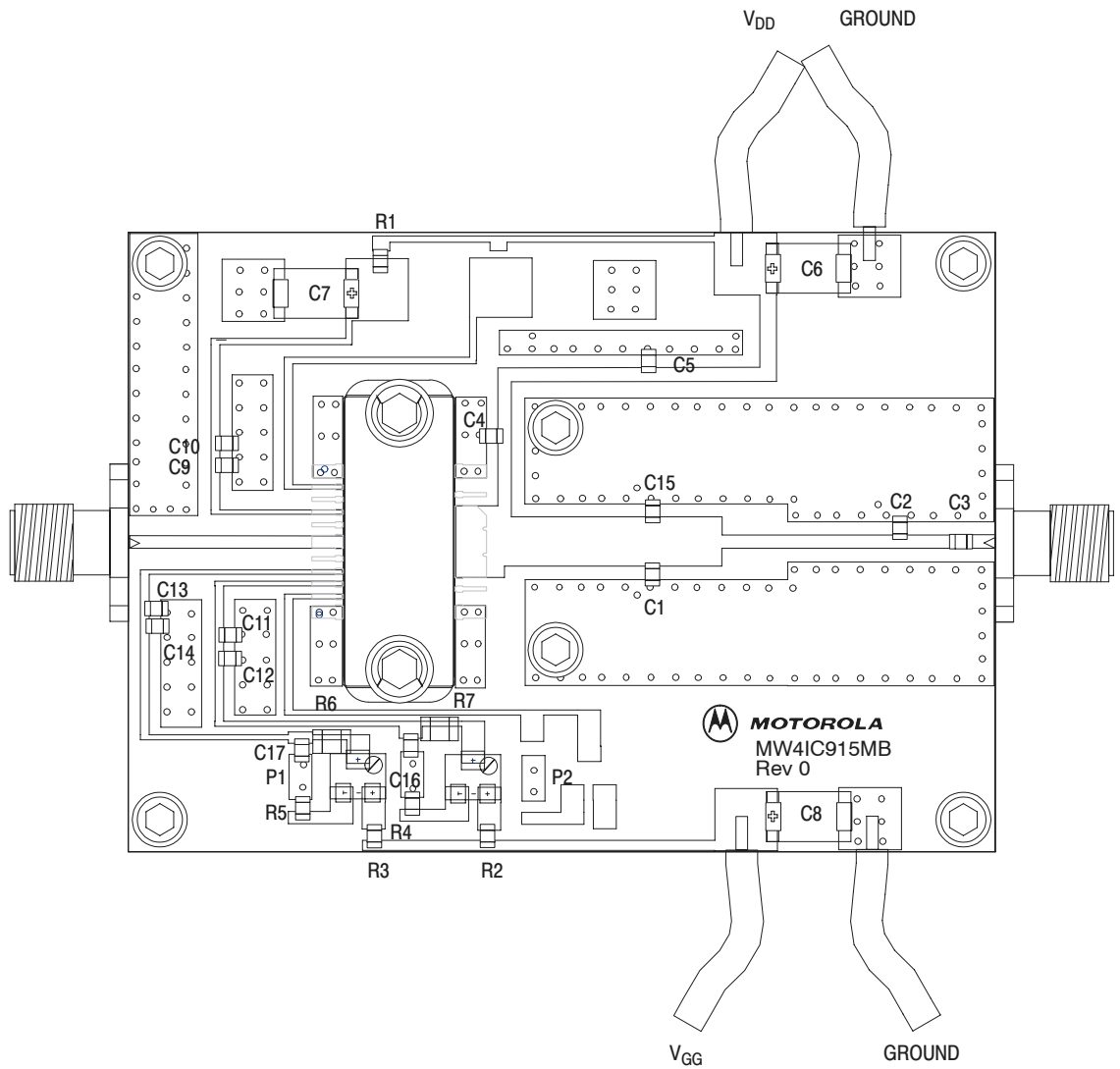


Figure 4. 860-960 MHz Reference Board Component Layout

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TYPICAL CHARACTERISTICS (MOTOROLA TEST FIXTURE, 50 OHM SYSTEM)

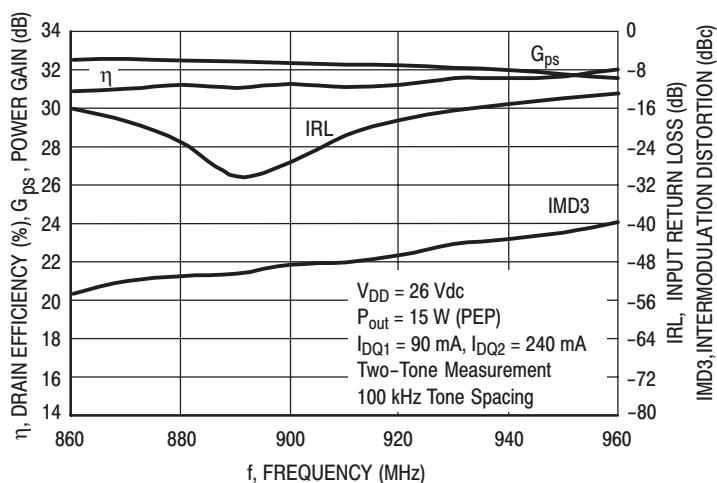


Figure 5. Two-Tone Wideband Circuit Performance

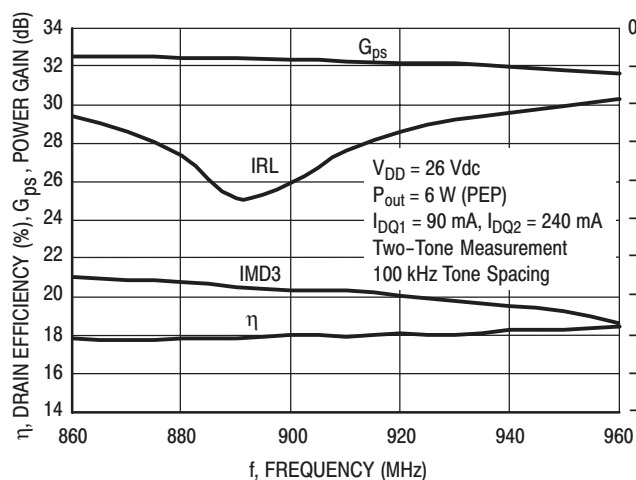


Figure 6. Two-Tone Wideband Circuit Performance

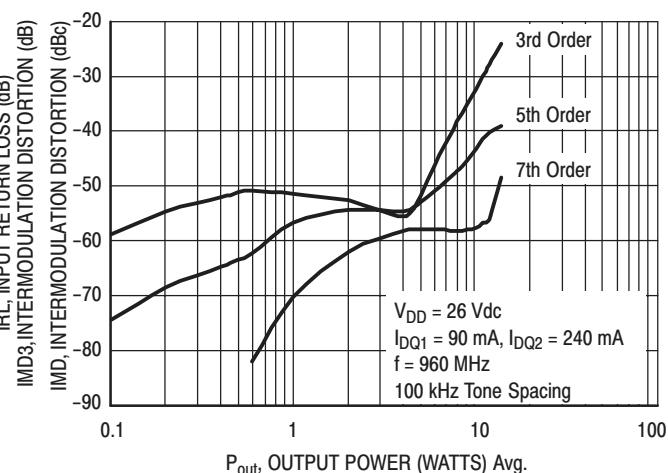


Figure 7. Intermodulation Distortion Products versus Output Power

TYPICAL CHARACTERISTICS (MOTOROLA REFERENCE BOARD)

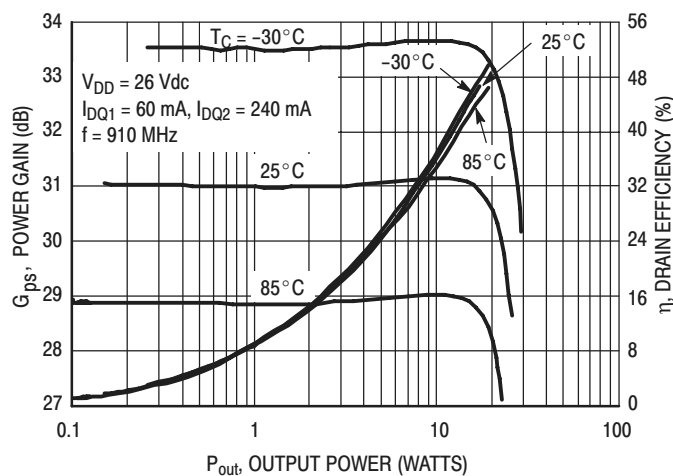


Figure 8. Power Gain and Efficiency versus Output Power

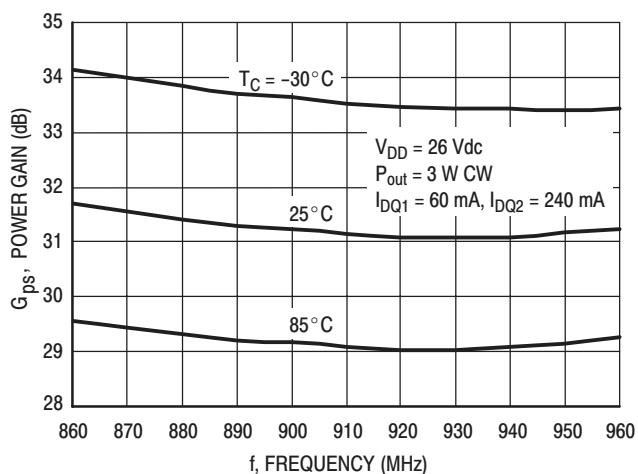


Figure 9. Power Gain versus Frequency

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TYPICAL CHARACTERISTICS (MOTOROLA REFERENCE BOARD) - CONTINUED

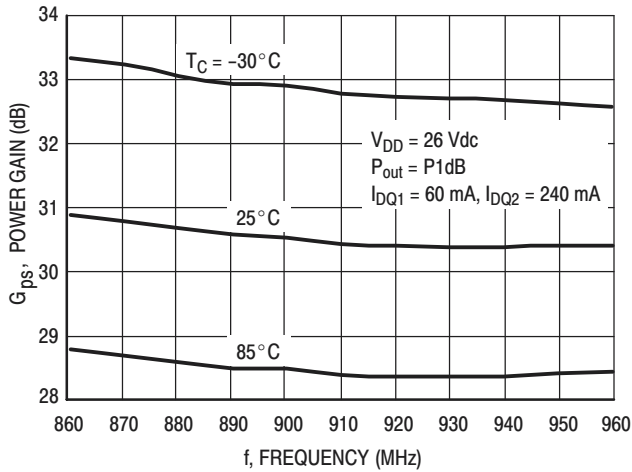


Figure 10. Power Gain versus Frequency

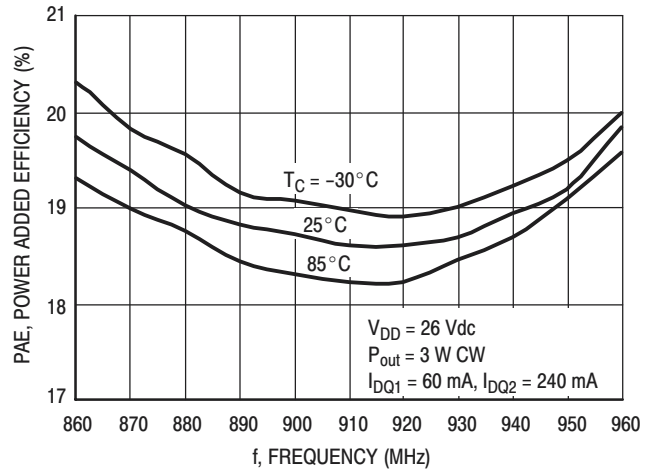


Figure 11. Power Added Efficiency versus Frequency

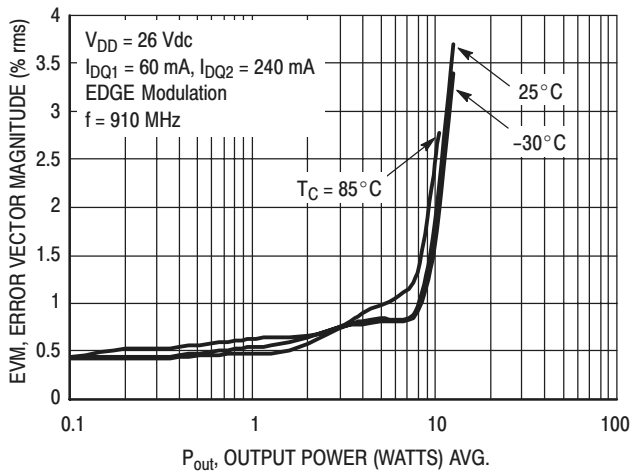


Figure 12. Error Vector Magnitude versus Output Power

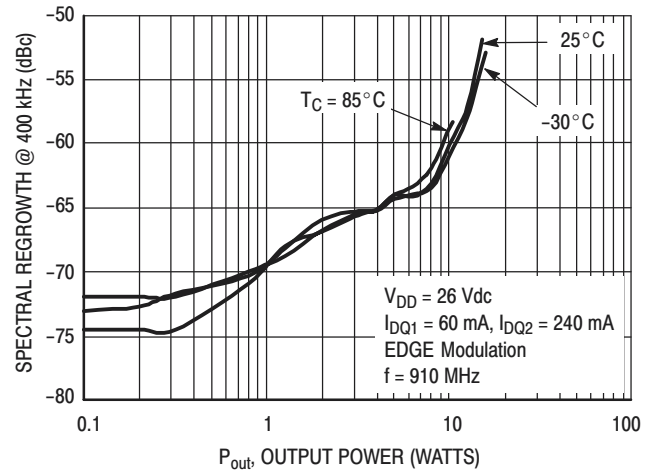


Figure 13. Spectral Regrowth at 400 kHz versus Output Power

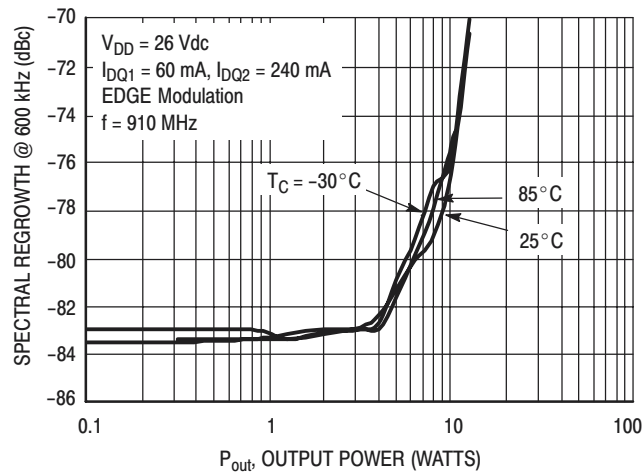
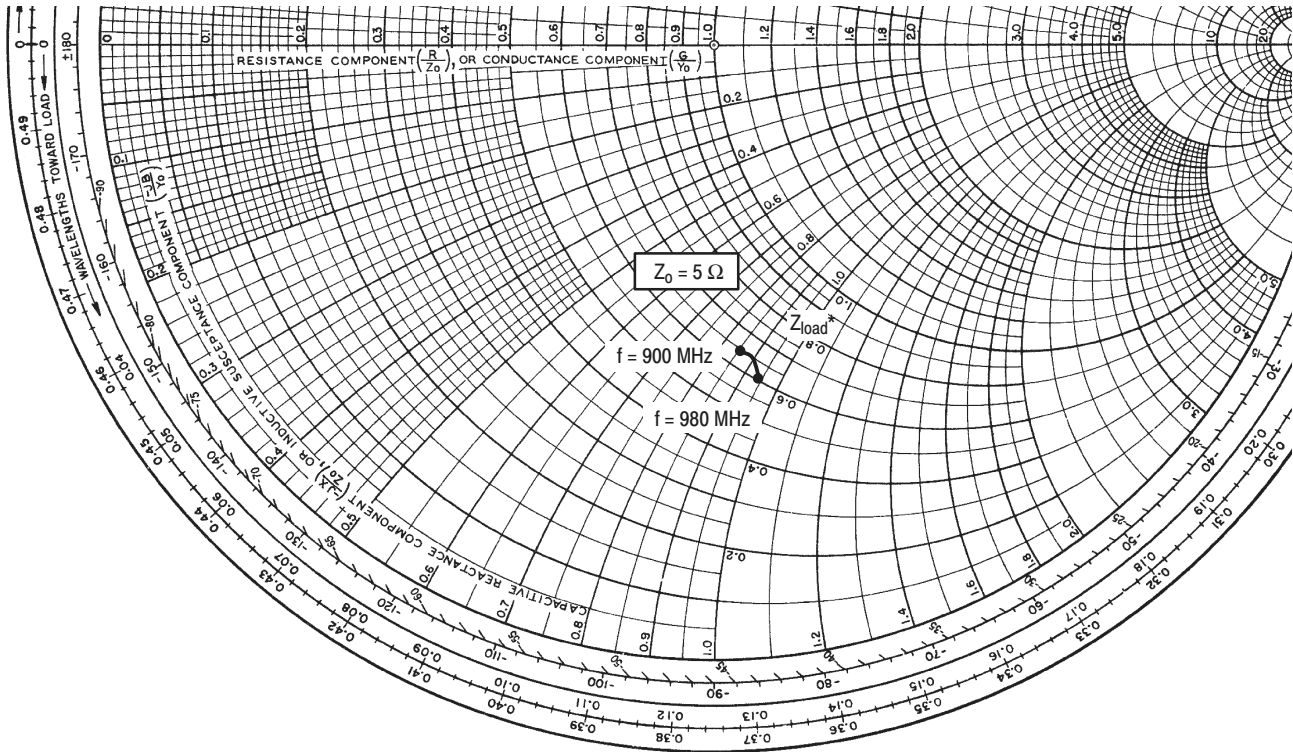


Figure 14. Spectral Regrowth at 600 kHz versus Output Power

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$V_{DD} = 26\text{ V}$, $I_{DQ1} = 60\text{ mA}$, $I_{DQ2} = 240\text{ mA}$, $P_{out} = P_{1dB}$

f MHz	Z_{load} Ω
900	3.23 - j4.30
910	3.24 - j4.36
920	3.25 - j4.42
930	3.25 - j4.47
940	3.23 - j4.52
950	3.21 - j4.56
960	3.16 - j4.60
970	3.11 - j4.65
980	3.04 - j4.70

Z_{load} = Test circuit impedance as measured from drain to ground.

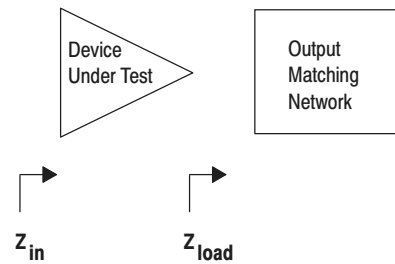


Figure 15. Series Equivalent Output Impedance

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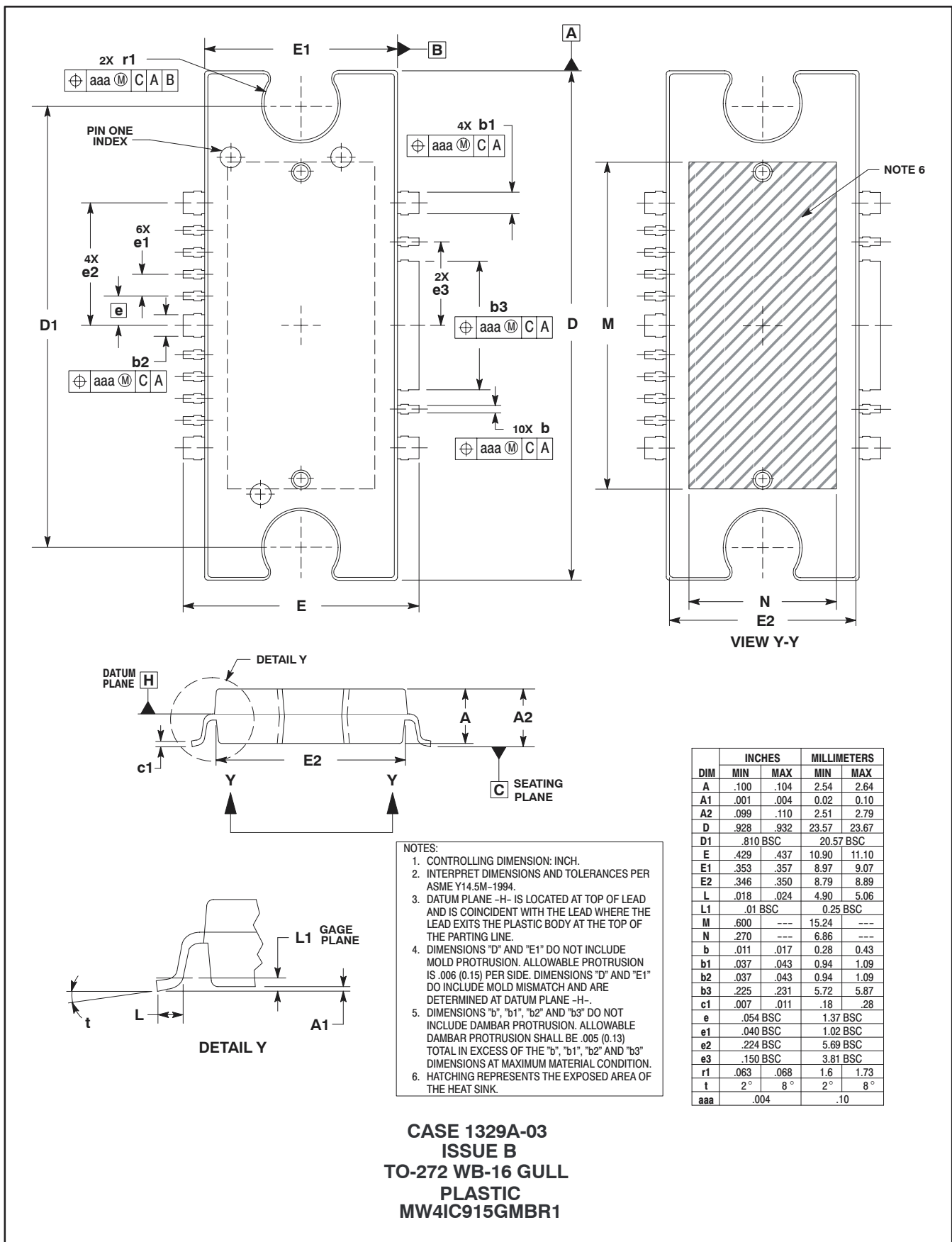
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