

RF LDMOS Integrated Power Amplifier

The MW6IC2420NB integrated circuit is designed with on-chip matching that makes it usable at 2450 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical industrial, scientific and medical modulation formats.

Driver Applications

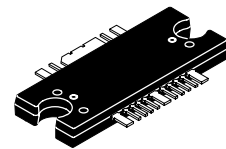
- Typical CW Performance at 2450 MHz: $V_{DD} = 28$ Volts, $I_{DQ1} = 210$ mA, $I_{DQ2} = 370$ mA, $P_{out} = 20$ Watts
 Power Gain — 19.5 dB
 Power Added Efficiency — 27%
- Capable of Handling 3:1 VSWR, @ 28 Vdc, 2170 MHz, 20 Watts CW Output Power
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 10 W CW P_{out} .

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >3 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function
- Integrated ESD Protection
- 200°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel

MW6IC2420NBR1

**2450 MHz, 20 W, 28 V
 CW
 RF LDMOS INTEGRATED POWER
 AMPLIFIER**



**CASE 1329-09
 TO-272 WB-16
 PLASTIC**

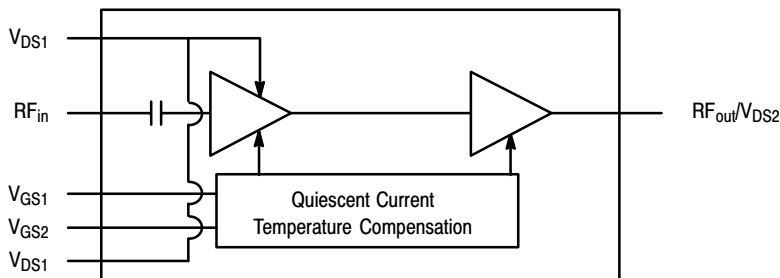
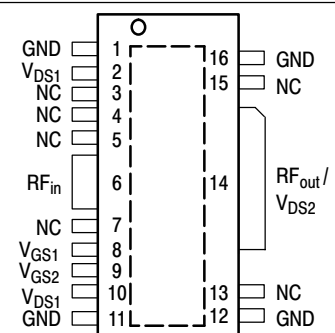


Figure 1. Functional Block Diagram



(Top View)

Note: Exposed backside of the package is the source terminal for the transistors.

Figure 2. Pin Connections

Table 1. Maximum Ratings

www.DataSheet4U.com

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +200	°C
Operating Junction Temperature	T_J	200	°C
Input Power	P_{in}	23	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value ⁽¹⁾	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
W-CDMA Application ($P_{out} = 4.5$ W Avg.)	Stage 1, 28 Vdc, $I_{DQ} = 210$ mA Stage 2, 28 Vdc, $I_{DQ} = 370$ mA	1.8 1	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Functional Tests (In Freescale Wideband 2110-2170 MHz Test Fixture, 50 ohm system) $V_{DD} = 28$ Vdc, $I_{DQ1} = 210$ mA, $I_{DQ2} = 370$ mA, $P_{out} = 4.5$ W Avg., $f_1 = 2112.5$ MHz, $f_2 = 2122.5$ MHz and $f_1 = 2157.5$ MHz, $f_2 = 2167.5$ MHz, 2-Carrier W-CDMA, 3.84 MHz Channel Bandwidth Carriers. ACPR measured in 3.84 MHz Channel Bandwidth @ ± 5 MHz Offset. IM3 measured in 3.84 MHz Channel Bandwidth @ ± 10 MHz Offset. PAR = 8.5 dB @ 0.01% Probability on CCDF.

Power Gain	G_{ps}	25.5	28	30	dB
Power Added Efficiency	PAE	13.7	15	—	%
Intermodulation Distortion	IM3	—	-43	-40	dBc
Adjacent Channel Power Ratio	ACPR	—	-46	-43	dBc
Input Return Loss	IRL	—	-15	-10	dB

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

(continued)

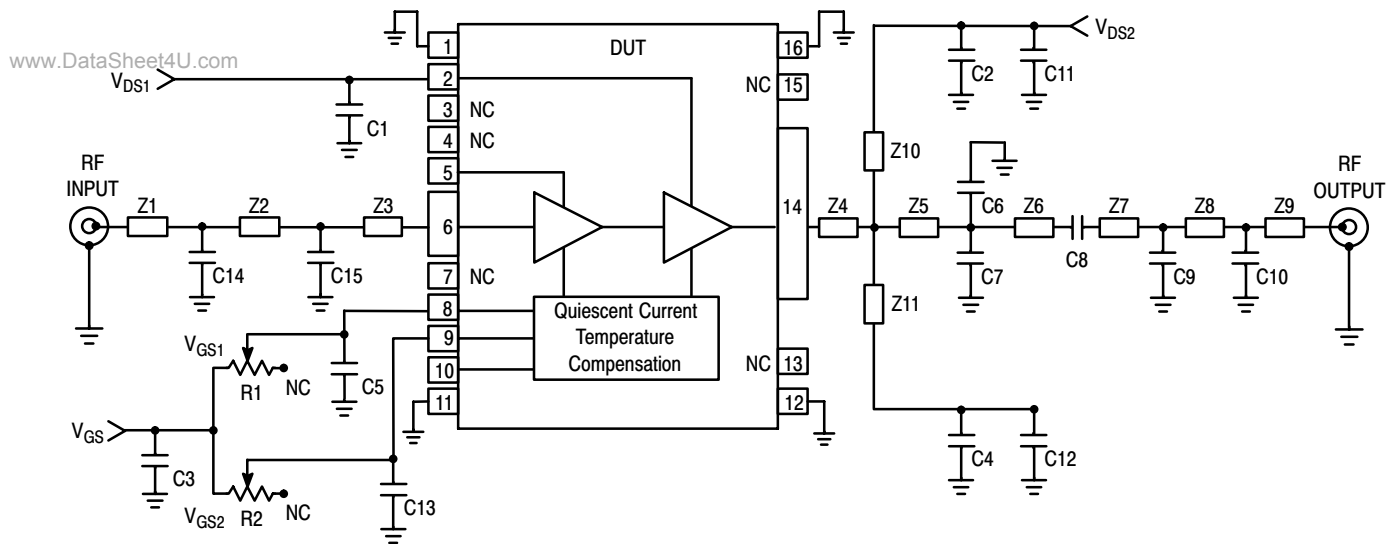
Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1} = 210\text{ mA}$, $I_{DQ2} = 370\text{ mA}$, 2110-2170 MHz					
Video Bandwidth @ 20 W PEP P_{out} where $IM3 = -30\text{ dBc}$ (Tone Spacing from 100 kHz to VBW) $\Delta IMD3 = IMD3 @ \text{VBW frequency} - IMD3 @ 100\text{ kHz} < 1\text{ dBc}$ (both sidebands)	VBW	—	30	—	MHz
Quiescent Current Accuracy over Temperature with 18 k Ω Gate Feed Resistors (-10 to 85°C) (1)	ΔI_{QT}	—	± 5	—	%
Gain Flatness in 30 MHz Bandwidth @ $P_{out} = 1\text{ W CW}$	G_F	—	0.2	—	dB
Average Deviation from Linear Phase in 30 MHz Bandwidth @ $P_{out} = 1\text{ W CW}$	Φ	—	2	—	°
Average Group Delay @ $P_{out} = 1\text{ W CW}$ Including Output Matching	Delay	—	2.8	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 1\text{ W CW}$, Six Sigma Window	$\Delta\Phi$	—	18	—	°

Table 6. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1} = 110\text{ mA}$, $I_{DQ2} = 370\text{ mA}$, 2110-2170 MHz					
Saturated Pulsed Output Power (8 μsec (on), 1 msec (off))	P_{sat}	—	60	—	W

1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977.



- | | | | |
|--------|----------------------------|----------|--|
| Z1 | 0.510" x 0.054" Microstrip | Z6 | 0.189" x 0.237" Microstrip |
| Z2 | 0.300" x 0.054" Microstrip | Z7 | 0.127" x 0.054" Microstrip |
| Z3, Z8 | 0.410" x 0.054" Microstrip | Z9 | 0.182" x 0.054" Microstrip |
| Z4 | 0.138" x 0.237" Microstrip | Z10, Z11 | 1.073" x 0.054" Microstrip |
| Z5 | 0.086" x 0.237" Microstrip | PCB | Taconic RF35, 0.020", $\epsilon_r = 3.5$ |

Figure 3. MW6IC2420NBR1 Test Circuit Schematic — 2450 MHz

Table 7. MW6IC2420NBR1 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4	2.2 μ F Chip Capacitors	C32225X5R1H225MT	TDK
C5, C13	100 nF Chip Capacitors	C1206C104K1KAC	Kemet
C6, C7	0.5 pF Chip Capacitors	08051J0R5BS	AVX
C8	6.8 pF Chip Capacitor	08051J6R8BS	AVX
C9	2.2 pF Chip Capacitor	08051J2R2BS	AVX
C10	1 pF Chip Capacitor	08051J1R0BS	AVX
C11, C12	5.6 pF Chip Capacitors	08051J5R6BS	AVX
C14	0.3 pF Chip Capacitor	ATC100B0R3BT500XT	ATC
C15	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
R1, R2	5 k Ω Potentiometer CMS Cermet Multi-turn	3224W-1-502E	Bourns

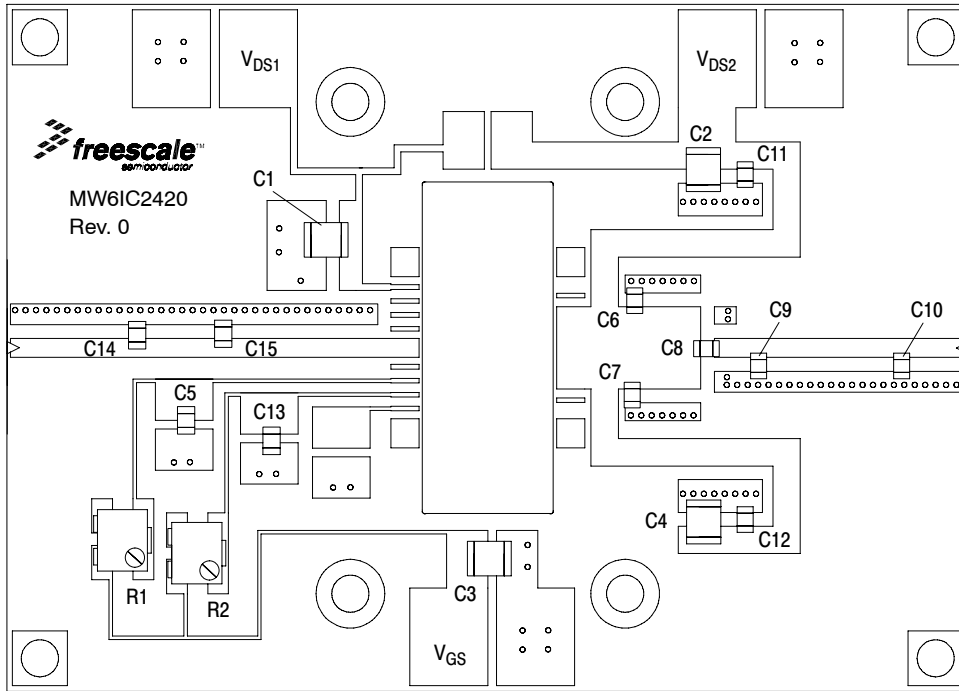


Figure 4. MW6IC2420NBR1 Test Circuit Component Layout — 2450 MHz

TYPICAL CHARACTERISTICS — 2450 MHz

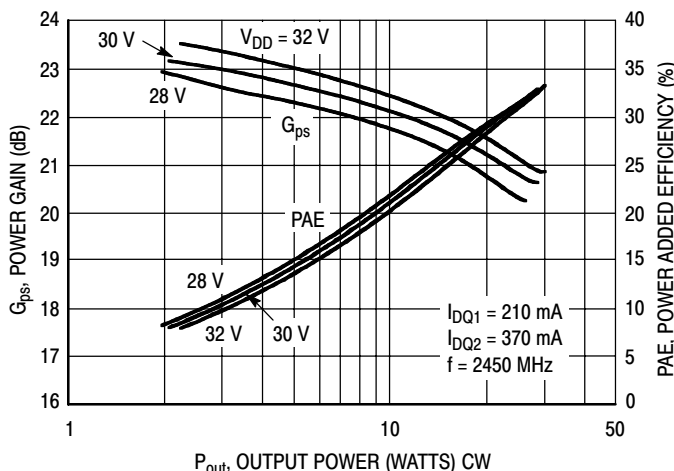


Figure 5. Power Gain and Power Added Efficiency versus CW Output Power as a Function of V_{DD}

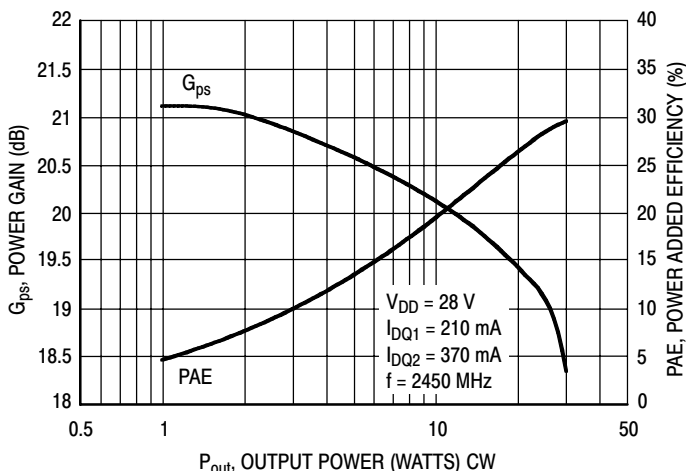


Figure 6. Power Gain and Power Added Efficiency versus CW Output Power

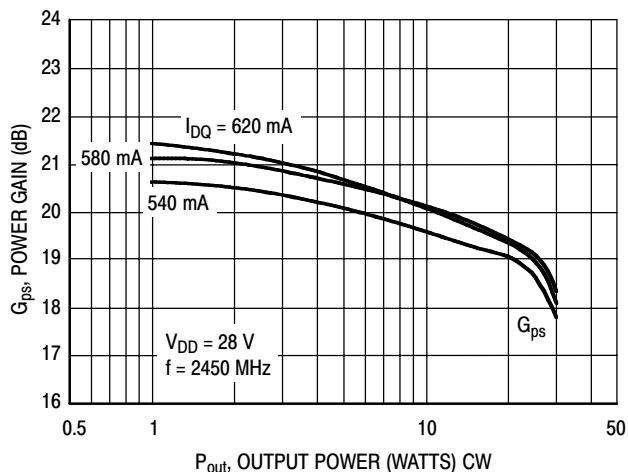
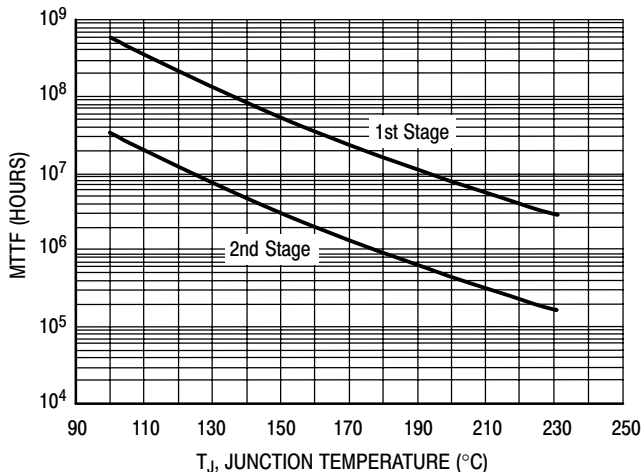


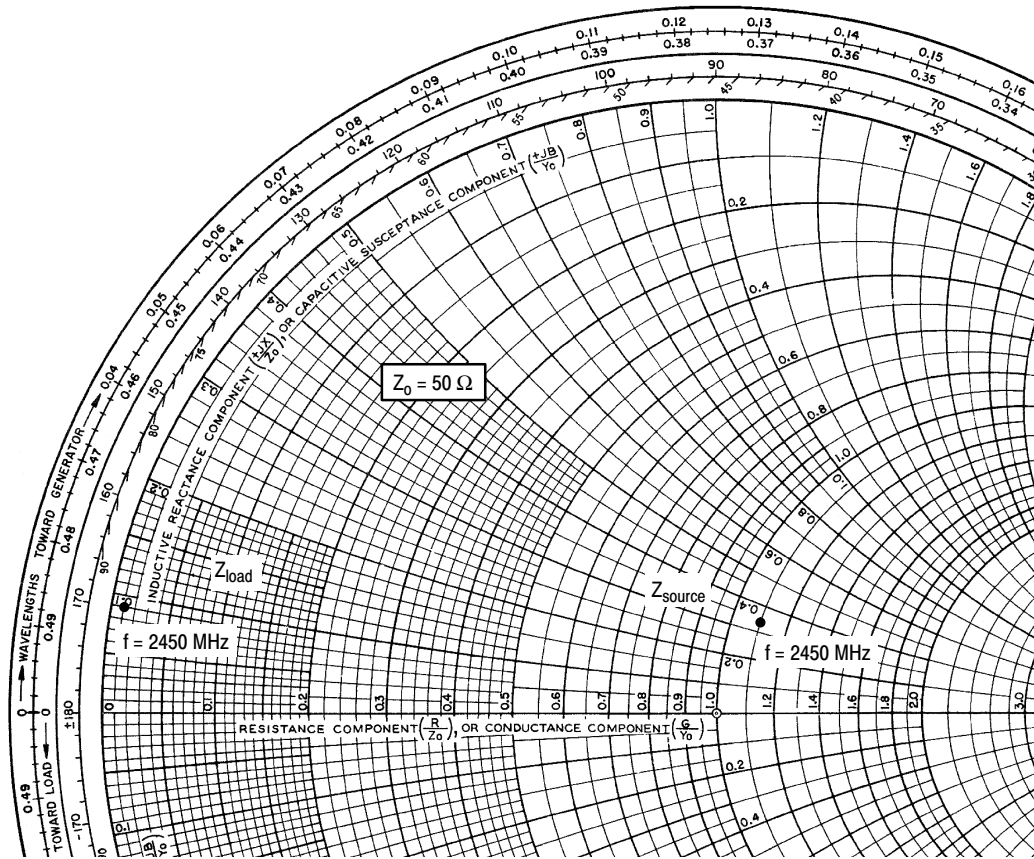
Figure 7. Power Gain and Power Added Efficiency versus CW Output Power as a Function of Total I_{DQ}



This above graph displays calculated MTTF in hours when the device is operated at $V_{DD} = 28$ Vdc, $P_{out} = 20$ W Avg., and PAE = 27%.

MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.

Figure 8. MTTF versus Junction Temperature



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1} = 210 \text{ mA}$, $I_{DQ2} = 370 \text{ mA}$, $P_{out} = 20 \text{ W CW}$

f MHz	Z_{source} Ω	Z_{load} Ω
2450	$54.8 + j16.6$	$0.42 + j4.3$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

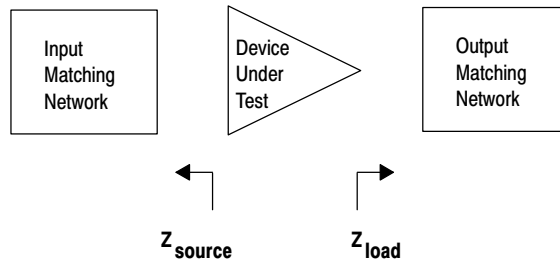
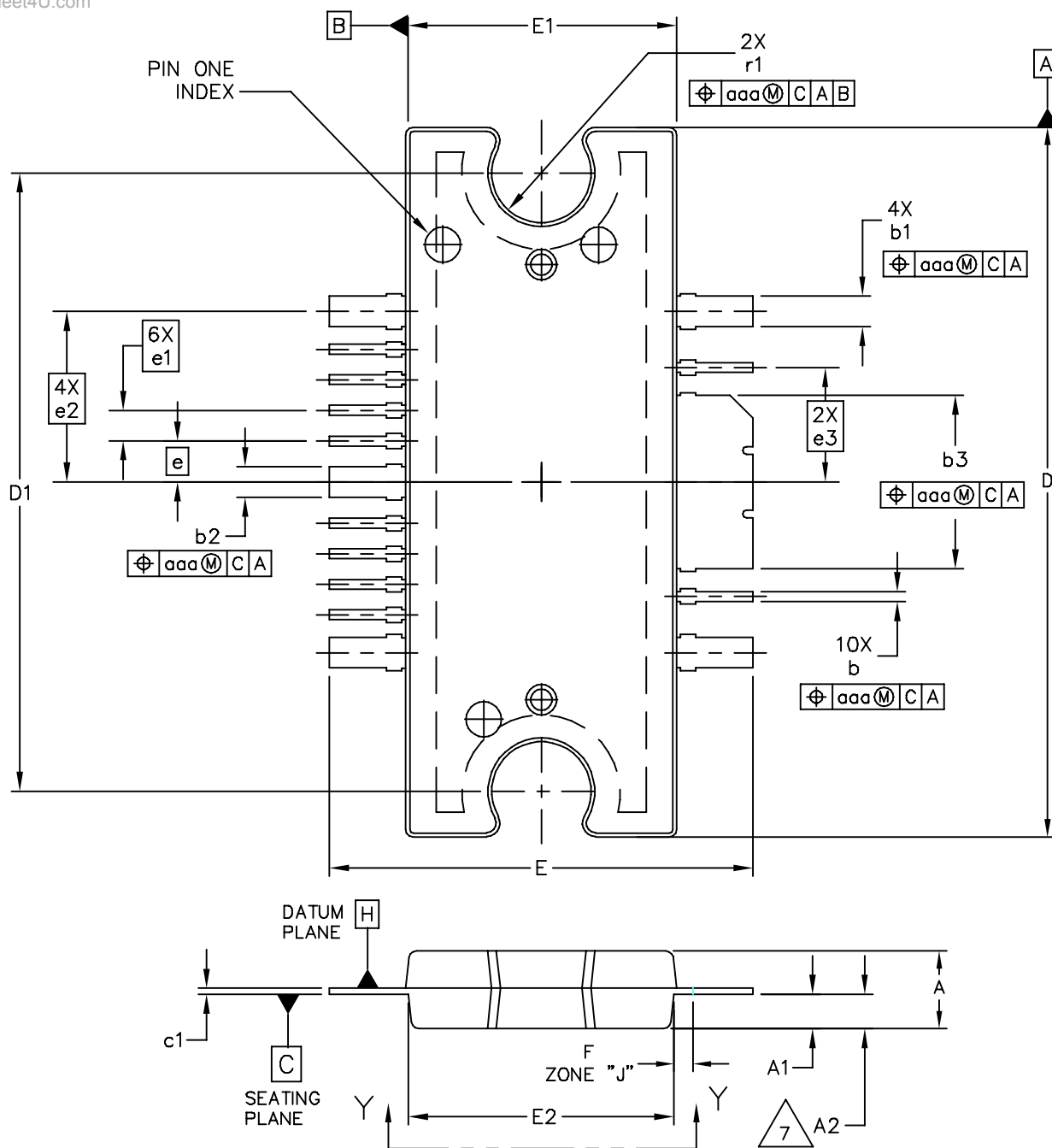
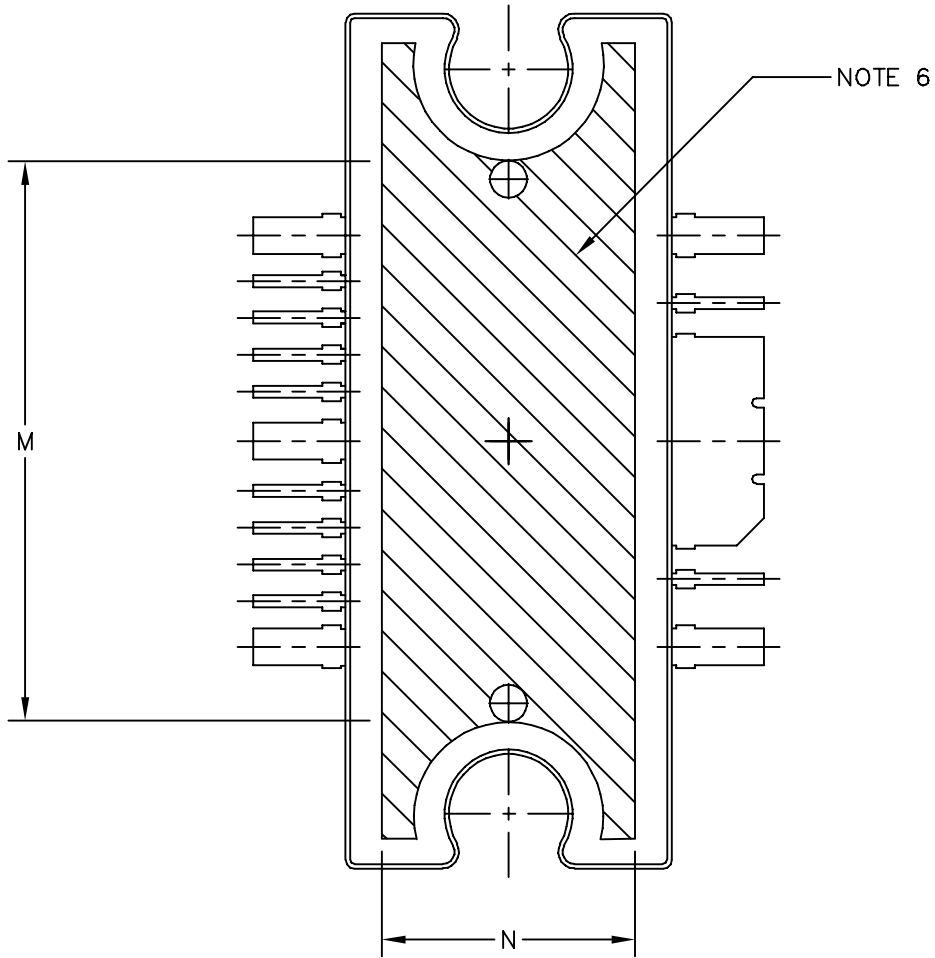


Figure 9. Series Equivalent Source and Load Impedance

PACKAGE DIMENSIONS



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A		REV: L
	CASE NUMBER: 1329-09		13 MAR 2006
	STANDARD: NON-JEDEC		



VIEW Y-Y

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A	REV: L	
	CASE NUMBER: 1329-09	13 MAR 2006	
	STANDARD: NON-JEDEC		

NOTES:

www.DataSheet4U.com

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.		MECHANICAL OUTLINE		PRINT VERSION NOT TO SCALE	
TITLE: TO-272 WIDE BODY MULTI-LEAD	DOCUMENT NO: 98ARH99164A		REV: L		
	CASE NUMBER: 1329-09		13 MAR 2006		
	STANDARD: NON-JEDEC				

PRODUCT DOCUMENTATION

www.DataSheet4U.com

Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Mar. 2007	<ul style="list-style-type: none">• Initial Release of Data Sheet

How to Reach Us:

Home Page:

www.freescale.com

Web Support:

<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:

Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2007. All rights reserved.

