



# RF LDMOS Wideband Integrated Power Amplifiers

The MW7IC2040N wideband integrated circuit is designed with on-chip matching that makes it usable from 1805 to 1990 MHz. This multi-stage structure is rated for 24 to 32 Volt operation and covers all typical cellular base station modulations.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 130$  mA,  $I_{DQ2} = 330$  mA,  $P_{out} = 4$  Watts Avg.,  $f = 1932.5$ , Channel Bandwidth = 3.84 MHz, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.
  - Power Gain — 32 dB
  - Power Added Efficiency — 17.5%
  - ACPR @ 5 MHz Offset — -50 dBc in 3.84 MHz Bandwidth
- Capable of Handling 5:1 VSWR, @ 32 Vdc, 1960 MHz, 50 Watts CW Output Power (3 dB Input Overdrive from Rated  $P_{out}$ )
- Stable into a 3:1 VSWR. All Spurs Below -60 dBc @ 100 mW to 40 Watts CW  $P_{out}$ .
- Typical  $P_{out}$  @ 1 dB Compression Point  $\approx 30$  Watts CW

## GSM EDGE Application

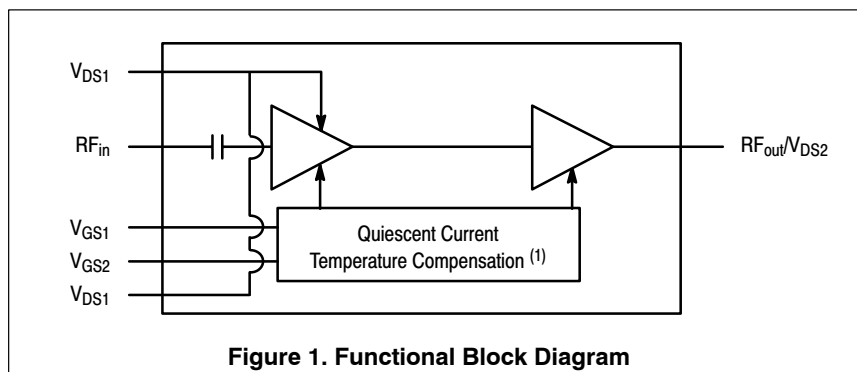
- Typical GSM EDGE Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 90$  mA,  $I_{DQ2} = 430$  mA,  $P_{out} = 16$  Watts Avg., 1805-1880 MHz
  - Power Gain — 33 dB
  - Power Added Efficiency — 35%
  - Spectral Regrowth @ 400 kHz Offset = -62 dBc
  - Spectral Regrowth @ 600 kHz Offset = -77 dBc
  - EVM — 1.5% rms

## GSM Application

- Typical GSM Performance:  $V_{DD} = 28$  Volts,  $I_{DQ1} = 90$  mA,  $I_{DQ2} = 430$  mA,  $P_{out} = 40$  Watts CW, 1805-1880 MHz and 1930-1990 MHz
  - Power Gain — 31 dB
  - Power Added Efficiency — 50%

## Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source S-Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked, >3 Ohm Output)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

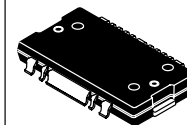
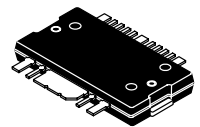


1. Refer to AN1977, Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family and to AN1987, Quiescent Current Control for the RF Integrated Circuit Device Family. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

**MW7IC2040NR1**  
**MW7IC2040GNR1**  
**MW7IC2040NBR1**

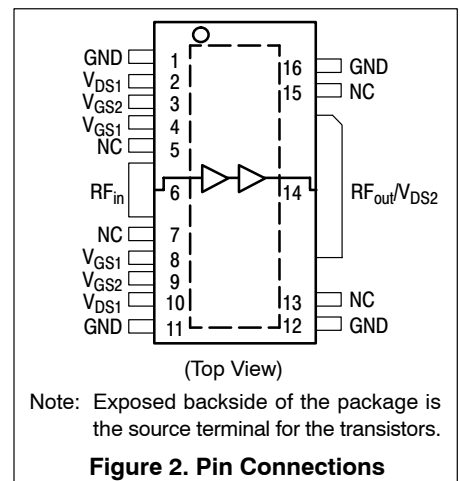
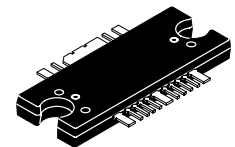
**1930-1990 MHz, 1805-1880 MHz,  
 4 W AVG., 28 V  
 SINGLE W-CDMA, GSM EDGE, GSM  
 RF LDMOS WIDEBAND  
 INTEGRATED POWER AMPLIFIERS**

**CASE 1886-01**  
**TO-270 WB-16**  
**PLASTIC**  
**MW7IC2040NR1**



**CASE 1887-01**  
**TO-270 WB-16 GULL**  
**PLASTIC**  
**MW7IC2040GNR1**

**CASE 1329-09**  
**TO-272 WB-16**  
**PLASTIC**  
**MW7IC2040NBR1**



**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-0.5, +65	Vdc
Gate-Source Voltage	$V_{GS}$	-0.5, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	150	°C
Operating Junction Temperature (1,2)	$T_J$	225	°C
Input Power	$P_{in}$	25	dBm

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
W-CDMA ( $P_{out} = 4$ W Avg., Case Temperature = 73°C)	Stage 1, 28 Vdc, $I_{DQ1} = 130$ mA Stage 2, 28 Vdc, $I_{DQ2} = 330$ mA	4.0 1.5	
GSM EDGE ( $P_{out} = 16$ W Avg., Case Temperature = 76°C)	Stage 1, 28 Vdc, $I_{DQ1} = 130$ mA Stage 2, 28 Vdc, $I_{DQ2} = 330$ mA	4.1 1.4	
GSM ( $P_{out} = 40$ W Avg., Case Temperature = 79°C)	Stage 1, 28 Vdc, $I_{DQ1} = 130$ mA Stage 2, 28 Vdc, $I_{DQ2} = 330$ mA	3.9 1.3	

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22-A114)	1C (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

**Table 4. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 1 — Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$
<b>Stage 1 — On Characteristics</b>					
Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 25$ $\mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28$ Vdc, $I_{DQ1} = 130$ mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_{DQ1} = 130$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	13	14.5	16	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

(continued)

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Stage 2 — Off Characteristics</b>					
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28\text{ Vdc}$ , $V_{GS} = 0\text{ Vdc}$ )	$I_{DSS}$	—	—	1	$\mu\text{Adc}$
Gate-Source Leakage Current ( $V_{GS} = 1.5\text{ Vdc}$ , $V_{DS} = 0\text{ Vdc}$ )	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**Stage 2 — On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 140\ \mu\text{Adc}$ )	$V_{GS(th)}$	1.2	2	2.7	Vdc
Gate Quiescent Voltage ( $V_{DS} = 28\text{ Vdc}$ , $I_{DQ2} = 330\text{ mAdc}$ )	$V_{GS(Q)}$	—	2.8	—	Vdc
Fixture Gate Quiescent Voltage ( $V_{DD} = 28\text{ Vdc}$ , $I_{DQ2} = 330\text{ mAdc}$ , Measured in Functional Test)	$V_{GG(Q)}$	7	8	9	Vdc
Drain-Source On-Voltage ( $V_{GS} = 10\text{ Vdc}$ , $I_D = 1\text{ Adc}$ )	$V_{DS(on)}$	0.2	0.39	1.2	Vdc

**Stage 2 — Dynamic Characteristics** (1)

Output Capacitance ( $V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$ )	$C_{oss}$	—	246	—	pF
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**Functional Tests** (3) (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 130\text{ mA}$ ,  $I_{DQ2} = 330\text{ mA}$ ,  $P_{out} = 4\text{ W Avg.}$ ,  $f = 1932.5\text{ MHz}$ , Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 45.2% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5\text{ MHz}$  Offset.

Power Gain	$G_{ps}$	29.5	32	34.5	dB
Power Added Efficiency	PAE	16	17.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-50	-46	dBc
Input Return Loss	IRL	—	-15	-8	dB

**Typical Performances** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 130\text{ mA}$ ,  $I_{DQ2} = 330\text{ mA}$ , 1930-1990 MHz

$P_{out}$ @ 1 dB Compression Point, CW	$P_{1dB}$	—	30	—	W
IMD Symmetry @ 22 W PEP, $P_{out}$ where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands > 2 dB)	$IMD_{sym}$	—	60	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	65	—	MHz
Quiescent Current Accuracy over Temperature (2) with 5.6 k $\Omega$ Gate Feed Resistors (-30 to 85°C)	$\Delta I_{QT}$	—	$\pm 3$	—	%
Gain Flatness in 60 MHz Bandwidth @ $P_{out} = 4\text{ W Avg.}$	$G_F$	—	1.2	—	dB
Average Deviation from Linear Phase in 60 MHz Bandwidth @ $P_{out} = 30\text{ W CW}$	$\Phi$	—	0.5	—	°
Average Group Delay @ $P_{out} = 30\text{ W CW}$ , $f = 1960\text{ MHz}$	Delay	—	2.5	—	ns
Part-to-Part Insertion Phase Variation @ $P_{out} = 30\text{ W CW}$ , $f = 1960\text{ MHz}$ , Six Sigma Window	$\Delta\Phi$	—	33	—	°
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.029	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P_{1dB}$	—	0.003	—	dBm/°C

1. Part internally matched both on input and output.
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.
3. Measurement made with device in straight lead configuration before any lead forming operation is applied.

(continued)

MW7IC2040NR1 MW7IC2040GNR1 MW7IC2040NBR1

**Table 5. Electrical Characteristics** ( $T_C = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Typical W-CDMA Performance — 1800 MHz</b> (In Freescale W-CDMA 1805-1880 MHz Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ1} = 130\text{ mA}$ , $I_{DQ2} = 330\text{ mA}$ , $P_{out} = 4\text{ W Avg.}$ , 1805-1880 MHz, Single-Carrier W-CDMA, 3GPP Test Model 1, 64 DPCH, 45.2% Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ $\pm 5\text{ MHz}$ Offset.					
Power Gain	$G_{ps}$	—	33.5	—	dB
Power Added Efficiency	PAE	—	16.5	—	%
Adjacent Channel Power Ratio	ACPR	—	-50	—	dBc
Input Return Loss	IRL	—	-6	—	dB

**Typical GSM EDGE Performance — 1800 MHz** (In Freescale GSM EDGE 1805-1880 MHz Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $P_{out} = 16\text{ W Avg.}$ ,  $I_{DQ1} = 90\text{ mA}$ ,  $I_{DQ2} = 430\text{ mA}$ , 1805-1880 MHz EDGE Modulation

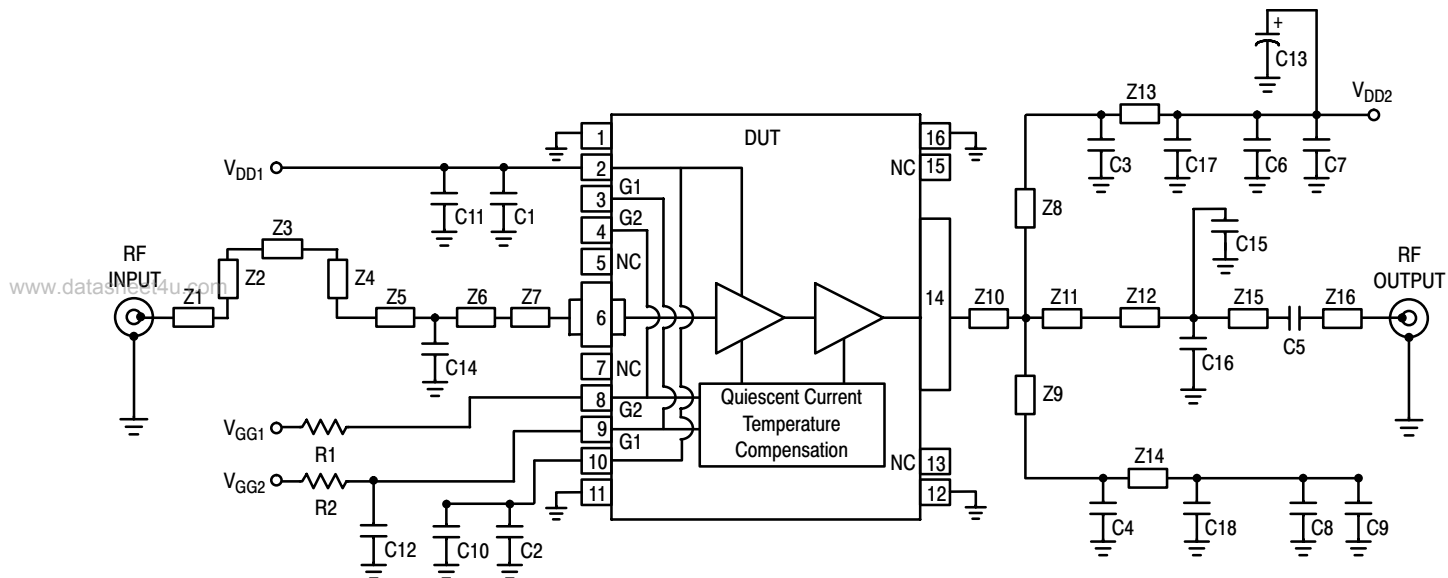
Power Gain	$G_{ps}$	—	33	—	dB
Power Added Efficiency	PAE	—	35	—	%
Error Vector Magnitude	EVM	—	1.5	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-77	—	dBc

**Typical GSM EDGE Performance — 1900 MHz** (In Freescale GSM EDGE 1930-1990 MHz Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $P_{out} = 16\text{ W Avg.}$ ,  $I_{DQ1} = 90\text{ mA}$ ,  $I_{DQ2} = 430\text{ mA}$ , 1930-1990 MHz EDGE Modulation

Power Gain	$G_{ps}$	—	30	—	dB
Power Added Efficiency	PAE	—	33	—	%
Error Vector Magnitude	EVM	—	1.5	—	% rms
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-80	—	dBc

**Typical CW Performance** (In Freescale GSM EDGE 1930-1990 MHz Test Fixture, 50 ohm system)  $V_{DD} = 28\text{ Vdc}$ ,  $I_{DQ1} = 90\text{ mA}$ ,  $I_{DQ2} = 430\text{ mA}$ ,  $P_{out} = 40\text{ W CW}$ , 1805-1880 MHz and 1930-1990 MHz

Power Gain	$G_{ps}$	—	31	—	dB
Power Added Efficiency	PAE	—	50	—	%
Input Return Loss	IRL	—	-15	—	dB
$P_{out}$ @ 1 dB Compression Point	P1dB	—	45	—	W



Z1	0.0826" x 0.5043" Microstrip	Z10	0.3419" x 0.1725" Microstrip
Z2	0.0826" x 0.3639" Microstrip	Z11	0.3419" x 0.4671" Microstrip
Z3	0.0826" x 0.4258" Microstrip	Z12	0.0830" x 0.4220" Microstrip
Z4	0.0826" x 0.3639" Microstrip	Z13, Z14	0.0830" x 0.2855" Microstrip
Z5	0.0826" x 0.3060" Microstrip	Z15	0.0830" x 0.9030" Microstrip
Z6	0.0826" x 0.9290" Microstrip	Z16	0.0830" x 0.2499" Microstrip
Z7	0.0600" x 0.1273" Microstrip	PCB	Rogers RO4350, 0.030", $\epsilon_r = 3.5$
Z8, Z9	0.0800" x 1.3684" Microstrip		

Figure 3. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Schematic — 1930-1990 MHz

Table 6. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1930-1990 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C6, C7, C8, C9, C10, C11	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C12	2.2 $\mu$ F, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C13	470 $\mu$ F, 63 V Electrolytic Capacitor, Radial	MCGPR63V477M13X26-RH	Multicomp
C14, C16	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
C15	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C17, C18	1 $\mu$ F, 50 V Chip Capacitors	GRM21BR71H105KA12L	Murata
R1, R2	5.6 K $\Omega$ , 1/4 W Chip Resistors	CRCW12065601FKEA	Vishay

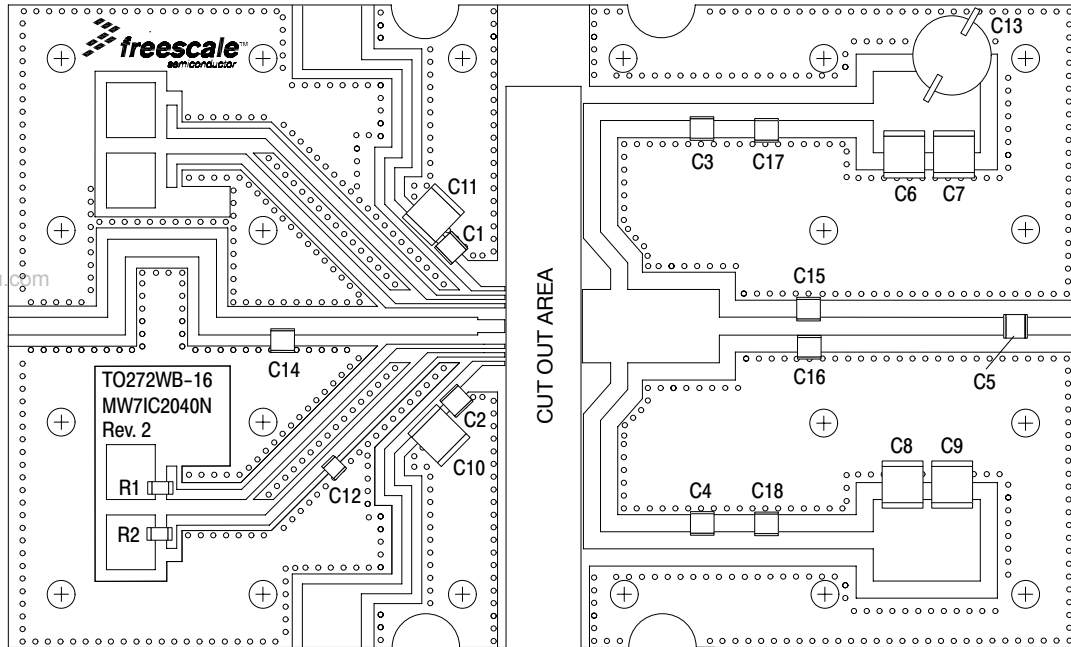


Figure 4. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Layout — 1930-1990 MHz

## TYPICAL CHARACTERISTICS

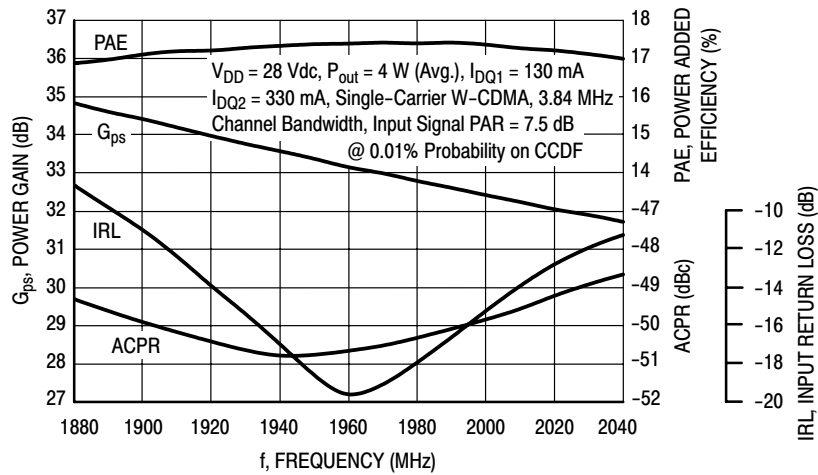


Figure 5. Single Carrier W-CDMA Broadband Performance  
@  $P_{out} = 4$  Watts Avg.

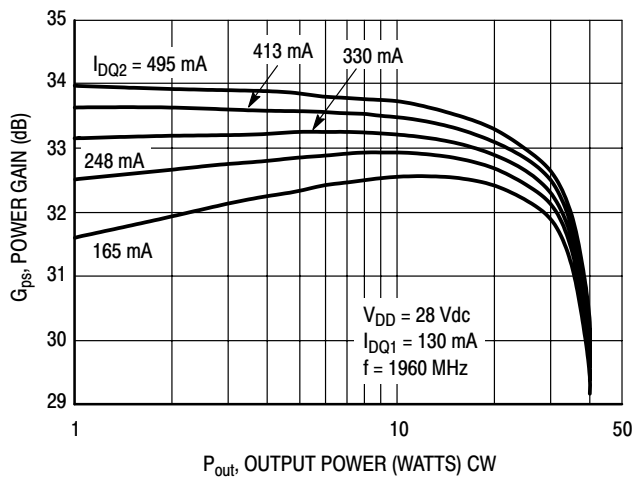


Figure 6. Power Gain versus Output Power  
@  $I_{DQ1} = 130$  mA

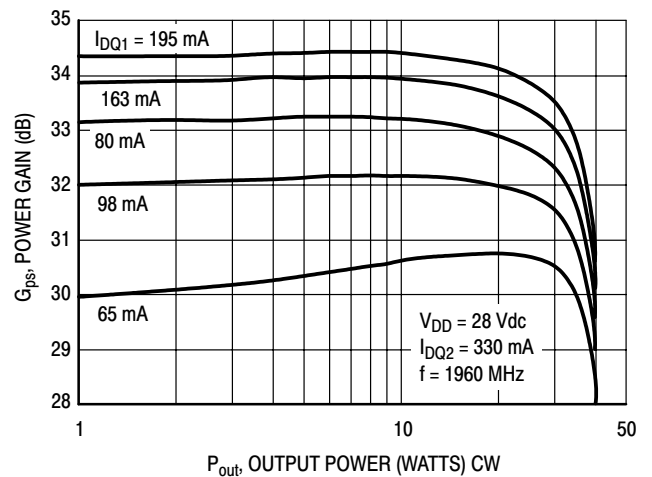


Figure 7. Power Gain versus Output Power  
@  $I_{DQ2} = 330$  mA

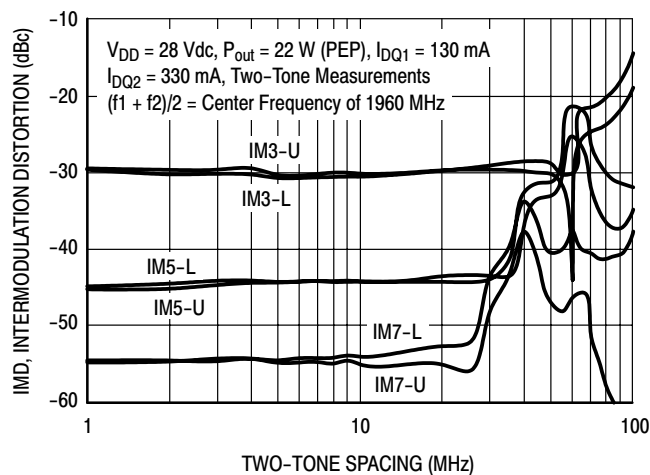
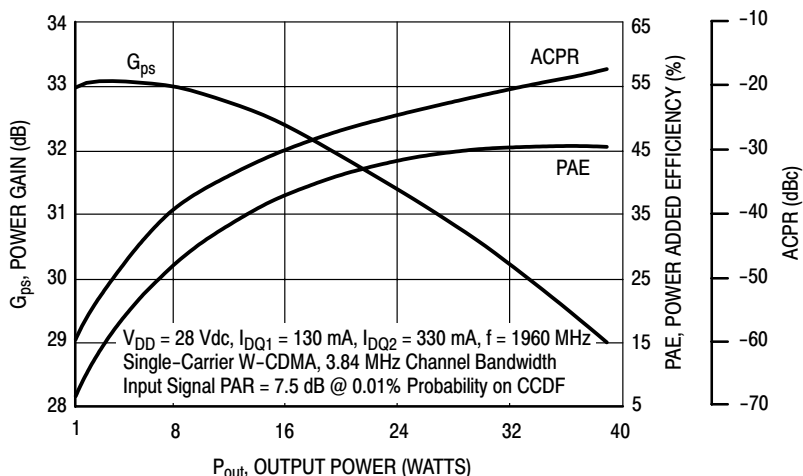
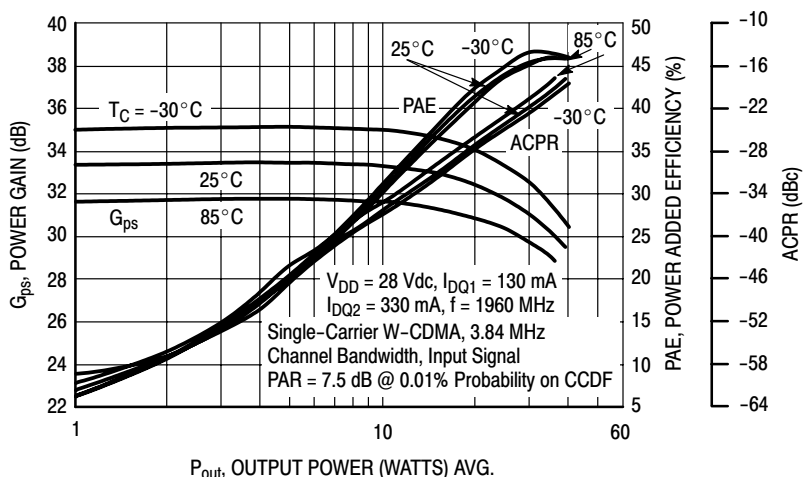


Figure 8. Intermodulation Distortion Products  
versus Two-Tone Spacing

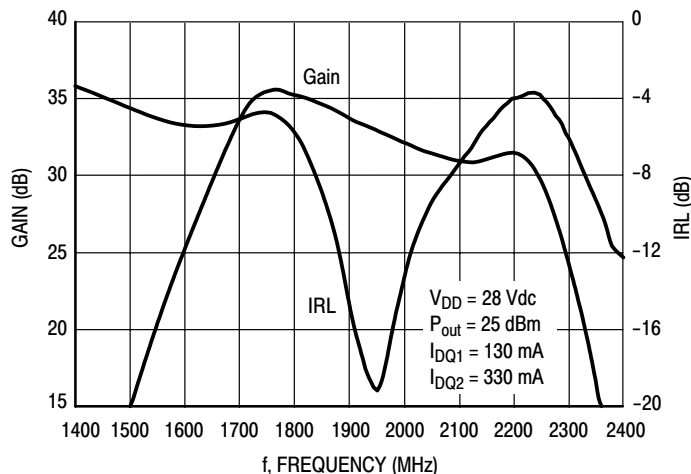
### TYPICAL CHARACTERISTICS



**Figure 9. Power Gain, ACPR and Power Added Efficiency versus Output Power**



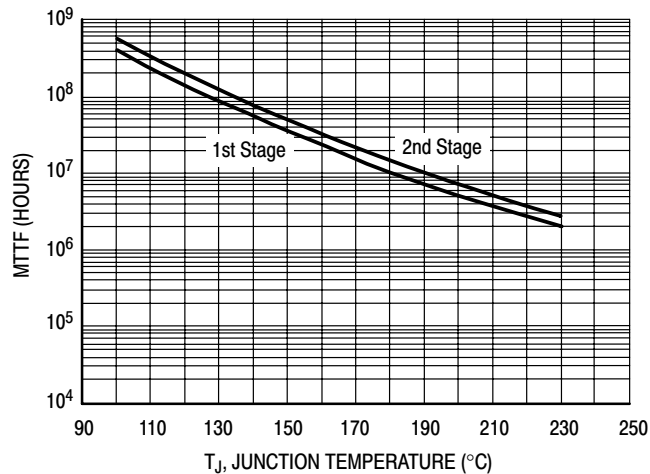
**Figure 10. Single-Carrier W-CDMA Power Gain, Power Added Efficiency and ACPR versus Output Power**



**Figure 11. Broadband Frequency Response**



## TYPICAL CHARACTERISTICS



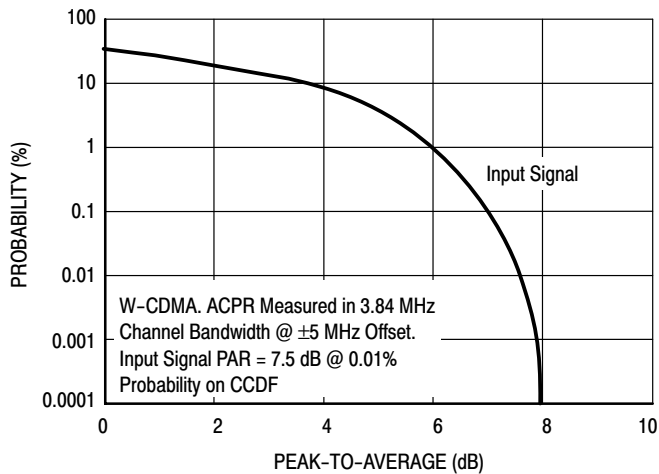
www.datasheet4u.com

This above graph displays calculated MTTF in hours when the device is operated at  $V_{DD} = 28$  Vdc,  $P_{out} = 4$  W Avg., and PAE = 17.5%.

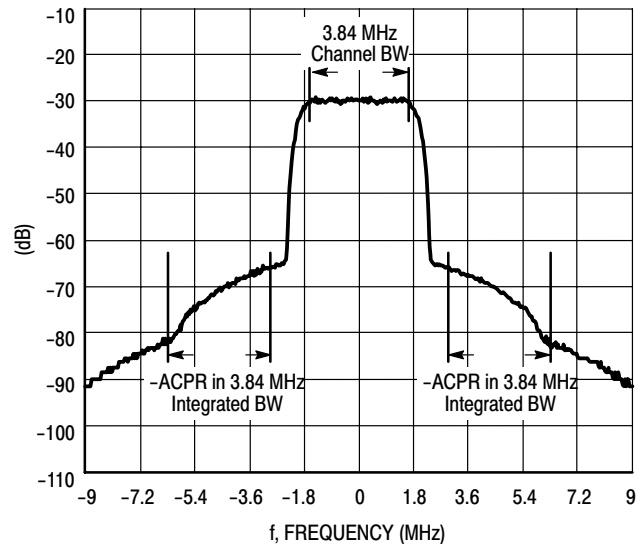
MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

**Figure 12. MTTF versus Junction Temperature**

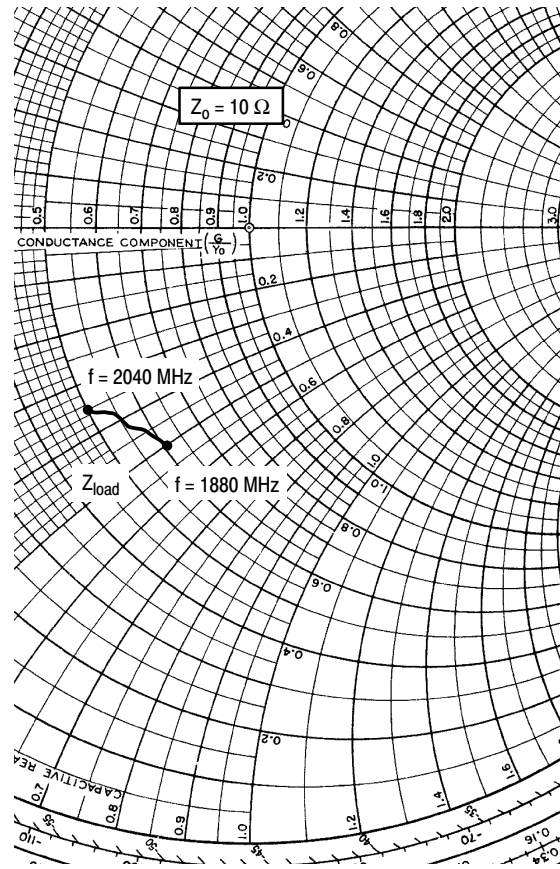
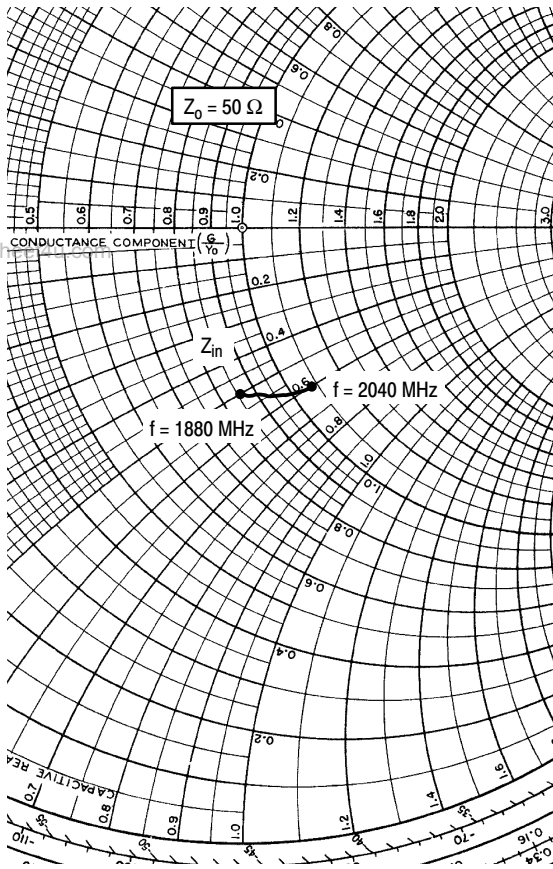
## W-CDMA TEST SIGNAL



**Figure 13. CCDF W-CDMA 3GPP, Test Model 1, 64 DPCH, 45.2% Clipping, Single-Carrier Test Signal**



**Figure 14. Single-Carrier W-CDMA Spectrum**



$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ1} = 130 \text{ mA}$ ,  $I_{DQ2} = 330 \text{ mA}$ ,  $P_{out} = 4 \text{ W Avg.}$

f MHz	$Z_{in}$ $\Omega$	$Z_{load}$ $\Omega$
1880	42.97 - j25.07	6.10 - j5.01
1900	44.01 - j25.91	5.92 - j4.71
1920	45.14 - j26.72	5.76 - j4.44
1940	46.38 - j27.48	5.62 - j4.21
1960	47.71 - j28.19	5.51 - j4.01
1980	49.16 - j28.83	5.40 - j3.83
2000	50.71 - j29.40	5.27 - j3.71
2020	52.36 - j29.87	5.13 - j3.60
2040	54.12 - j30.23	4.99 - j3.52

$Z_{in}$  = Device input impedance as measured from gate to ground.

$Z_{load}$  = Test circuit impedance as measured from drain to ground.

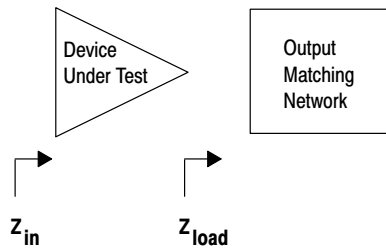
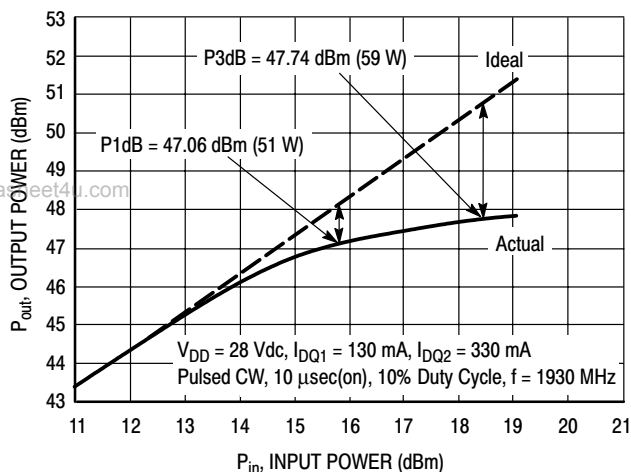


Figure 15. Series Equivalent Input and Load Impedance

## ALTERNATIVE PEAK TUNE LOAD PULL CHARACTERISTICS

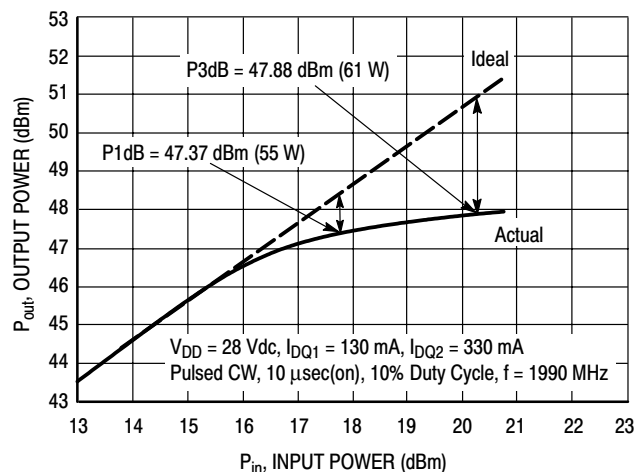


NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P1dB	49.30 + j8.40	3.60 - j4.50

**Figure 16. Pulsed CW Output Power versus Input Power @ 28 V @ 1930 MHz**



NOTE: Load Pull Test Fixture Tuned for Peak P1dB Output Power @ 28 V

Test Impedances per Compression Level

	$Z_{source}$ $\Omega$	$Z_{load}$ $\Omega$
P1dB	50.0 - j4.90	3.40 - j5.10

**Figure 17. Pulsed CW Output Power versus Input Power @ 28 V @ 1990 MHz**

**Table 7. Common Source S-Parameters** ( $V_{DD} = 28\text{ V}$ ,  $I_{DQ1} = 90\text{ mA}$ ,  $I_{DQ2} = 430\text{ mA}$ ,  $T_C = 25^\circ\text{C}$ , 50 Ohm System)

f MHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	S <sub>11</sub>	∠φ	S <sub>21</sub>	∠φ	S <sub>12</sub>	∠φ	S <sub>22</sub>	∠φ
1500	0.595	-118.5	2.110	-151.3	0.00174	-71.2	0.888	-160.3
1550	0.545	-147.4	3.851	178.9	0.00192	-86.7	0.876	170.4
1600	0.482	-176.5	7.415	144.7	0.00294	-114.0	0.867	137.1
1650	0.398	156.7	15.620	103.6	0.00445	-149.9	0.872	94.6
1700	0.332	146.1	37.544	45.5	0.00746	177.5	0.884	29.4
1750	0.542	116.5	62.685	-48.6	0.00940	110.9	0.650	-93.8
1800	0.488	59.6	50.513	-124.5	0.00642	67.4	0.454	157.6
1850	0.373	8.7	42.562	-178.8	0.00497	40.5	0.419	105.4
1900	0.294	-46.7	38.690	132.3	0.00438	19.1	0.416	75.9
1950	0.269	-107.0	36.138	85.3	0.00416	-7.3	0.443	54.0
2000	0.297	-161.3	33.838	39.7	0.00382	-28.5	0.497	31.7
2050	0.342	154.0	32.122	-4.7	0.00350	-50.7	0.553	8.0
2100	0.389	114.8	30.682	-48.5	0.00342	-69.9	0.602	-16.3
2150	0.420	78.2	29.594	-92.4	0.00354	-84.6	0.640	-41.0
2200	0.424	41.2	28.734	-137.7	0.00396	-101.3	0.666	-65.4
2250	0.388	2.9	27.277	175.2	0.00425	-125.1	0.689	-89.2
2300	0.302	-37.2	24.568	126.4	0.00483	-153.1	0.720	-113.5
2350	0.188	-78.8	20.404	78.5	0.00470	174.4	0.753	-138.7
2400	0.066	-123.6	16.281	33.8	0.00415	148.7	0.778	-163.6
2450	0.034	55.1	12.661	-8.6	0.00388	124.4	0.806	171.0
2500	0.104	12.1	9.738	-48.2	0.00368	106.5	0.826	145.2
2550	0.154	-17.7	7.577	-85.7	0.00328	77.5	0.842	119.7
2600	0.191	-44.6	5.905	-121.7	0.00281	57.2	0.851	94.4
2700	0.250	-94.4	3.679	169.8	0.00245	37.8	0.856	45.7
2750	0.278	-118.4	2.921	136.7	0.00271	19.5	0.854	22.1
2800	0.309	-142.0	2.330	104.5	0.00373	2.2	0.854	-0.5
2850	0.343	-165.3	1.874	72.7	0.00250	-19.6	0.849	-23.5
2900	0.382	171.0	1.518	41.5	0.00286	-40.7	0.851	-46.0
2950	0.420	147.7	1.226	10.6	0.00313	-71.3	0.850	-68.4
3000	0.459	124.6	0.985	-19.8	0.00262	-98.0	0.851	-91.1
3050	0.498	102.9	0.782	-49.0	0.00101	-108.5	0.847	-113.4
3100	0.542	79.6	0.641	-76.9	0.00279	-84.9	0.850	-136.3
3150	0.577	56.4	0.531	-105.1	0.00504	-110.7	0.856	-159.8
3200	0.603	33.6	0.439	-133.3	0.00526	-152.0	0.857	176.4
3250	0.628	11.0	0.363	-161.1	0.00587	-176.6	0.858	152.0
3300	0.654	-11.9	0.303	171.0	0.00659	160.1	0.857	126.8
3350	0.661	-35.4	0.250	143.7	0.00909	129.6	0.853	101.4
3400	0.678	-57.0	0.208	115.4	0.00691	98.1	0.845	74.5
3450	0.692	-80.2	0.157	88.5	0.00718	80.9	0.745	42.1
3500	0.704	-103.7	0.158	71.5	0.01000	46.8	0.760	43.7

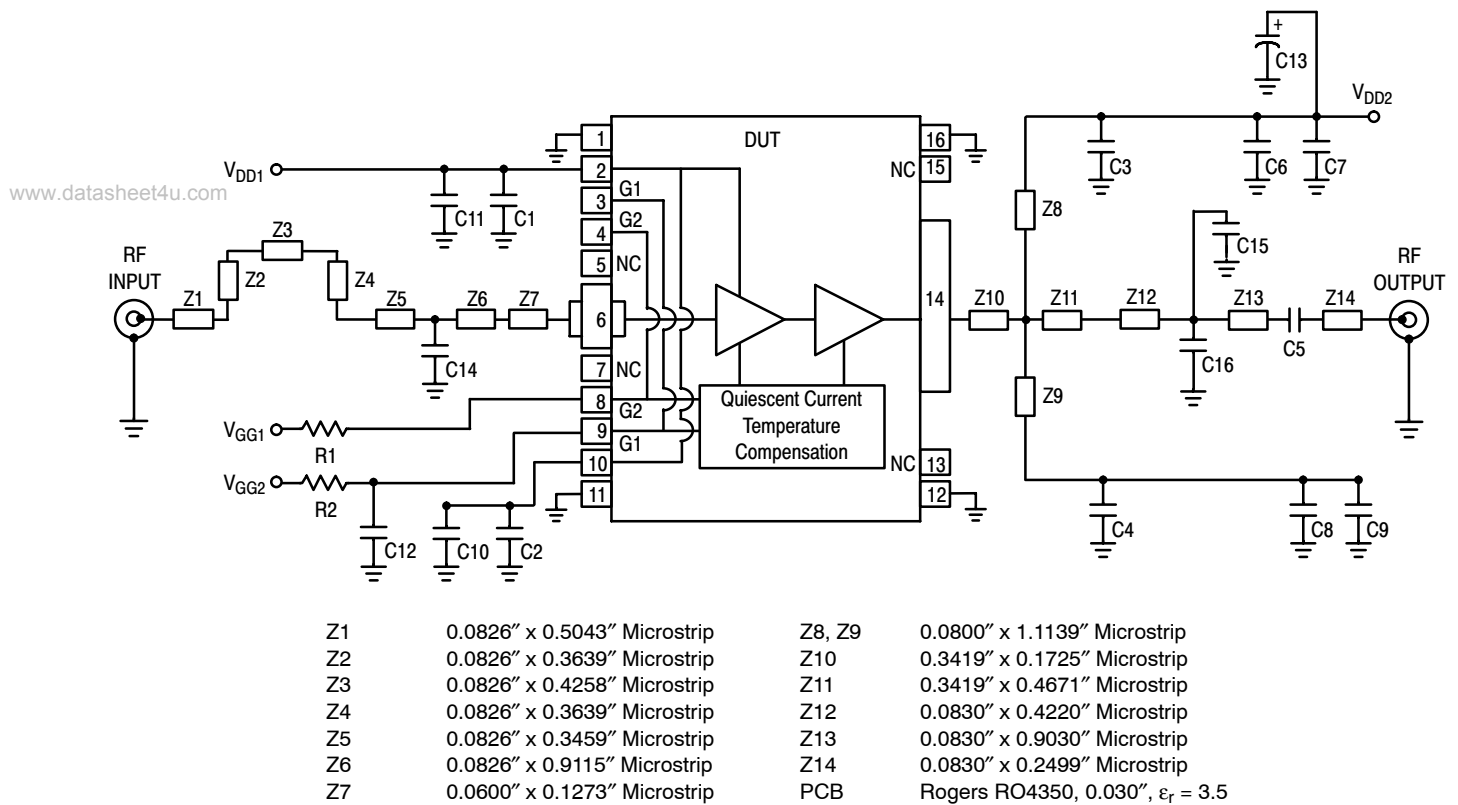


Figure 18. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Schematic — 1805-1880 MHz

Table 8. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1805-1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C6, C7, C8, C9, C10, C11	10 μF, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C12	2.2 μF, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C13	470 μF, 63 V Electrolytic Capacitor, Radial	MCGPR63V477M13X26-RH	Multicomp
C14, C15, C16	1 pF Chip Capacitors	ATC100B1R0BT500XT	ATC
R1, R2	5.6 KΩ, 1/4 W Chip Resistors	CRCW12065601FKEA	Vishay

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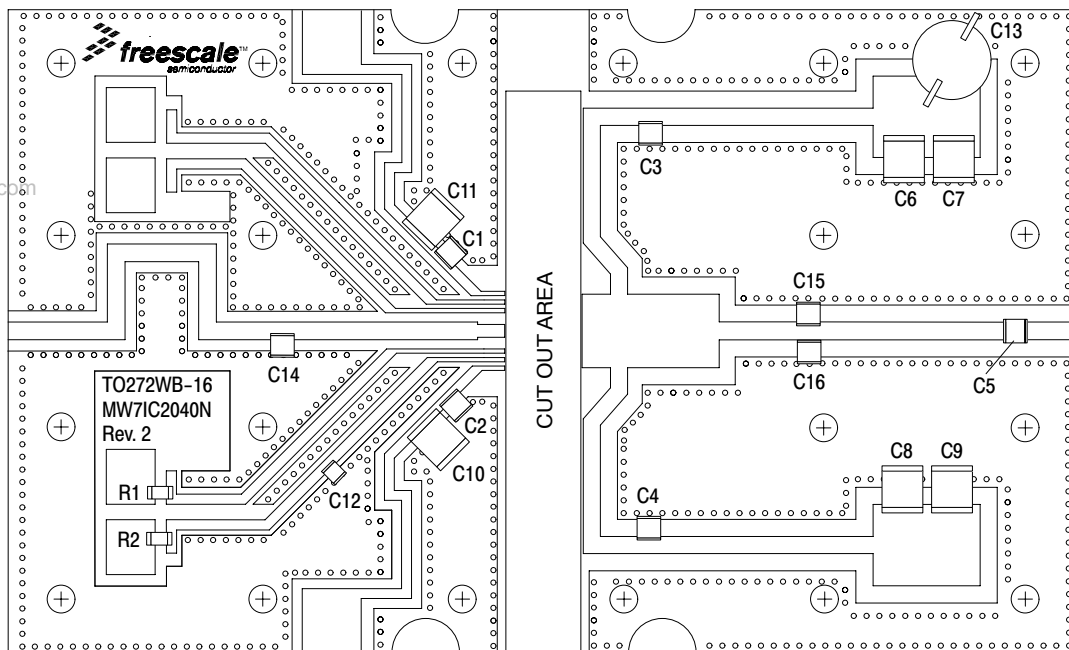
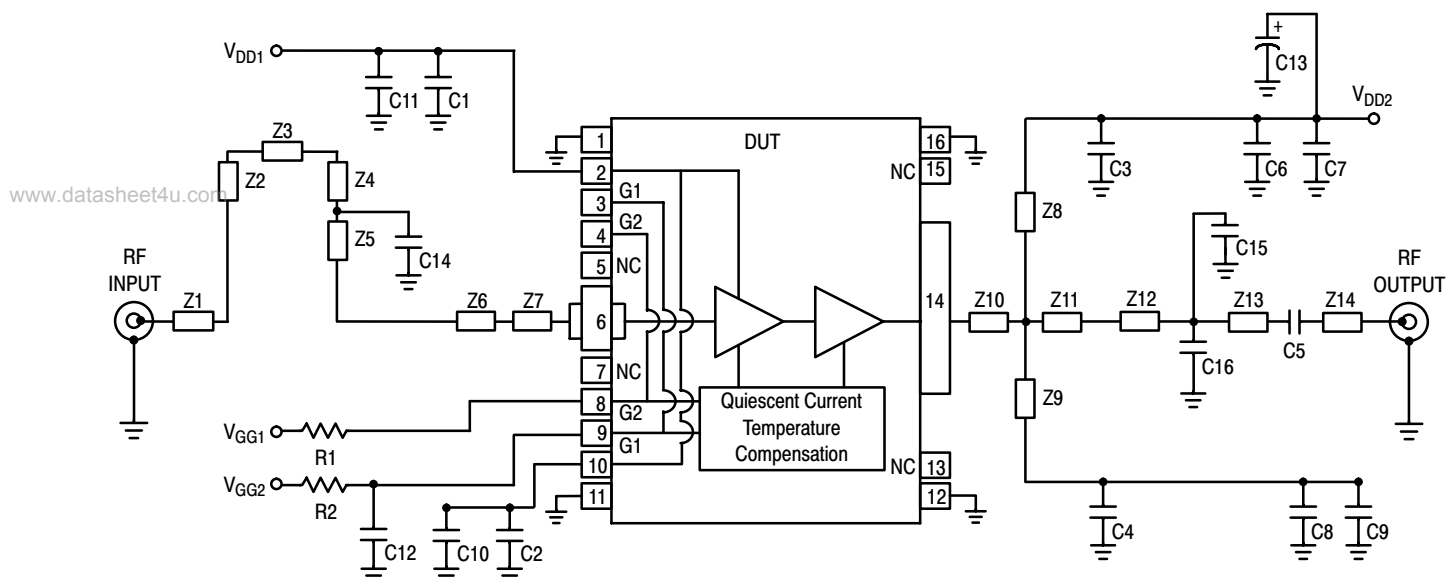


Figure 19. MW71C2040NR1(GNR1)(NBR1) Test Circuit Component Layout — 1805-1880 MHz

## GSM EDGE — 1805-1880 MHz



Z1	0.0826" x 0.5043" Microstrip	Z8, Z9	0.0800" x 1.3354" Microstrip
Z2	0.0826" x 0.3639" Microstrip	Z10	0.3419" x 0.1725" Microstrip
Z3	0.0826" x 0.4258" Microstrip	Z11	0.3419" x 0.4671" Microstrip
Z4	0.0826" x 0.2315" Microstrip	Z12	0.0830" x 0.3575" Microstrip
Z5	0.0826" x 0.1324" Microstrip	Z13	0.0830" x 0.9675" Microstrip
Z6	0.0826" x 1.2574" Microstrip	Z14	0.0830" x 0.2499" Microstrip
Z7	0.0600" x 0.1273" Microstrip	PCB	Rogers RO4350, 0.030", $\epsilon_r = 3.5$

**Figure 20. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Schematic — 1805-1880 MHz**

**Table 9. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1805-1880 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C6, C7, C8, C9, C10, C11	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C12	2.2 $\mu$ F, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C13	470 $\mu$ F, 63 V Electrolytic Capacitor, Radial	MCGPR63V477M13X26-RH	Multicomp
C14	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C15	1 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
C16	1.2 pF Chip Capacitor	ATC100B1R2BT500XT	ATC
R1, R2	5.6 K $\Omega$ , 1/4 W Chip Resistors	CRCW12065601FKEA	Vishay

GSM EDGE — 1805-1880 MHz

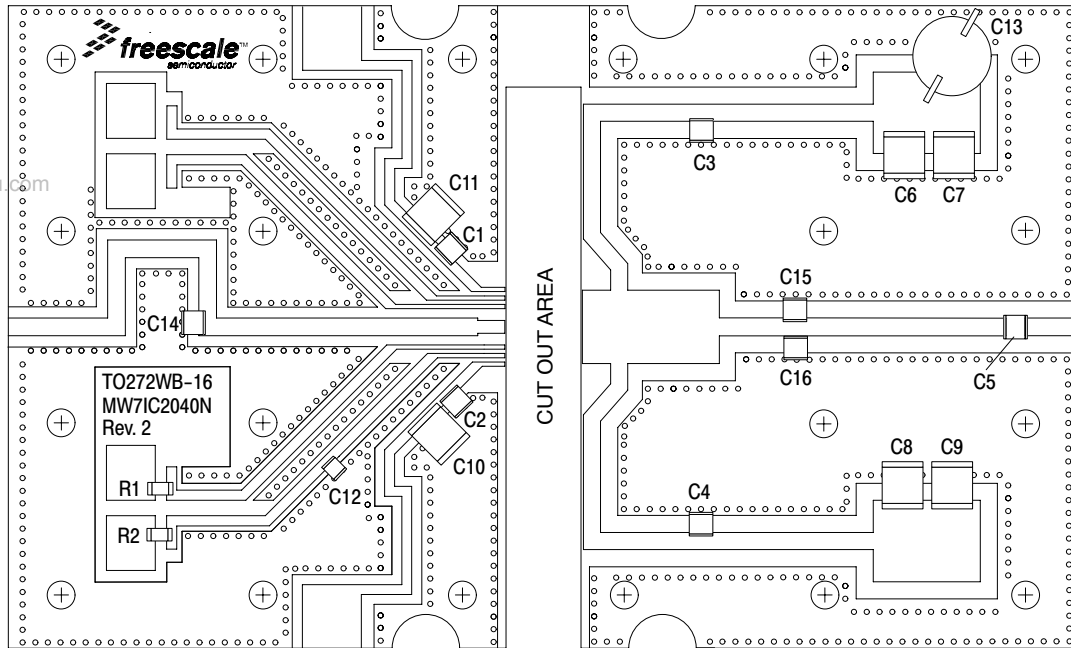
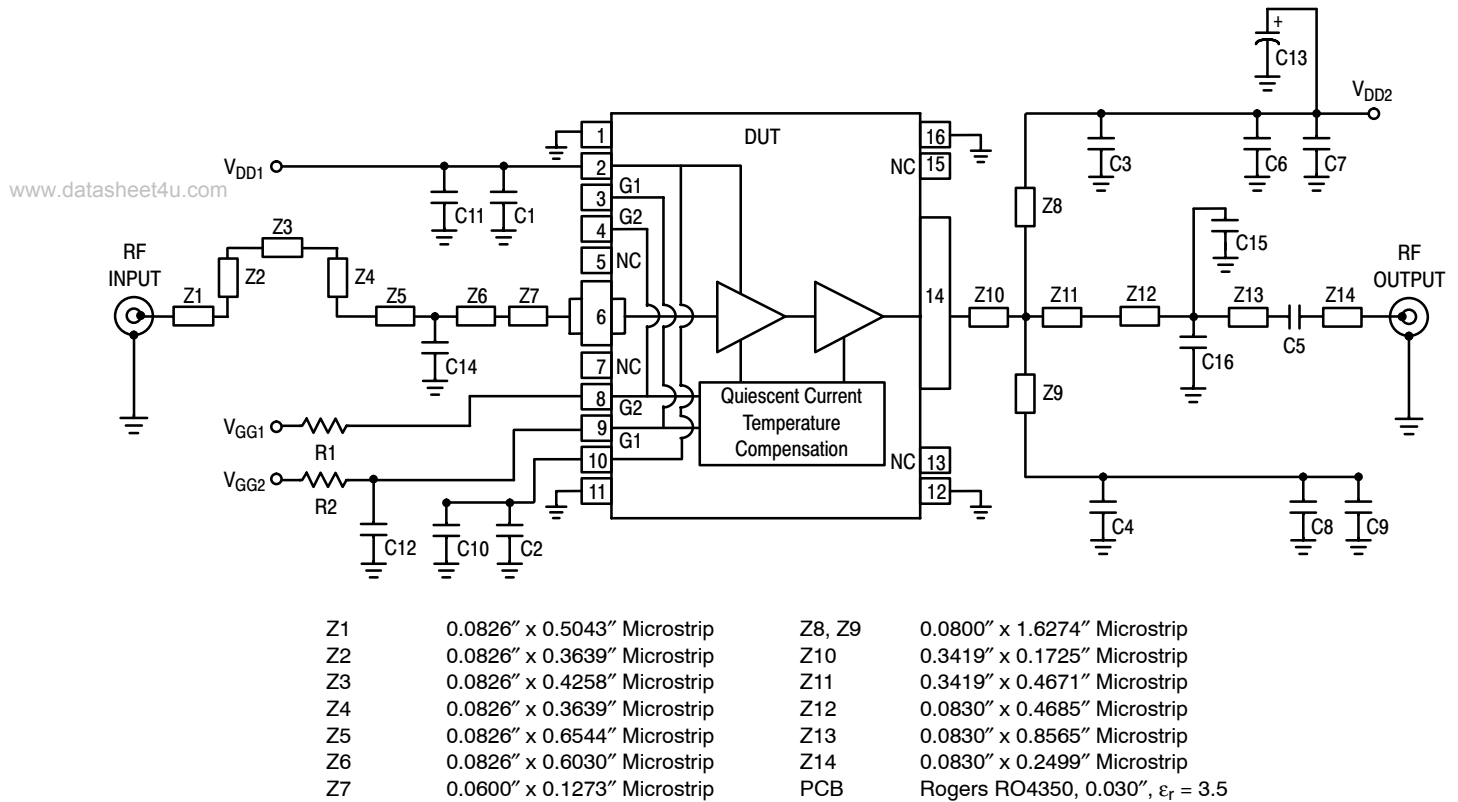


Figure 21. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Layout — 1805-1880 MHz



## GSM EDGE — 1930-1990 MHz



**Figure 22. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Schematic — 1930-1990 MHz**

**Table 10. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Designations and Values — 1930-1990 MHz**

Part	Description	Part Number	Manufacturer
C1, C2, C3, C4, C5	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C6, C7, C8, C9, C10, C11	10 $\mu$ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C12	2.2 $\mu$ F, 16 V Chip Capacitor	C1206C225K4RAC	Kemet
C13	470 $\mu$ F, 63 V Electrolytic Capacitor, Radial	MCGPR63V477M13X26-RH	Multicomp
C14	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C15, C16	0.8 pF Chip Capacitors	ATC100B0R8BT500XT	ATC
R1, R2	5.6 K $\Omega$ , 1/4 W Chip Resistors	CRCW12065601FKEA	Vishay

GSM EDGE — 1930-1990 MHz

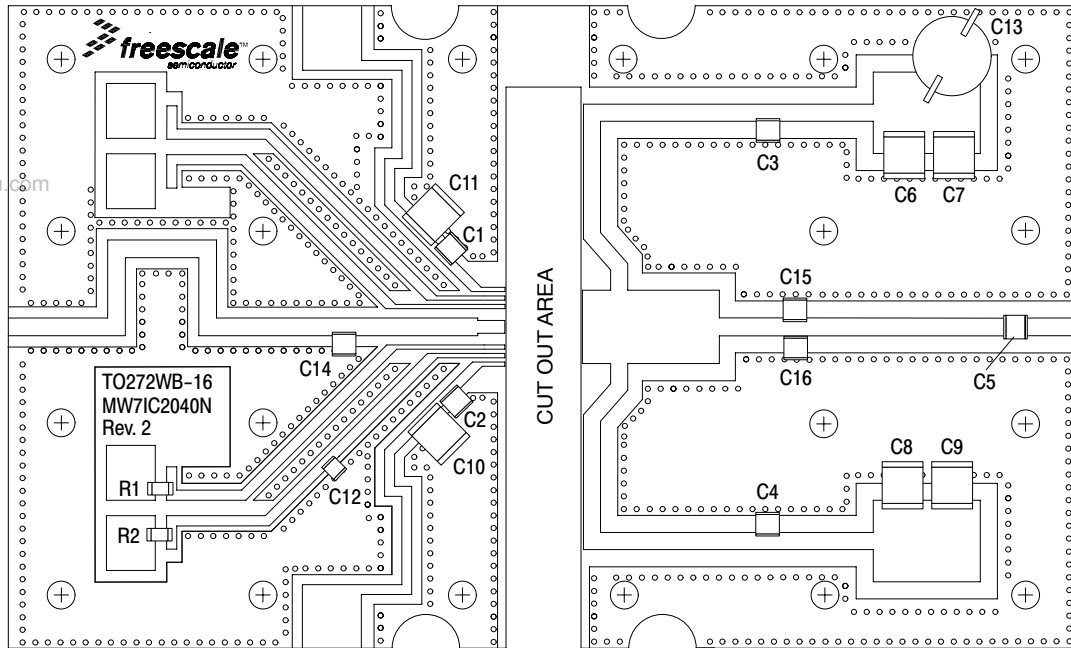
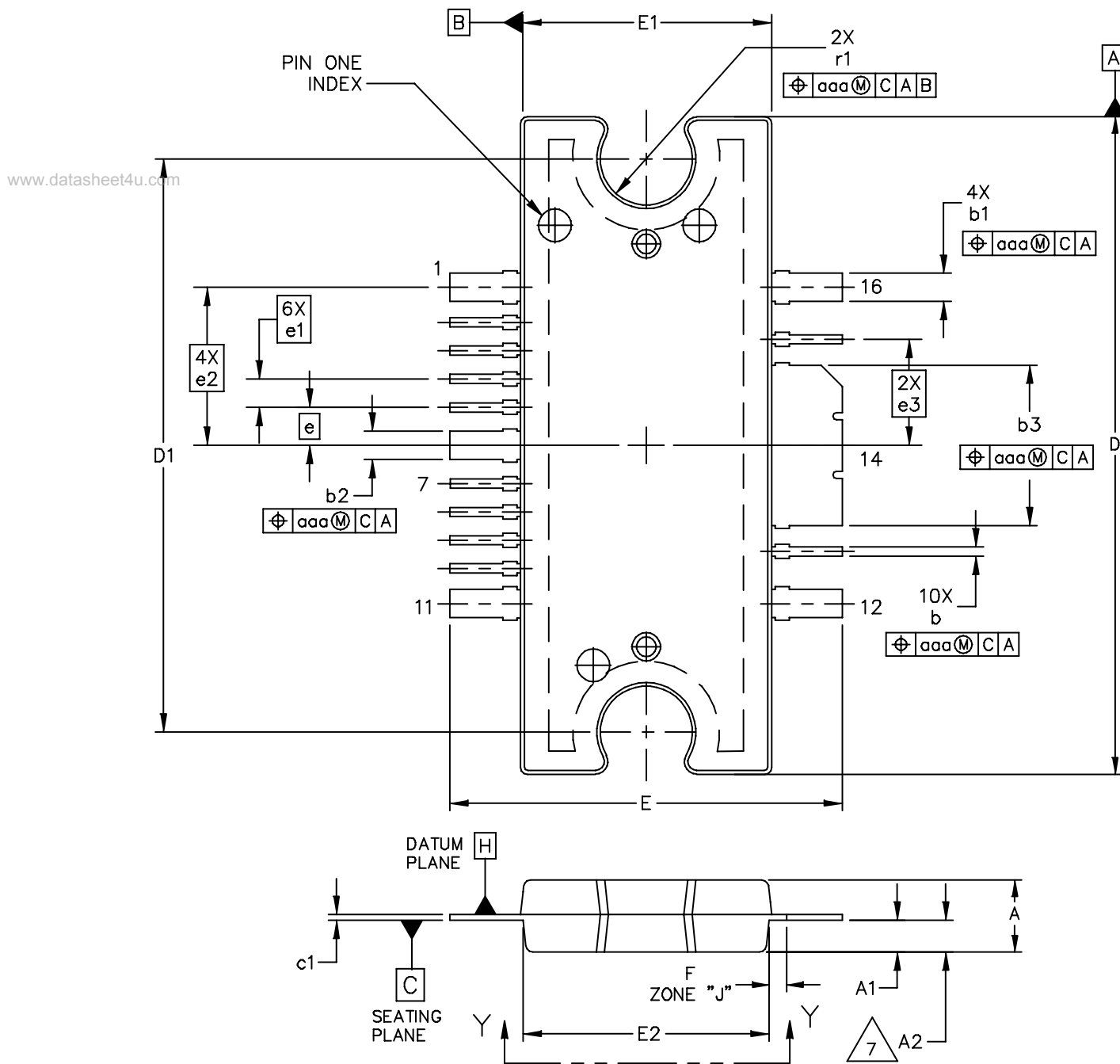
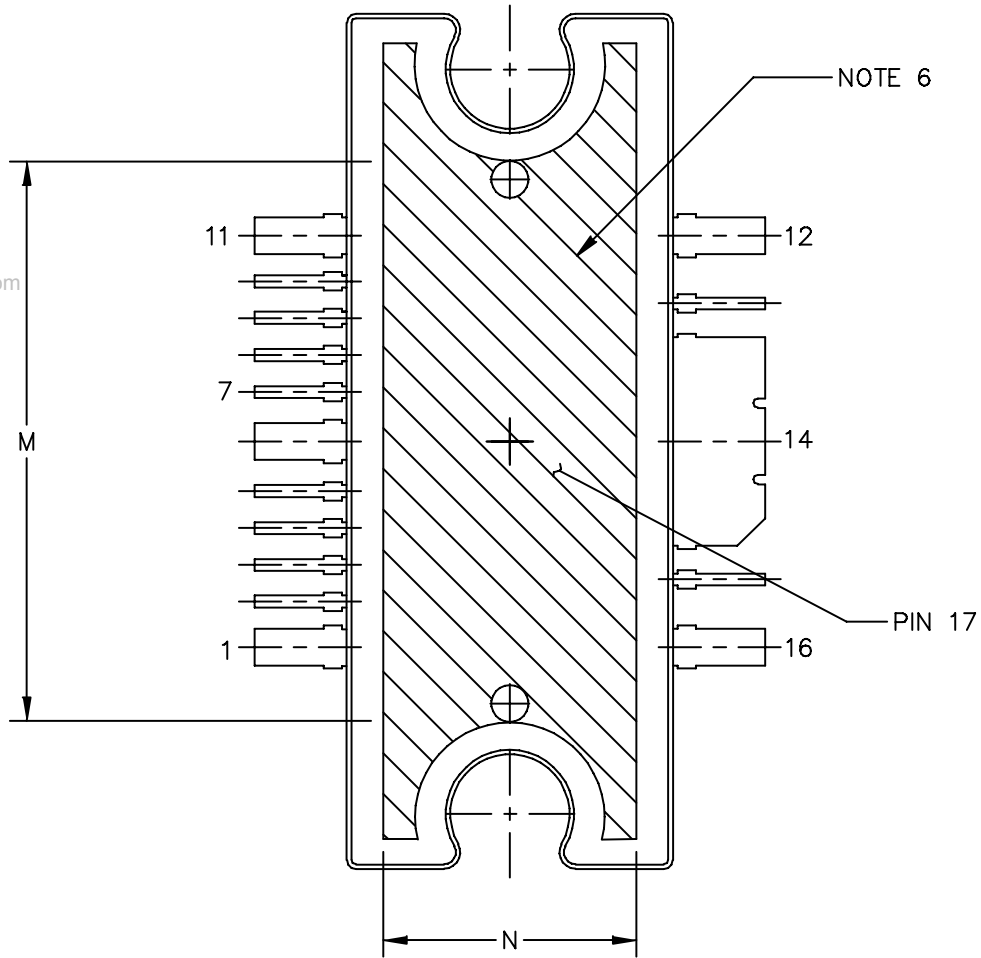


Figure 23. MW7IC2040NR1(GNR1)(NBR1) Test Circuit Component Layout — 1930-1990 MHz

PACKAGE DIMENSIONS



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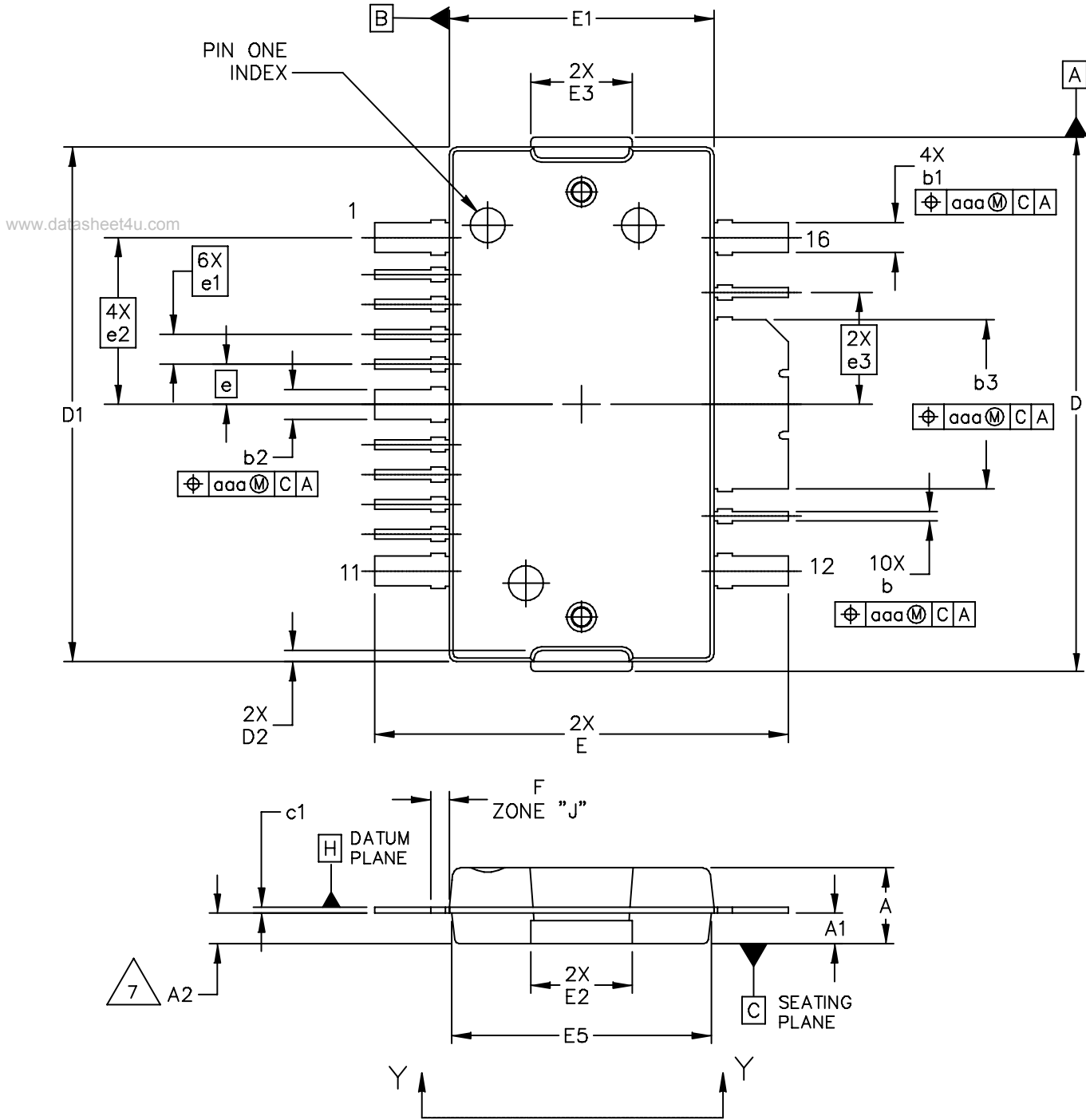
VIEW Y-Y

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	CASE NUMBER: 1329-09	23 AUG 2007	
	STANDARD: NON-JEDEC		

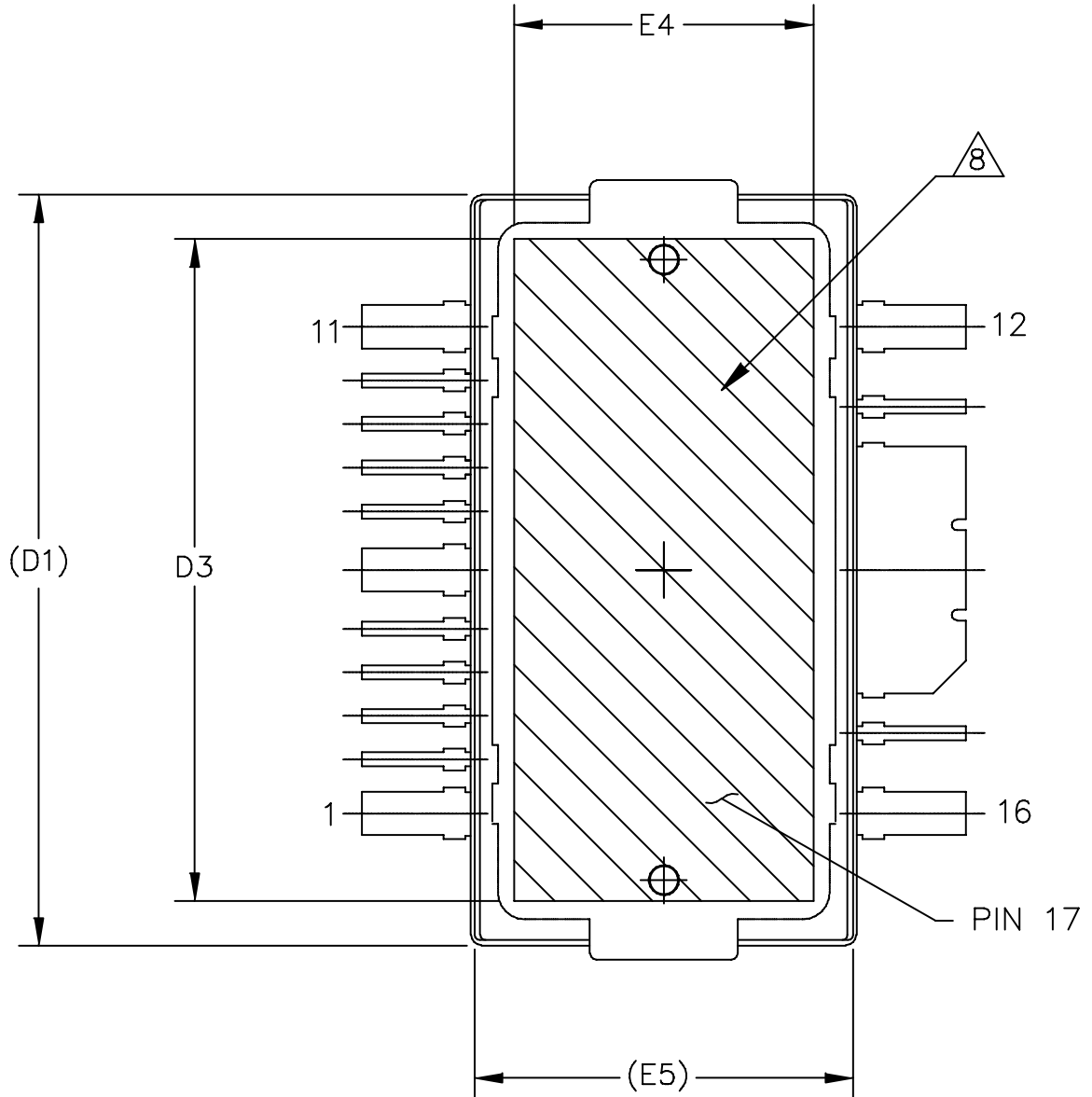
NOTES:

1. CONTROLLING DIMENSION: INCH
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3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.011	.017	0.28	0.43
A1	.038	.044	0.96	1.12	b1	.037	.043	0.94	1.09
A2	.040	.042	1.02	1.07	b2	.037	.043	0.94	1.09
D	.928	.932	23.57	23.67	b3	.225	.231	5.72	5.87
D1	.810 BSC		20.57 BSC		c1	.007	.011	.18	.28
E	.551	.559	14.00	14.20	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.346	.350	8.79	8.89	e2	.224 BSC		5.69 BSC	
F	.025 BSC		0.64 BSC		e3	.150 BSC		3.81 BSC	
M	.600	----	15.24	----	r1	.063	.068	1.6	1.73
N	.270	----	6.86	----	aaa	.004		.10	
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		CASE NUMBER: 1886-01	31 AUG 2007
		STANDARD: NON-JEDEC	



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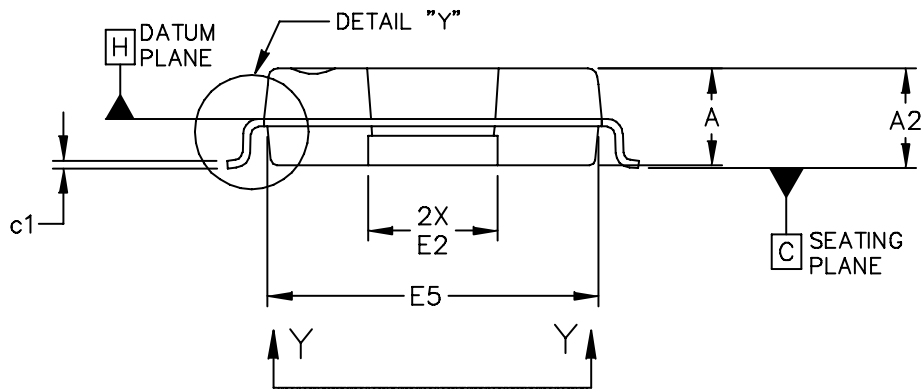
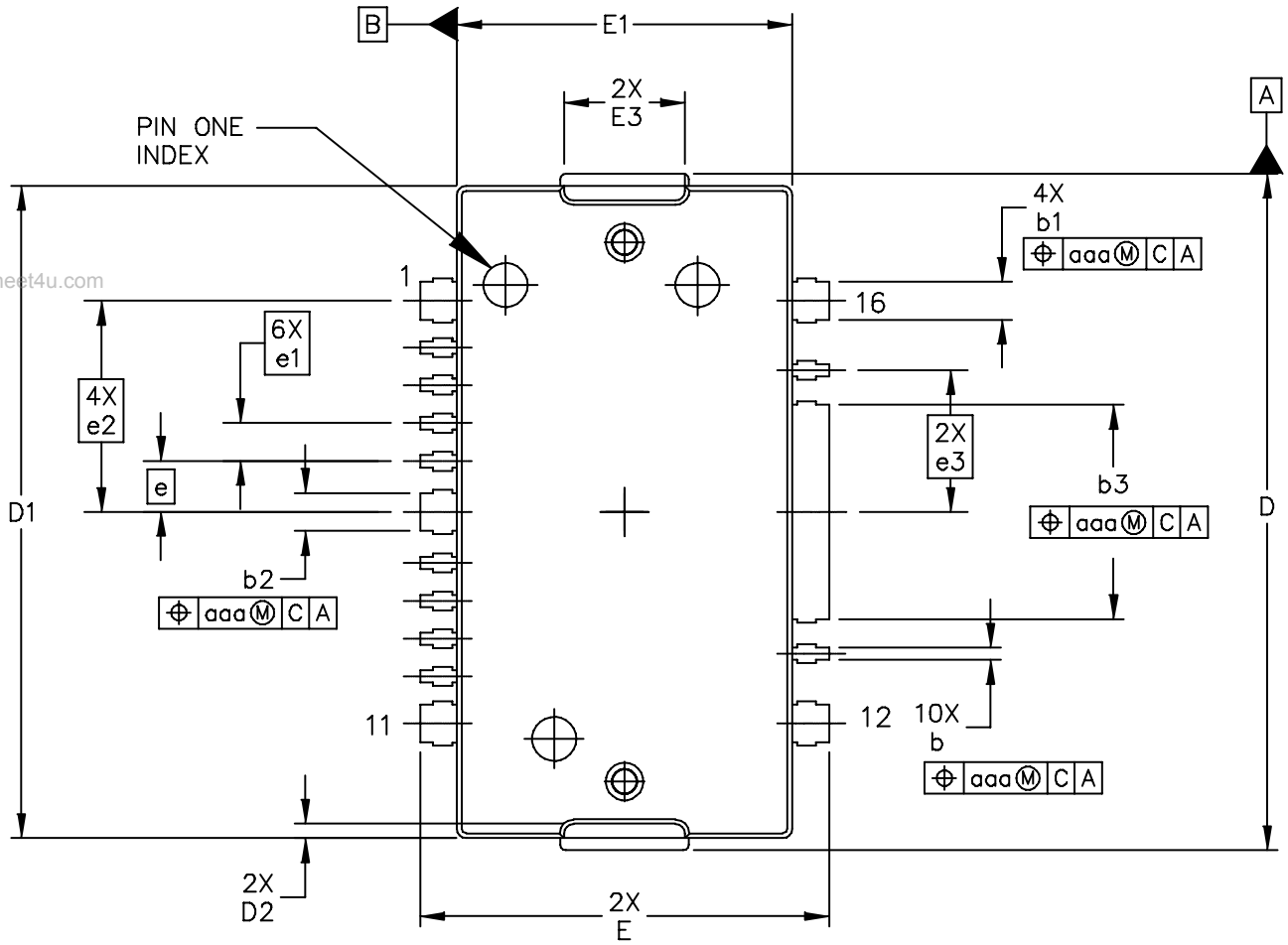
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	CASE NUMBER: 1886-01	31 AUG 2007	
	STANDARD: NON-JEDEC		

NOTES:

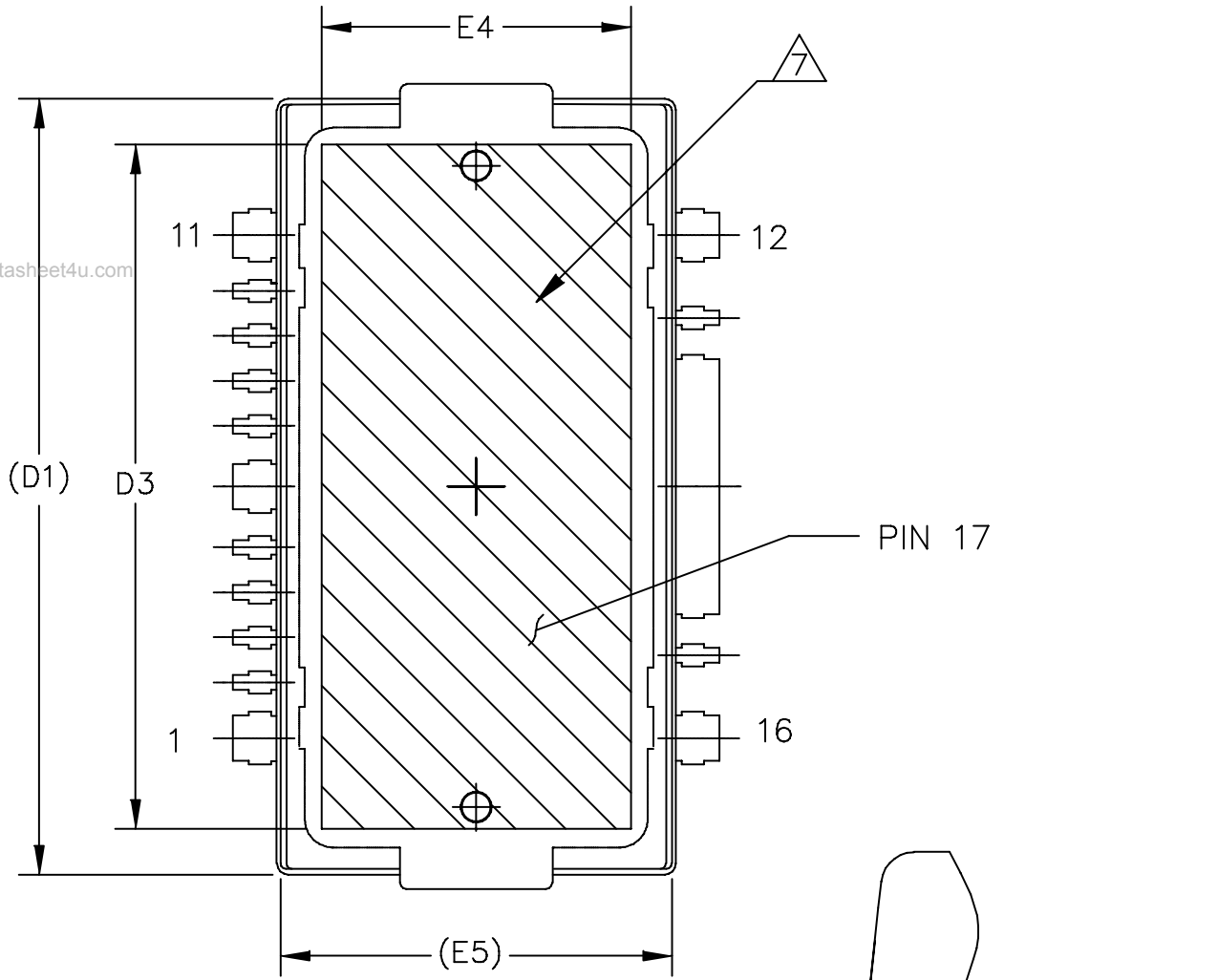
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2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
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5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.011	.017	0.28	0.43
A2	.040	.042	1.02	1.07	b1	.037	.043	0.94	1.09
D	.712	.720	18.08	18.29	b2	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b3	.225	.231	5.72	5.87
D2	.011	.019	0.28	0.48	c1	.007	.011	.18	.28
D3	.600	---	15.24	---	e	.054 BSC		1.37 BSC	
E	.551	.559	14	14.2	e1	.040 BSC		1.02 BSC	
E1	.353	.357	8.97	9.07	e2	.224 BSC		5.69 BSC	
E2	.132	.140	3.35	3.56	e3	.150 BSC		3.81 BSC	
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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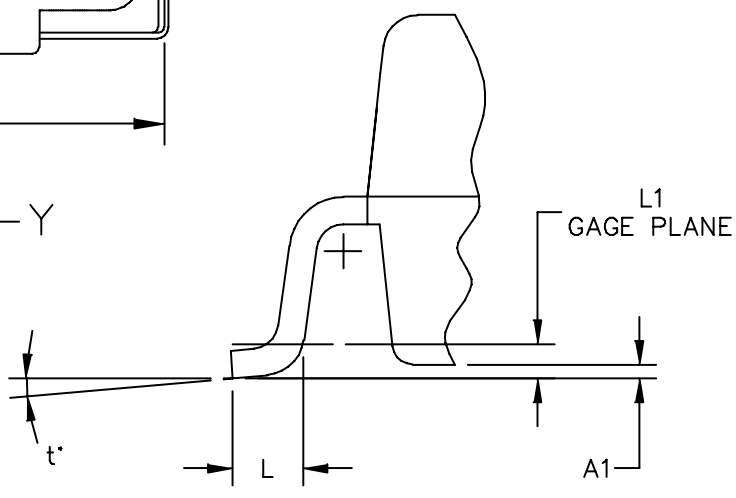




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VIEW Y-Y



DETAIL "Y"

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NOTES:

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4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b", "b1", "b2" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b", "b1", "b2" AND "b3" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. DATUM -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS EXPOSED AREA OF THE HEAT SLUG. HATCHED AREA SHOWN IS ON THE SAME PLANE.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.011	.017	0.28	0.43
D	.712	.720	18.08	18.29	b1	.037	.043	0.94	1.09
D1	.688	.692	17.48	17.58	b2	.037	.043	0.94	1.09
D2	.011	.019	0.28	0.48	b3	.225	.231	5.72	5.87
D3	.600	---	15.24	---	c1	.007	.011	0.18	0.28
E	.429	.437	10.9	11.1	e	.054 BSC		1.37 BSC	
E1	.353	.357	8.97	9.07	e1	.040 BSC		1.02 BSC	
E2	.132	.140	3.35	3.56	e2	.224 BSC		5.69 BSC	
E3	.124	.132	3.15	3.35	e3	.150 BSC		3.81 BSC	
E4	.270	---	6.86	---	t	2'	8'	2'	8'
E5	.346	.350	8.79	8.89	aaa	.004		0.10	
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					CASE NUMBER: 1887-01			31 AUG 2007	
					STANDARD: NON-JEDEC				

## PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Feb. 2009	<ul style="list-style-type: none"><li>• Initial Release of Data Sheet</li></ul>

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