



RF LDMOS Wideband Integrated Power Amplifiers

The MWE6IC9080N wideband integrated circuit is designed with on-chip matching that makes it usable from 865 to 960 MHz. This multi-stage structure is rated for 26 to 32 Volt operation and covers all typical cellular base station modulations.

- Typical GSM Performance: $V_{DD} = 28$ Volts, $I_{DQ1} = 230$ mA, $I_{DQ2} = 630$ mA, $P_{out} = 80$ Watts CW

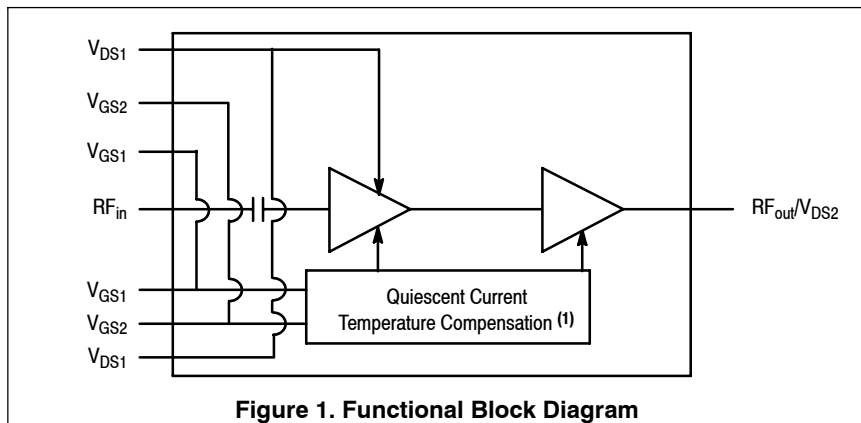
Frequency	G_{ps} (dB)	PAE (%)
920 MHz	29.0	49.7
940 MHz	28.8	51.6
960 MHz	28.5	52.3

- Capable of Handling 10:1 VSWR, @ 32 Vdc, 940 MHz, $P_{out} = 128$ Watts CW (3 dB Input Overdrive from Rated P_{out}), Designed for Enhanced Ruggedness
- Stable into a 5:1 VSWR. All Spurs Below -60 dBc @ 1 mW to 80 Watts CW P_{out}
- Typical P_{out} @ 1 dB Compression Point = 90 Watts CW
- Typical GSM EDGE Performance: $V_{DD} = 28$ Volts, $I_{DQ1} = 230$ mA, $I_{DQ2} = 630$ mA, $P_{out} = 35$ Watts Avg.

Frequency	G_{ps} (dB)	PAE (%)	SR1 @ 400 kHz (dBc)	SR2 @ 600 kHz (dBc)	EVM (% rms)
920 MHz	30.0	37.0	-62	-75	0.8
940 MHz	30.0	37.8	-62	-75	1.2
960 MHz	29.5	38.0	-62	-75	1.5

Features

- Characterized with Series Equivalent Large-Signal Impedance Parameters and Common Source Scattering Parameters
- On-Chip Matching (50 Ohm Input, DC Blocked)
- Integrated Quiescent Current Temperature Compensation with Enable/Disable Function (1)
- Integrated ESD Protection
- 225°C Capable Plastic Package
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

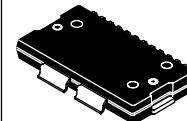
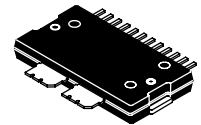


1. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

MWE6IC9080NR1
MWE6IC9080GNR1
MWE6IC9080NBR1

865-960 MHz, 80 W CW, 28 V
GSM, GSM EDGE
RF LDMOS WIDEBAND
INTEGRATED POWER AMPLIFIERS

CASE 1618-02
TO-270 WB-14
PLASTIC
MWE6IC9080NR1



CASE 1621-02
TO-270 WB-14 GULL
PLASTIC
MWE6IC9080GNR1

CASE 1617-02
TO-272 WB-14
PLASTIC
MWE6IC9080NBR1

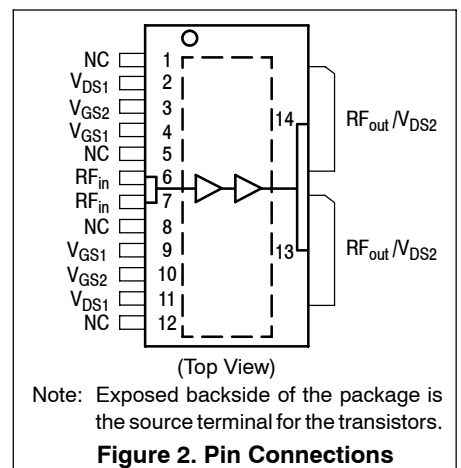
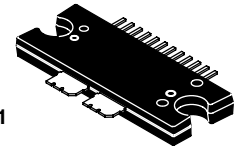


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-0.5, +66	Vdc
Gate-Source Voltage	V_{GS}	-0.5, +6	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature (1,2)	T_J	225	°C
Input Power	P_{in}	20.5	dBm

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$		°C/W
GSM Application (Case Temperature 80°C, $P_{out} = 80$ W CW, 940 MHz)	Stage 1, 28 Vdc, $I_{DQ1} = 230$ mA Stage 2, 28 Vdc, $I_{DQ2} = 630$ mA	3.5 0.52	
GSM EDGE Application (Case Temperature 80°C, $P_{out} = 40$ W CW, 940 MHz)	Stage 1, 28 Vdc, $I_{DQ1} = 230$ mA Stage 2, 28 Vdc, $I_{DQ2} = 630$ mA	3.6 0.54	

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1B (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	III (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 1 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 66$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	10	μA dc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	I_{DSS}	—	—	1	μA dc
Gate-Source Leakage Current ($V_{GS} = 1.5$ Vdc, $V_{DS} = 0$ Vdc)	I_{GSS}	—	—	1	μA dc
Stage 1 — On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10$ Vdc, $I_D = 33$ μA dc)	$V_{GS(th)}$	1.5	2	3.5	Vdc
Gate Quiescent Voltage ($V_{DS} = 28$ Vdc, $I_{DQ1} = 230$ mAdc)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28$ Vdc, $I_{DQ1} = 230$ mAdc, Measured in Functional Test)	$V_{GG(Q)}$	15	17	19	Vdc

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Stage 2 — Off Characteristics					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 66\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 1.5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

Stage 2 — On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 270\ \mu\text{Adc}$)	$V_{GS(th)}$	1.5	2	3.5	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_{DQ2} = 630\text{ mAdc}$)	$V_{GS(Q)}$	—	2.7	—	Vdc
Fixture Gate Quiescent Voltage ($V_{DD} = 28\text{ Vdc}$, $I_{DQ2} = 630\text{ mAdc}$, Measured in Functional Test)	$V_{GG(Q)}$	16.5	18.5	20.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	0.1	0.45	0.8	Vdc

Functional Tests ⁽¹⁾ (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $P_{out} = 80\text{ W CW}$, $I_{DQ1} = 230\text{ mA}$, $I_{DQ2} = 630\text{ mA}$, $f = 960\text{ MHz}$

Power Gain	G_{ps}	27.0	28.5	30.5	dB
Power Added Efficiency	PAE	48.0	52.3	—	%
Input Return Loss	IRL	—	-28	-10	dB

Typical Broadband Performance (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $P_{out} = 80\text{ W CW}$, $I_{DQ1} = 230\text{ mA}$, $I_{DQ2} = 630\text{ mA}$

Frequency	G_{ps} (dB)	PAE (%)	IRL (dB)
920 MHz	29.0	49.7	-24
940 MHz	28.8	51.6	-28
960 MHz	28.5	52.3	-28

Typical Performances (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ1} = 230\text{ mA}$, $I_{DQ2} = 630\text{ mA}$, 920-960 MHz Bandwidth

Characteristic	Symbol	Min	Typ	Max	Unit
P_{out} @ 1 dB Compression Point, CW	P_{1dB}	—	90	—	W
IMD Symmetry @ 100 W PEP, P_{out} where IMD Third Order Intermodulation $\cong 30\text{ dBc}$ (Delta IMD Third Order Intermodulation between Upper and Lower Sidebands $> 2\text{ dB}$)	IMD_{sym}	—	28	—	MHz
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	30	—	MHz
Quiescent Current Accuracy over Temperature ⁽²⁾ with 4.12 k Ω Gate Feed Resistors (-30 to 85 $^\circ\text{C}$)	ΔI_{QT}	—	2.6 2.6	—	%
Gain Flatness in 40 MHz Bandwidth @ $P_{out} = 80\text{ W CW}$	G_F	—	0.7	—	dB
Gain Variation over Temperature (-30 $^\circ\text{C}$ to +85 $^\circ\text{C}$)	ΔG	—	0.039	—	dB/ $^\circ\text{C}$
Output Power Variation over Temperature (-30 $^\circ\text{C}$ to +85 $^\circ\text{C}$)	ΔP_{1dB}	—	0.008	—	dBm/ $^\circ\text{C}$

1. Part internally matched both on input and output.

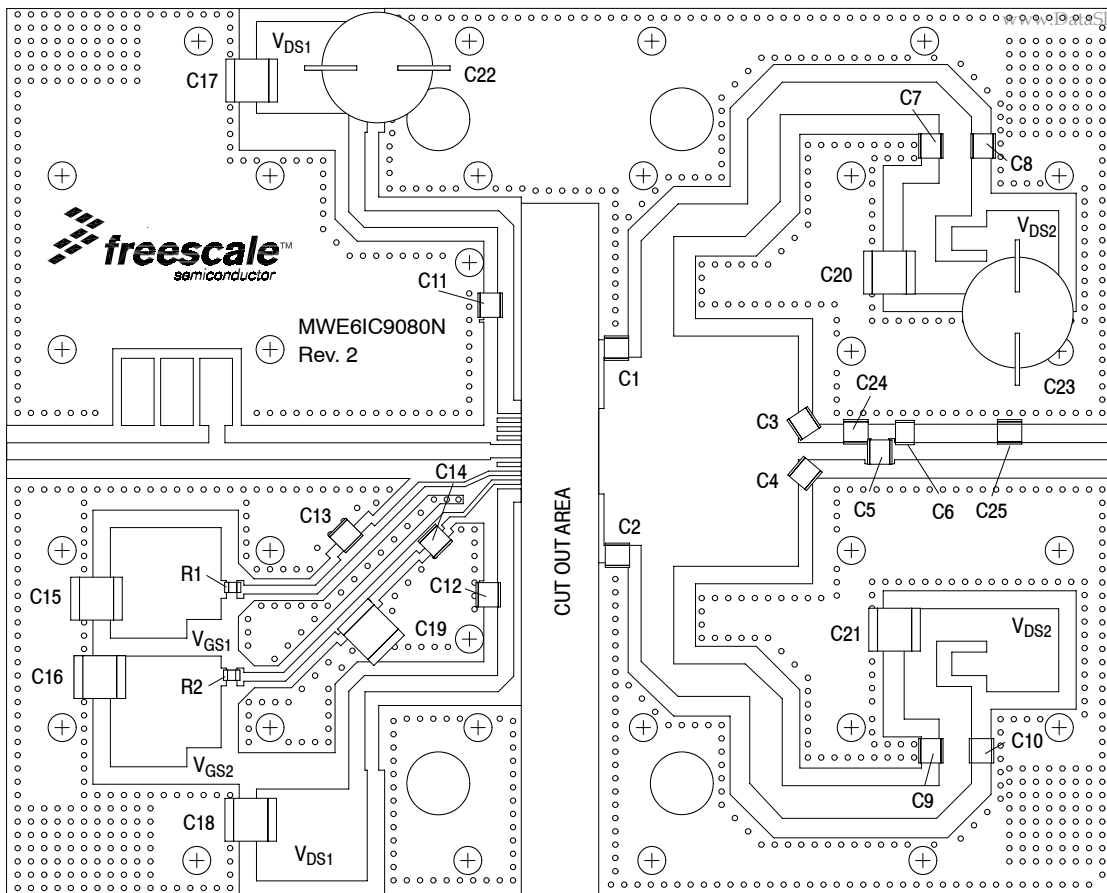
2. Refer to AN1977, *Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family* and to AN1987, *Quiescent Current Control for the RF Integrated Circuit Device Family*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1977 or AN1987.

(continued)

Table 5. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted) (continued)

Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $P_{out} = 35\text{ W Avg.}$, $I_{DQ1} = 230\text{ mA}$, $I_{DQ2} = 630\text{ mA}$, 920-960 MHz EDGE Modulation

Frequency	G_{ps} (dB)	PAE (%)	SR1 @ 400 kHz (dBc)	SR2 @ 600 kHz (dBc)	EVM (% rms)
920 MHz	30.0	37.0	-62	-75	0.8
940 MHz	30.0	37.8	-62	-75	1.2
960 MHz	29.5	38.0	-62	-75	1.5



*C6 is mounted vertically.

Figure 3. MWE6IC9080NR1(GNR1)(NBR1) Test Circuit Component Layout

Table 6. MWE6IC9080NR1(GNR1)(NBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	6.8 pF Chip Capacitors	ATC100B6R8CT500XT	ATC
C3, C4	4.7 pF Chip Capacitors	ATC100B4R7CT500XT	ATC
C5, C7, C8, C9, C10, C11, C12, C13, C14	33 pF Chip Capacitors	ATC100B330JT500XT	ATC
C6	4.3 pF Chip Capacitor	ATC100B4R3CT500XT	ATC
C15, C16, C17, C18, C19, C20, C21	10 μ F, 50 V Chip Capacitors	GRM55DR61H106KA88L	Murata
C22, C23	470 μ F, 63 V Electrolytic Capacitors, Radial	MCGPR63V477M13X26-RH	Multicomp
C24	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
C25	1.0 pF Chip Capacitor	ATC100B1R0BT500XT	ATC
R1, R2	4.12 K Ω , 1/4 W Chip Resistors	CRCW12064K12FKEA	Vishay
PCB	0.030", $\epsilon_r = 2.8$	IS680-280	Isola

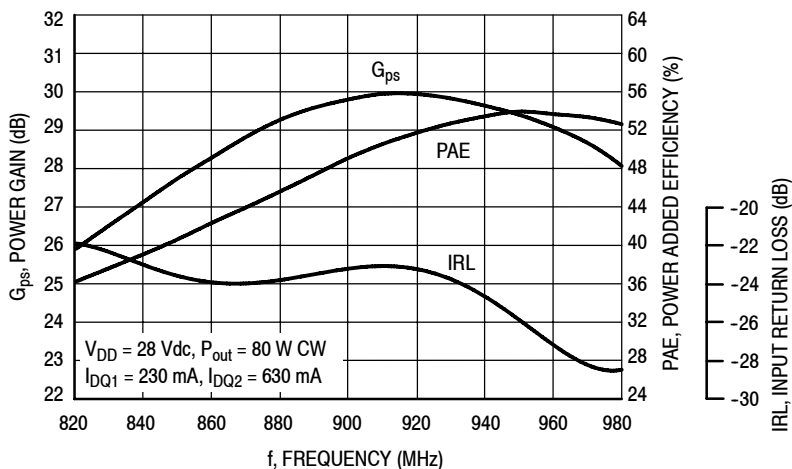


Figure 4. Power Gain, Input Return Loss and Power Added Efficiency versus Frequency @ $P_{out} = 80$ Watts CW

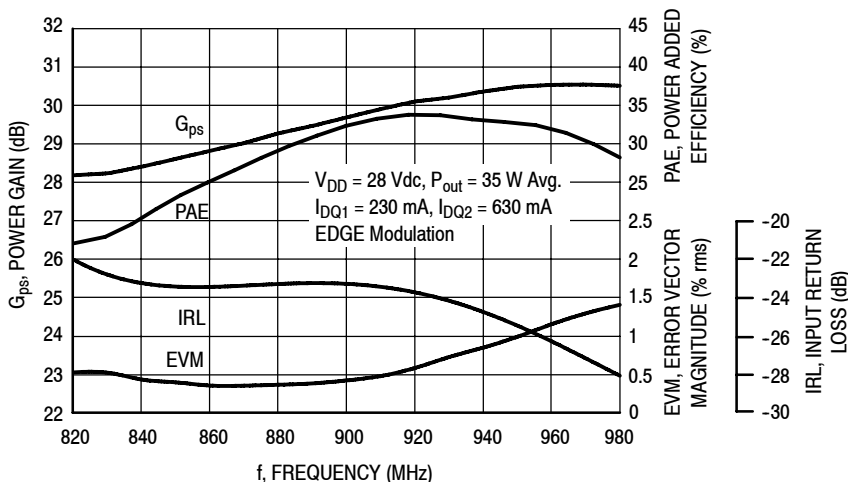


Figure 5. Power Gain, Input Return Loss, EVM and Power Added Efficiency versus Frequency @ $P_{out} = 35$ Watts Avg.

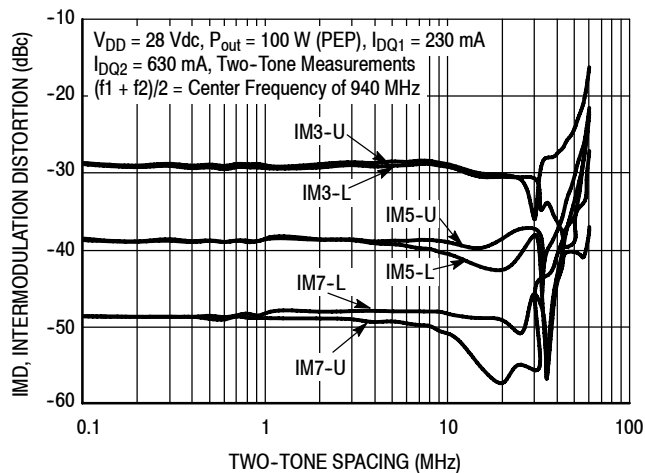


Figure 6. Intermodulation Distortion Products versus Two-Tone Spacing

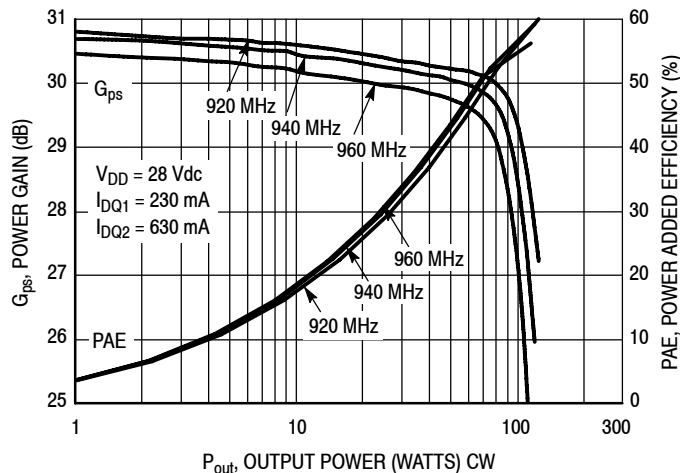


Figure 7. Power Gain and Power Added Efficiency versus Output Power

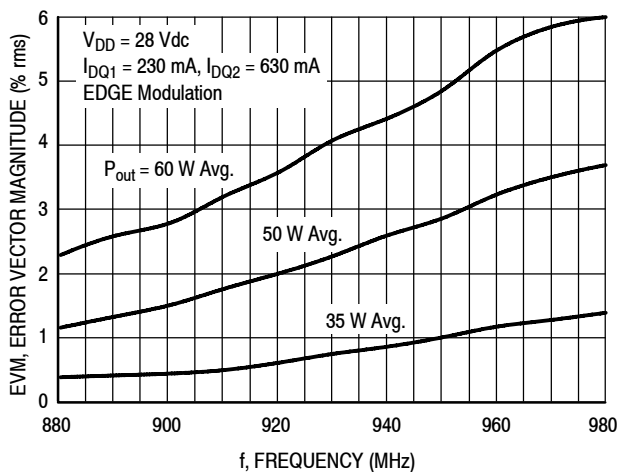


Figure 8. EVM versus Frequency

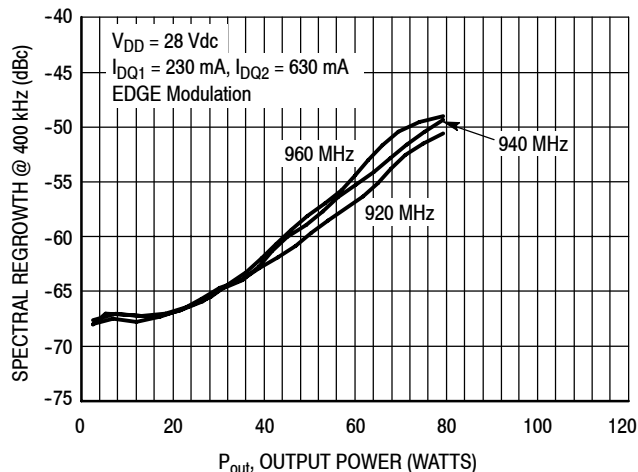


Figure 9. Spectral Regrowth at 400 kHz versus Output Power

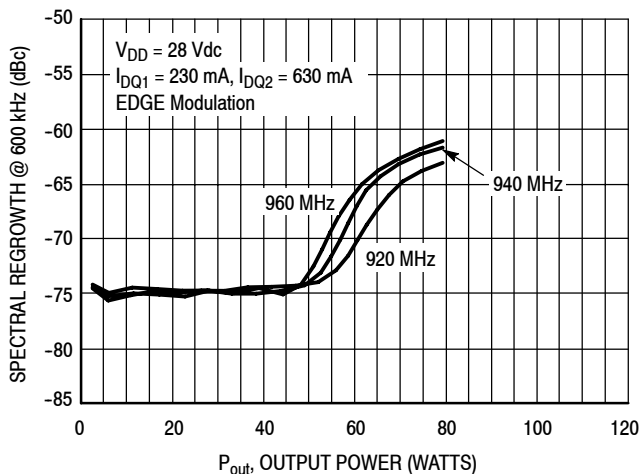


Figure 10. Spectral Regrowth at 600 kHz versus Output Power

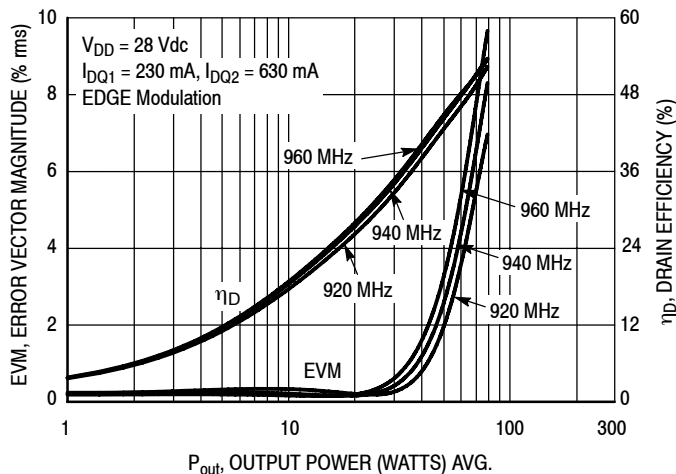


Figure 11. EVM and Drain Efficiency versus Output Power

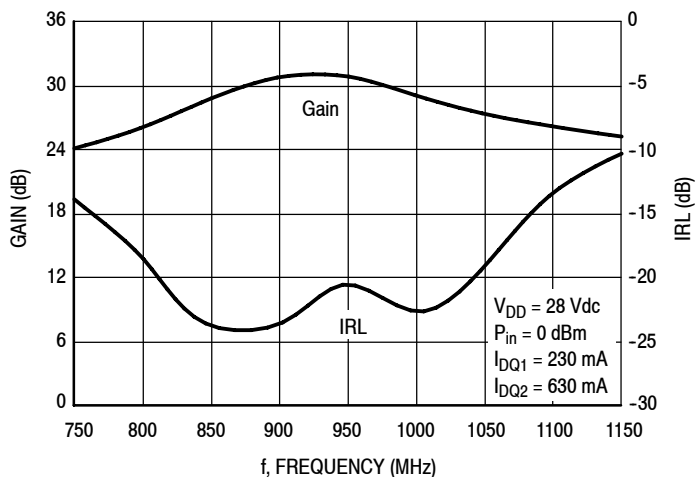


Figure 12. Broadband Frequency Response

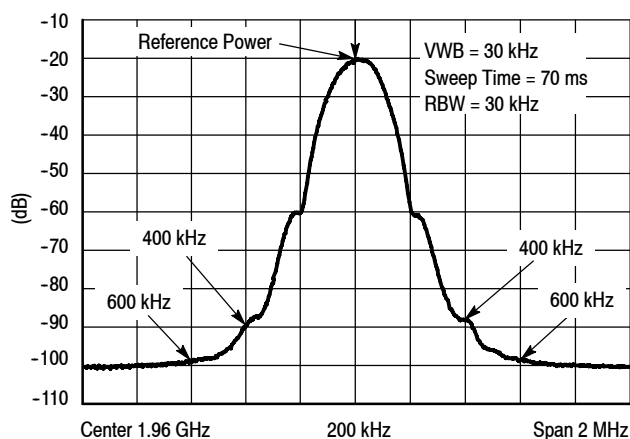


Figure 13. EDGE Spectrum

$V_{DD} = 28 \text{ Vdc}$, $I_{DQ1} = 230 \text{ mA}$, $I_{DQ2} = 630 \text{ mA}$, $P_{out} = 80 \text{ W CW}$

f MHz	Z_{in} Ω	Z_{load} Ω
820	56.91 - j7.34	1.22 - j0.47
840	52.38 - j6.36	1.26 - j0.26
860	49.30 - j5.92	1.35 - j0.58
880	45.68 - j4.07	1.44 + j0.14
900	44.22 - j2.13	1.54 + j0.33
920	42.43 - j0.62	1.62 + j0.49
940	41.50 + j1.76	1.74 + j0.66
960	42.19 + j3.25	1.91 + j0.82
980	43.07 + j3.14	2.08 + j0.94

Z_{in} = Device input impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

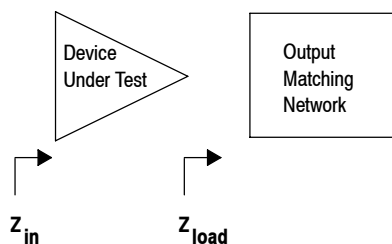
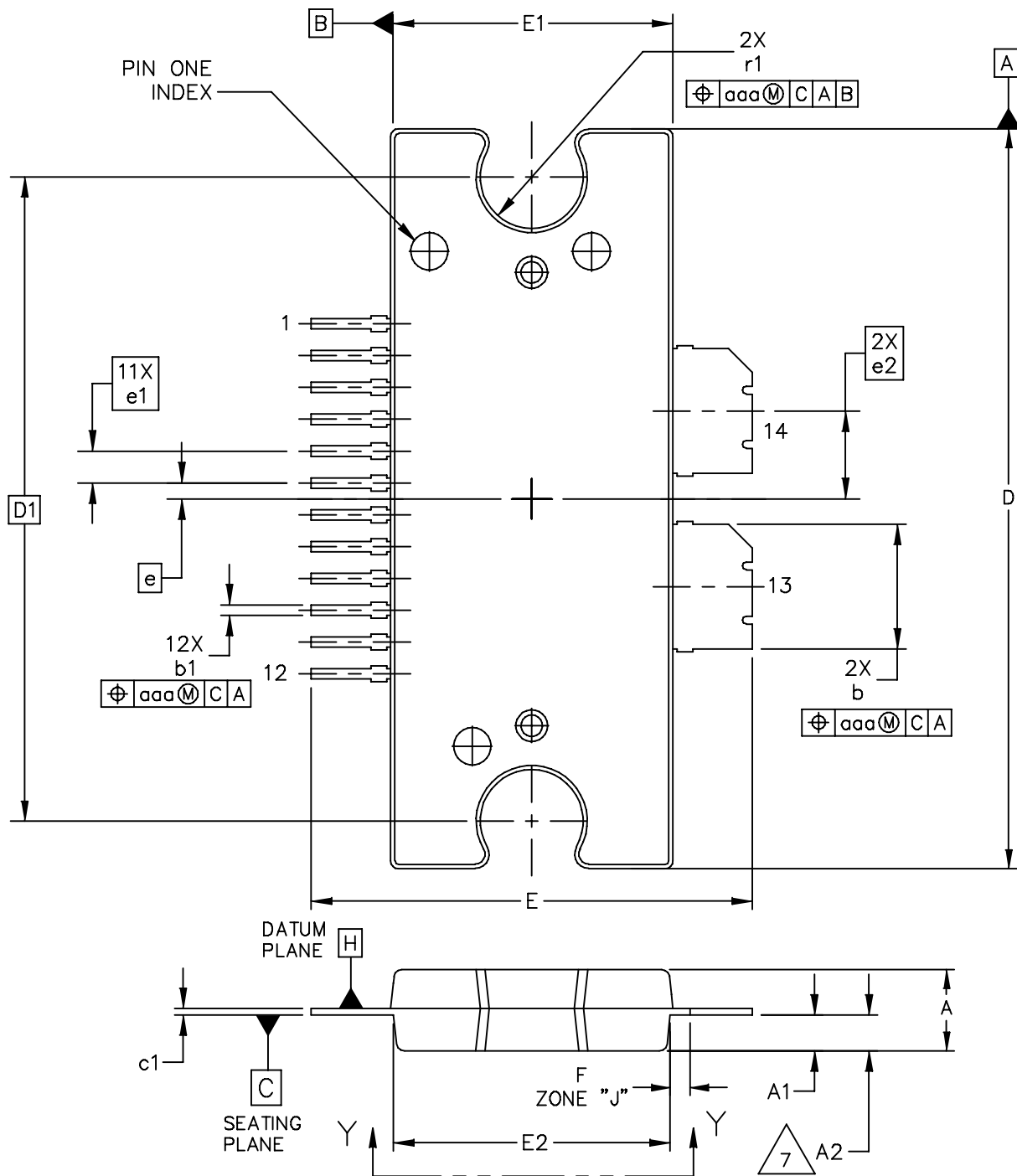


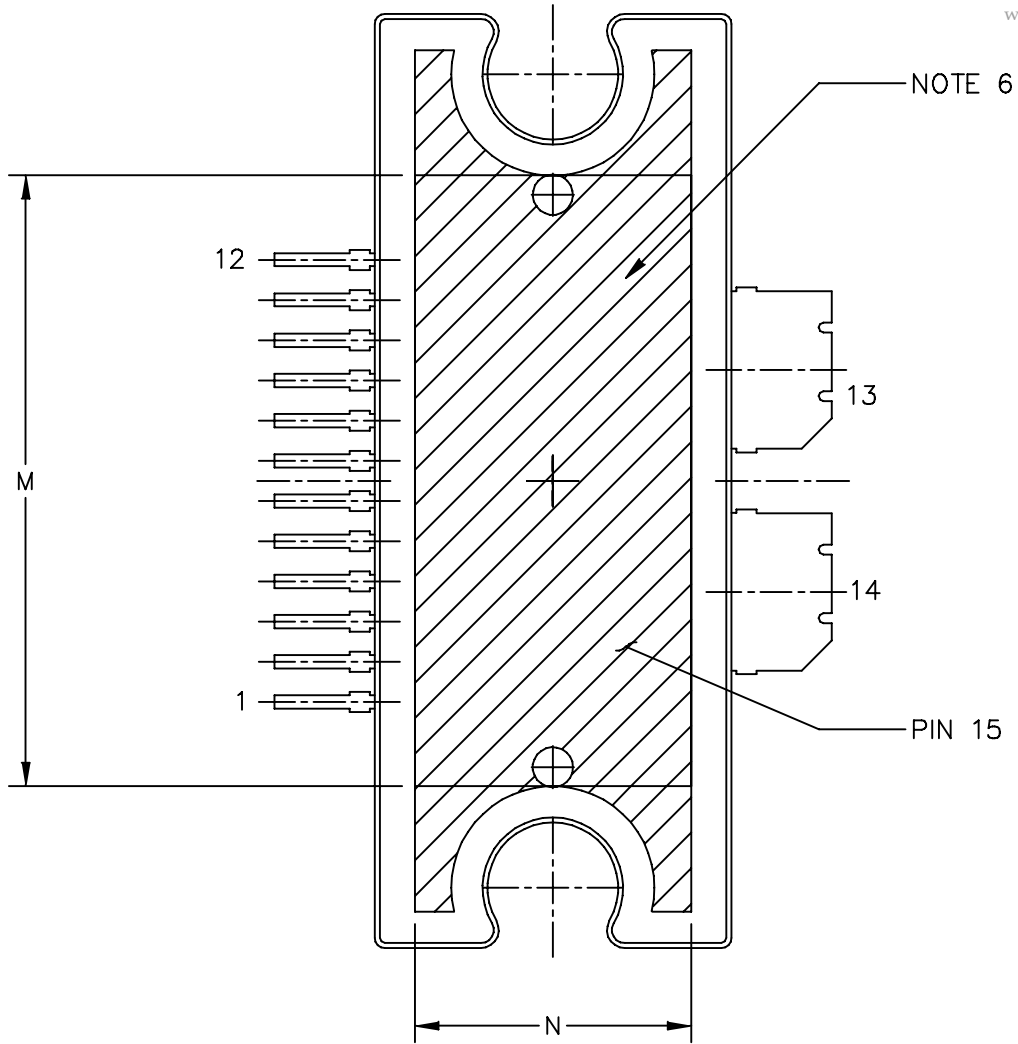
Figure 14. Series Equivalent Input and Load Impedance

PACKAGE DIMENSIONS



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	<p>CASE NUMBER: 1617-02</p>		<p>27 JUN 2007</p>
	<p>STANDARD: NON-JEDEC</p>		

MWE6IC9080NR1 MWE6IC9080GNR1 MWE6IC9080NBR1



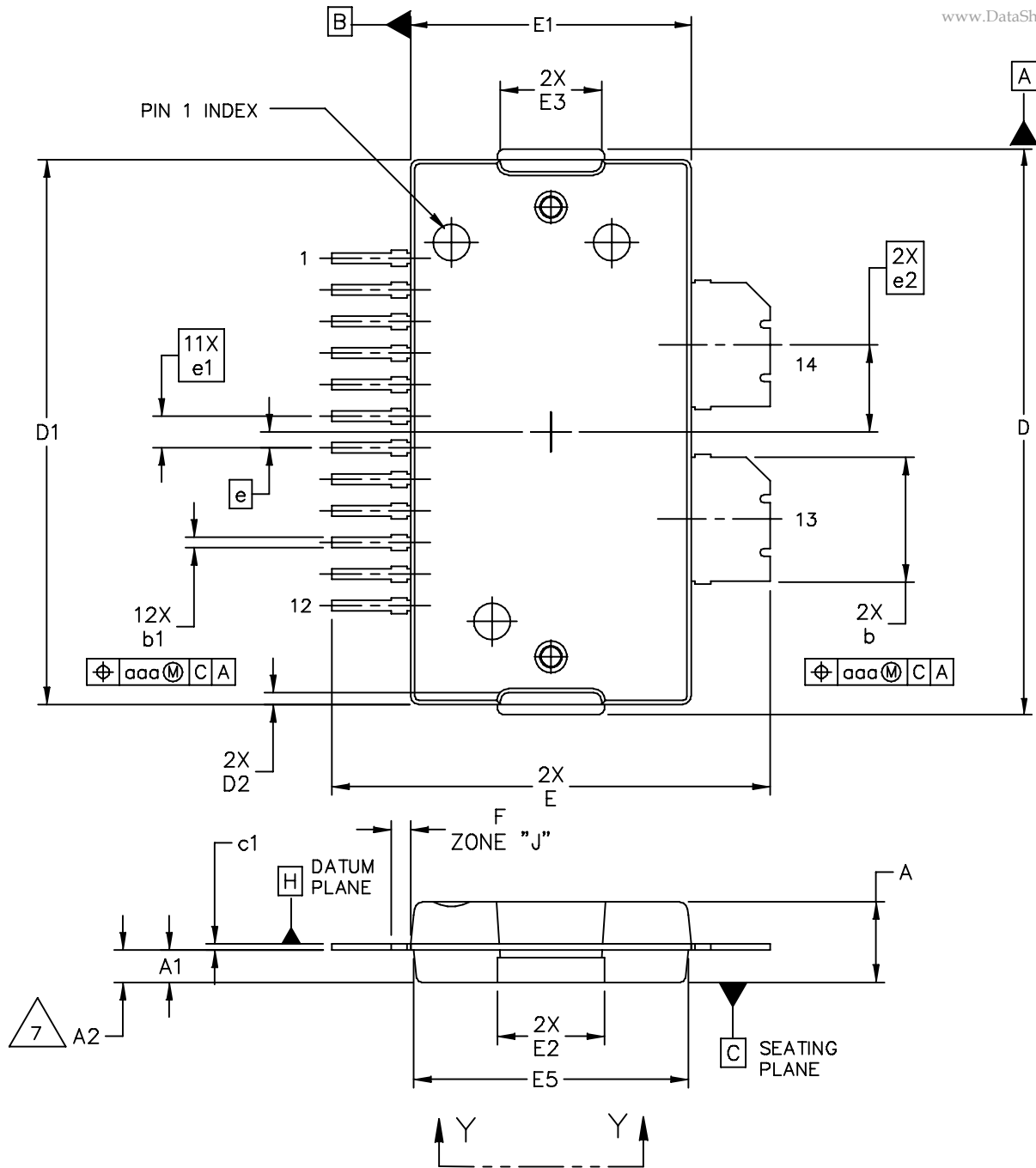
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	STANDARD: NON-JEDEC		

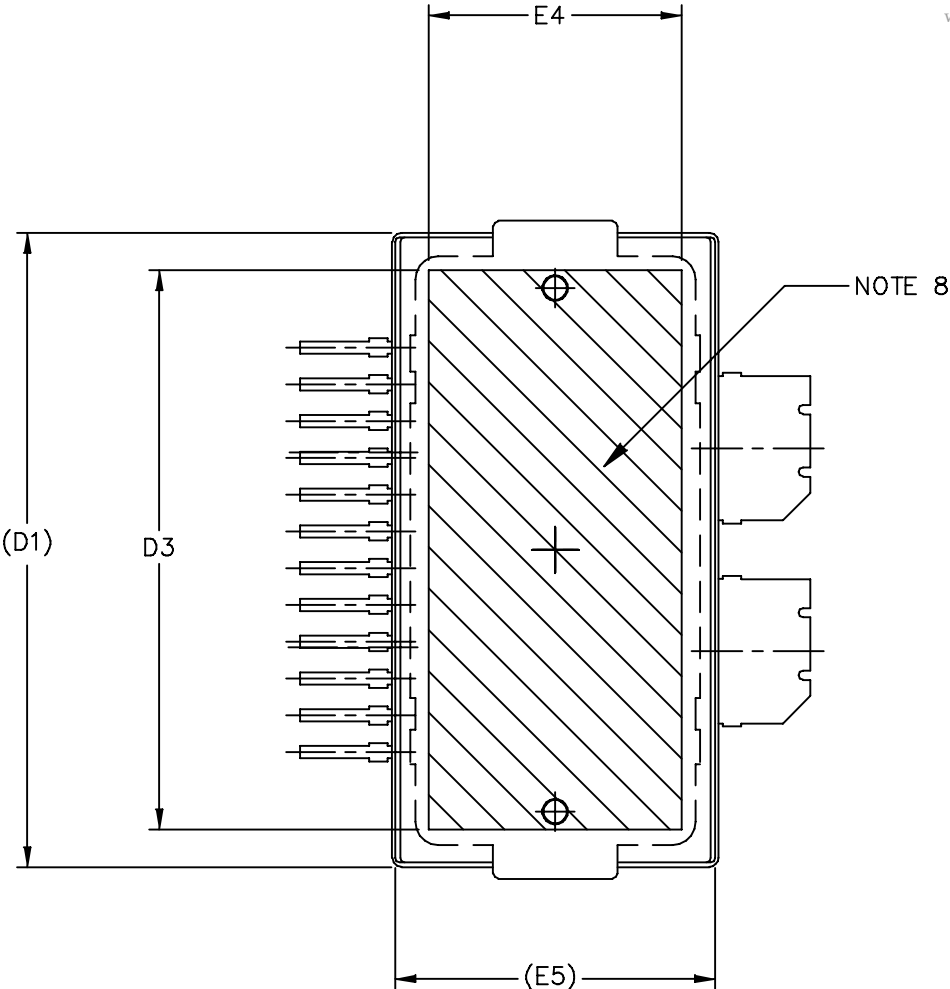
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 (0.15) PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 (0.13) TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
7. DIM A2 APPLIES WITHIN ZONE "J" ONLY.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	b	.154	.160	3.91	4.06
A1	.039	.043	0.99	1.09	b1	.010	.016	0.25	0.41
A2	.040	.042	1.02	1.07	c1	.007	.011	0.18	0.28
D	.928	.932	23.57	23.67	e	.020 BSC		0.51 BSC	
D1	.810 BSC		20.57 BSC		e1	.040 BSC		1.02 BSC	
E	.551	.559	14.00	14.20	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	r1	.063	.068	1.6	1.73
E2	.346	.350	8.79	8.89	aaa	.004		0.10	
F	.025 BSC		0.64 BSC						
M	.600	----	15.24	----					
N	.270	----	6.86	----					
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					STANDARD: NON-JEDEC				



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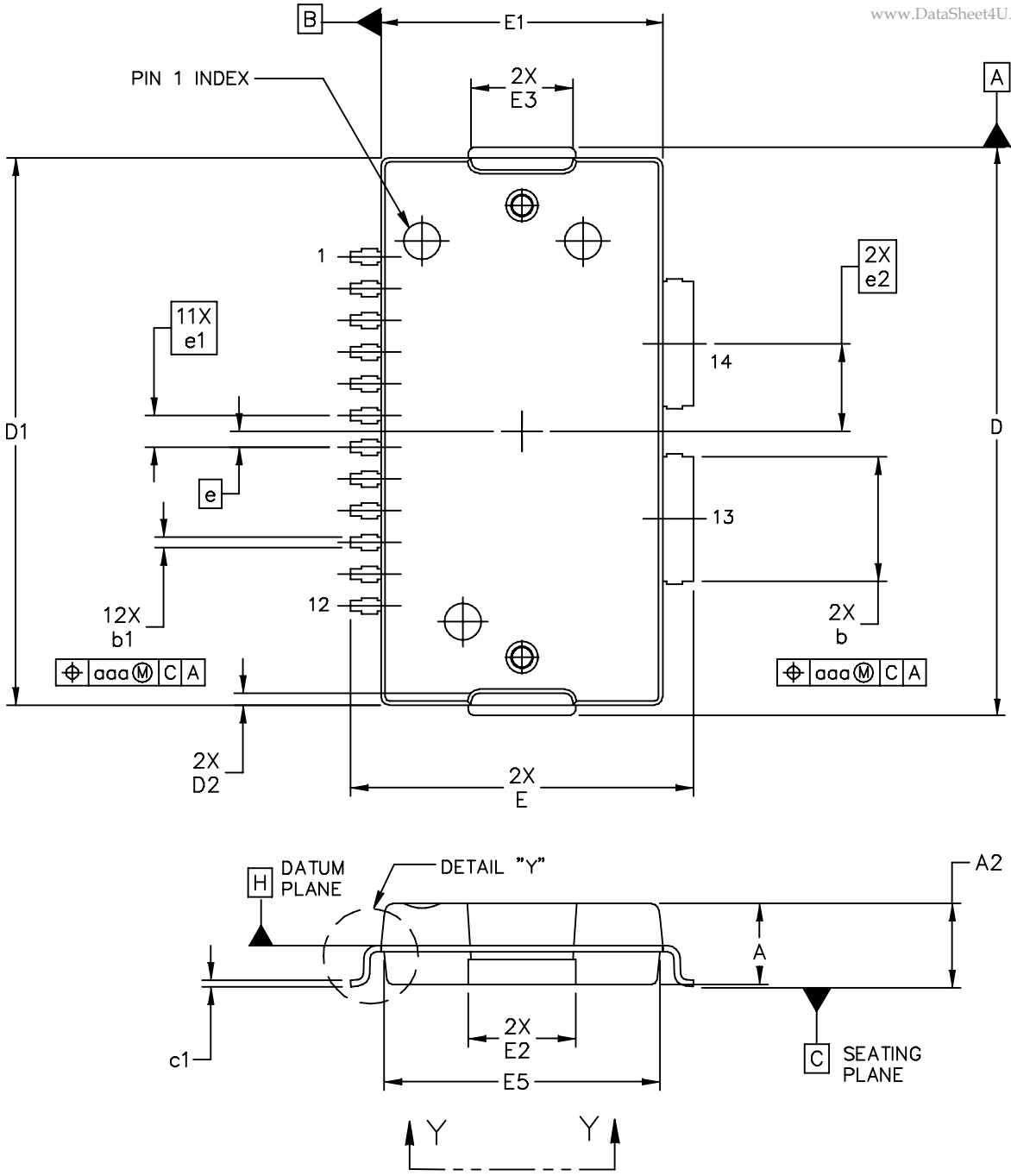
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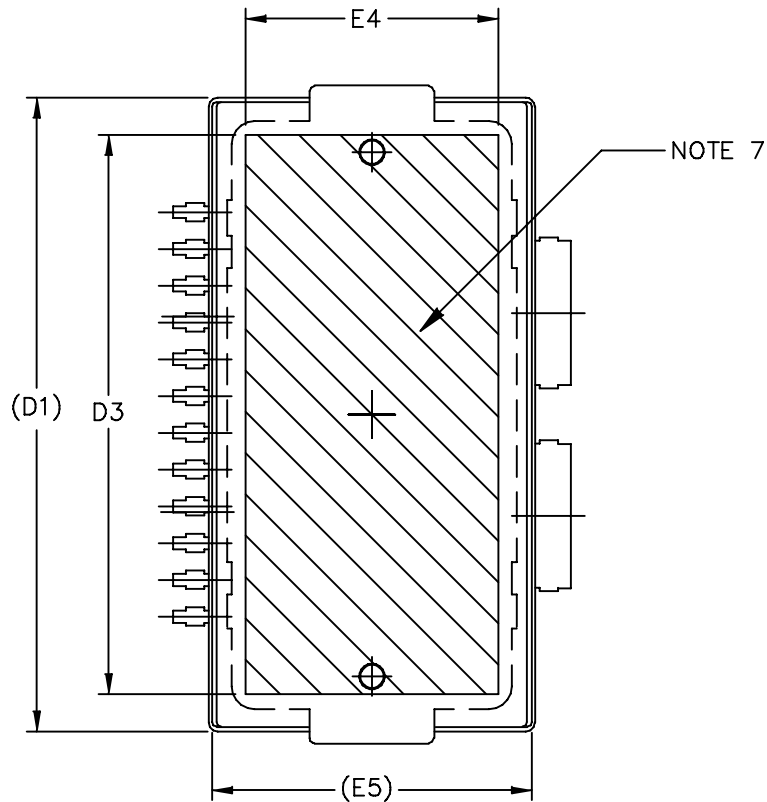
NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

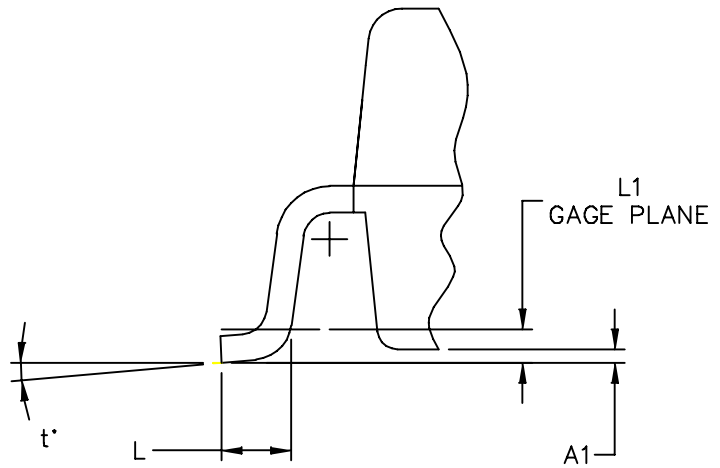
DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	F	.025 BSC		0.64 BSC	
A1	.039	.043	0.99	1.09	b	.154	.160	3.91	4.06
A2	.040	.042	1.02	1.07	b1	.010	.016	0.25	0.41
D	.712	.720	18.08	18.29	c1	.007	.011	.18	.28
D1	.688	.692	17.48	17.58	e	.020 BSC		0.51 BSC	
D2	.011	.019	0.28	0.48	e1	.040 BSC		1.02 BSC	
D3	.600	---	15.24	---	e2	.1105 BSC		2.807 BSC	
E	.551	.559	14	14.2					
E1	.353	.357	8.97	9.07	aaa	.004		.10	
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35					
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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TITLE: TO-270 WIDE BODY 14 LEAD					DOCUMENT NO: 98ASA10650D			REV: A	
					CASE NUMBER: 1618-02			19 JUN 2007	
					STANDARD: NON-JEDEC				



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	CASE NUMBER: 1621-02	19 JUN 2007	
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VIEW Y-Y



DETAIL "Y"

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	CASE NUMBER: 1621-02		19 JUN 2007
	STANDARD: NON-JEDEC		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b" AND "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b" AND "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64	L	.018	.024	0.46	0.61
A1	.001	.004	0.02	0.10	L1	.010 BSC		0.25 BSC	
A2	.099	.110	2.51	2.79	b	.154	.160	3.91	4.06
D	.712	.720	18.08	18.29	b1	.010	.016	0.25	0.41
D1	.688	.692	17.48	17.58	c1	.007	.011	.18	.28
D2	.011	.019	0.28	0.48	e	.020 BSC		0.51 BSC	
D3	.600	---	15.24	---	e1	.040 BSC		1.02 BSC	
E	.429	.437	10.9	11.1	e2	.1105 BSC		2.807 BSC	
E1	.353	.357	8.97	9.07	t	2°	8°	2°	8°
E2	.132	.140	3.35	3.56					
E3	.124	.132	3.15	3.35	aaa	.004		.10	
E4	.270	---	6.86	---					
E5	.346	.350	8.79	8.89					
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Refer to the following documents to aid your design process.

Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN1977: Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family
- AN1987: Quiescent Current Control for the RF Integrated Circuit Device Family
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages
- AN3789: Clamping of High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTF Calculator
- RF High Power Model
- .s2p File

For Software, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2010	• Initial Release of Data Sheet

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