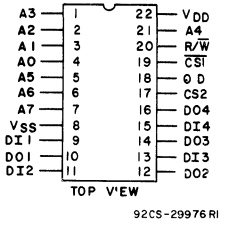
MWS5101



TERMINAL ASSIGNMENT

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- *Industry standard pinout*
- *Very low operating current-8 mA at V_{DD} = 5 V and cycle time = 1 μs*
- *Two Chip-Select inputs-simple memory expansion*
- *Memory retention for standby battery voltage of 2 V min*
- *Output-Disable for common I/O systems*
- *3-state data output for bus-oriented systems*
- *Separate data inputs and outputs*

The RCA-MWS5101 is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by $\overline{CS}1$ and/or CS2.

The high noise immunity of the CMOS technology is preserved in this design. For TTL interfacing at 5-V operation, excellent system noise margin is preserved by using an external pull-up resistor at each input.

For applications requiring wider temperature and operating voltage ranges, the mechanically and functionally equivalent static RAM, RCA-CDP1822, may be used

The MWS5101 types are supplied in 22-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 $\overline{CS}1$	Chip Select 2 CS2	Output Disable OD	Read/Write R/$\overline{W}$	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

File Number **1106**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (V_{DD})
(All voltage referenced to V_{SS} terminal) .. .. −0.5 to −7 V
INPUT VOLTAGE RANGE, ALL INPUTS.... ....−0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = −40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E)..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = −55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPE D .....−55 to +125° C
PACKAGE TYPE E .....−40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) .....−65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1 59 ± 0 79 mm) from case for 10 s max ..... +265° C

OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS ALL TYPES		UNITS
	Min.	Max.	
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%.

CHARACTERISTIC		TEST CONDITIONS V_O (V)	TEST CONDITIONS V_{IN} (V)	LIMITS MWS5101D MWS5101E Min.	LIMITS Typ.●	LIMITS Max.	UNITS
Quiescent Device Current, I_{DD}	L2 Types	–	0,5	–	25	50	μA
	L3 Types	–	0,5	–	100	200	
Output Voltage: Low-Level,	V_{OL}	–	0,5	–	0	0.1	V
High-Level,	V_{OH}	–	0,5	4.9	5	–	
Input Low Voltage,	V_{IL}	–	–	–	–	1.5	
Input High Voltage,	V_{IH}	–	–	3.5	–	–	
Output Low (Sink) Current,	I_{OL}	0.4	0,5	2	4	–	mA
Output High (Source) Current,	I_{OH}	4.6	0,5	−1	−2	–	
Input Current,	I_{IN}	–	0,5	–	–	±5	μA
3-State Output Leakage Current, I_{OUT}	L2 Types	0,5	0,5	–	–	±5	
	L3 Types	0,5	0,5	–	–	±5	
Operating Current,	I_{DD1}#	–	0,5	–	4	8	mA
Input Capacitance,	C_{IN}	–	–	–	5	7.5	pF
Output Capacitance,	C_{OUT}	–	–	–	10	15	

● Typical values are for T_A = 25°C and nominal V_{DD}.

Outputs open-circuited, cycle time=1 μs.

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DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		LIMITS MWS5101D, MWS5101E						UNITS
		L2 Types			L3 Types			
		Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Read Cycle Times (Fig. 1)								
Read Cycle	t_{RC}	250	–	–	350	–	–	ns
Access from Address	t_{AA}	–	150	250	–	200	350	ns
Output Valid from $\overline{\text{Chip-Select 1}}$	t_{DOA1}	–	150	250	–	200	350	ns
Output Valid from Chip-Select 2	t_{DOA2}	–	150	250	–	200	350	ns
Output Valid from Output Disable	t_{DOA3}	–	–	110	–	–	150	ns
Output Hold from $\overline{\text{Chip-Select 1}}$	t_{DOH1}	20	–	–	20	–	–	ns
Output Hold from Chip-Select 2	t_{DOH2}	20	–	–	20	–	–	ns
Output Hold from Output Disable	t_{DOH3}	20	–	–	20	–	–	ns

† Time required by a limit device to allow for the indicated function
● Typical values are for T_A = 25°C and nominal V_{DD}

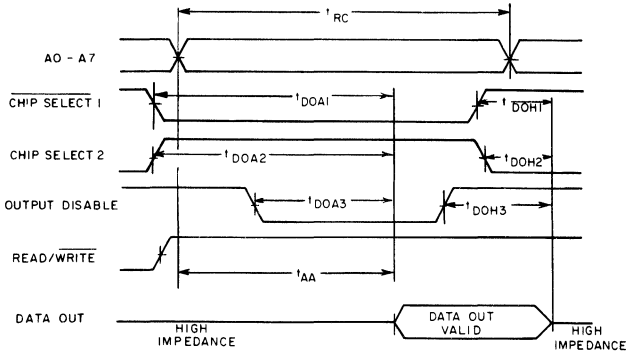
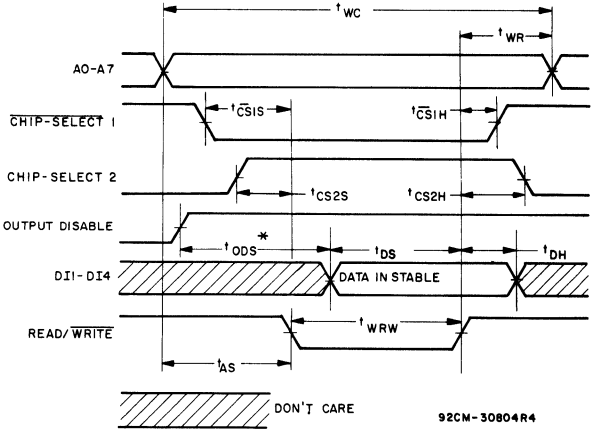


Fig. 1 - Read cycle timing waveforms

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V ±5%, t_r,t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF

CHARACTERISTIC		LIMITS MWS5101D, MWS5101E						UNITS
		L2 Types			L3 Types			
		Min.†	Typ.●	Max.	Min.†	Typ.●	Max.	
Write Cycle Times (Fig. 2)								
Write Cycle	t_{WC}	300	–	–	400	–	–	ns
Address Setup	t_{AS}	110	–	–	150	–	–	
Write Recovery	t_{WR}	40	–	–	50	–	–	
Write Width	t_{WRW}	150	–	–	200	–	–	
Input Data Setup Time	t_{DS}	150	–	–	200	–	–	
Data In Hold	t_{DH}	40	–	–	50	–	–	
$\overline{\text{Chip-Select 1}}$ Setup	$t_{\overline{CS}1S}$	110	–	–	150	–	–	
Chip-Select 2 Setup	t_{CS2S}	110	–	–	150	–	–	
$\overline{\text{Chip-Select 1}}$ Hold	$t_{\overline{CS}1H}$	0	–	–	0	–	–	
Chip-Select 2 Hold	t_{CS2H}	0	–	–	0	–	–	
Output Disable Setup	t_{ODS}	110	–	–	150	–	–	

† Time required by a limit device to allow for the indicated function
● Typical values are for T_A = 25°C and nominal V_{DD}



* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig. 2 - Write cycle timing waveforms.

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DATA RETENTION CHARACTERISTICS at T_A = 0 to 70°C; See Fig. 3

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	V_{DR} (V)	V_{DD} (V)	All Types			
			Min.	Typ.●	Max.	
Minimum Data Retention Voltage, V_{DR}	–	–	–	1.5	2	V
Data Retention Quiescent Current, I_{DD} L2 Types	2	–	–	2	10	μA
Data Retention Quiescent Current, I_{DD} L3 Types	2	–	–	5	50	μA
Chip Deselect to Data Retention Time, t_{CDR}	–	5	600	–	–	ns
Recovery to Normal Operation Time, t_{RC}	–	5	600	–	–	ns
V_{DD} to V_{DR} Rise and Fall Time t_r,t_f	2	5	1	–	–	μs

● Typical values are for T_A = 25°C and nominal V_{DD}

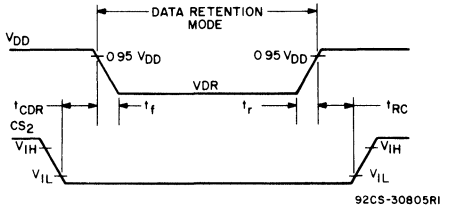

Fig. 3 - Low V_{DD} data retention timing waveforms.

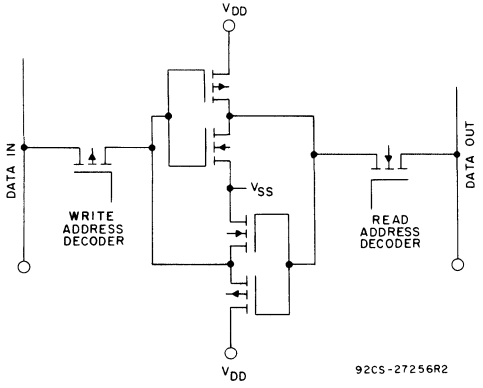

Fig. 4 - Memory cell configuration

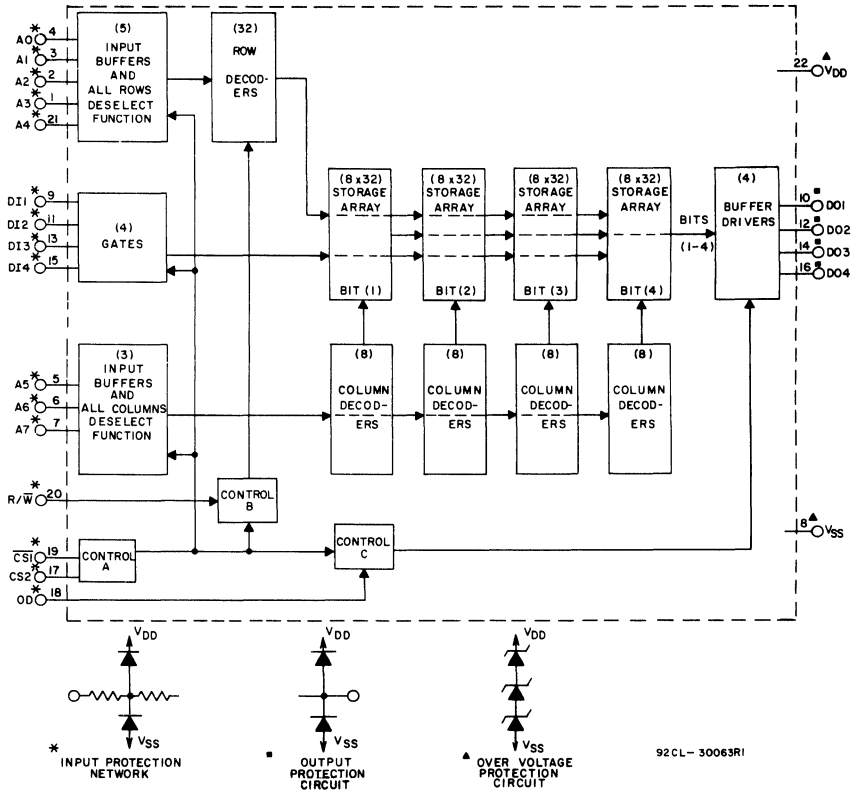

Fig 5 - Functional block diagram for MWS5101

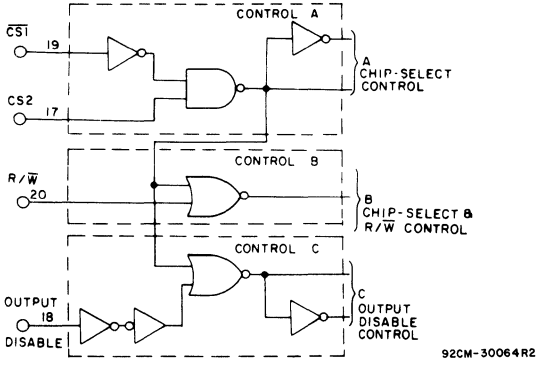

Fig 6 - Logic diagram of controls for MWS5101.