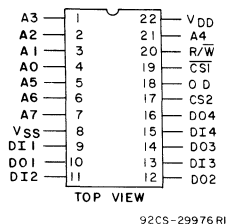


MWS5101A



TERMINAL ASSIGNMENT

256-Word by 4-Bit LSI Static Random-Access Memory

Features:

- Industry standard pinout
- Very low operating current—8 mA at $V_{DD} = 5\text{ V}$ and cycle time = $1\ \mu\text{s}$
- Two Chip-Select inputs—simple memory expansion
- Memory retention for standby battery voltage of 2 V min.
- TTL compatible
- Output-Disable for common I/O systems
- 3-state data output for bus-oriented systems
- Separate data inputs and outputs

The RCA-MWS5101A is a 256-word by 4-bit static random-access memory designed for use in memory systems where high speed, very low operating current, and simplicity in use are desirable. It has separate data inputs and outputs and utilizes a single power supply of 4 to 6.5 volts.

Two Chip-Select inputs are provided to simplify system expansion. An Output Disable control provides Wire-OR capability and is also useful in common Input/Output systems. The Output Disable input allows these RAM's to be used in common data Input/Output systems by forcing the output into a high-impedance state during a write operation independent of the Chip-Select input condition. The output

assumes a high-impedance state when the Output Disable is at high level or when the chip is deselected by CS1 and/or CS2.

For applications requiring CMOS compatibility over wider operating voltage and temperature ranges, the mechanical and functional equivalent RCA-CDP1822 static RAM may be used.

The MWS5101A types are supplied in 22-lead hermetic dual-in-line, side-brazed ceramic packages (D suffix), in 22-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

OPERATIONAL MODES

MODE	INPUTS				OUTPUT
	Chip Select 1 CS1	Chip Select 2 CS2	Output Disable OD	Read/Write R/W	
READ	0	1	0	1	Read
WRITE	0	1	0	0	Data In
WRITE	0	1	1	0	High Impedance
STANDBY	1	X	X	X	High Impedance
STANDBY	X	0	X	X	High Impedance
OUTPUT DISABLE	X	X	1	X	High Impedance

Logic 1 = High Logic 0 = Low X = Don't Care

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OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	ALL TYPES		
	Min.	Max.	
DC Operating-Voltage Range	4	6.5	V
Input Voltage Range	V _{SS}	V _{DD}	

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE (V _{DD})	-0.5 to -7 V
(All voltage referenced to V _{SS} terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V _{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P ₀)*	
For T _A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T _A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T _A = -55 to +100°C (PACKAGE TYPE D)	500 mW
For T _A = +100 to +125°C (PACKAGE TYPE D)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T _A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T _A)	
PACKAGE TYPE D	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T _{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

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STATIC ELECTRICAL CHARACTERISTICS at T_A = 0 to 70°C, V_{DD} = 5 V

CHARACTERISTIC		TEST CONDITIONS		LIMITS			UNITS
		V _O (V)	V _{IN} (V)	MWS5101AD MWS5101AE			
				Min.	Typ.*	Max.	
Quiescent Device Current, I _{DD}	L2 Types	—	0, 5	—	25	50	μA
	L3 Types	—	0, 5	—	100	200	
Output Voltage:	Low-Level, V _{OL}	—	0, 5	—	0	0.1	V
	High-Level, V _{OH}	—	0, 5	4.9	5	—	
Input Low Voltage, V _{IL}	—	—	—	—	—	0.65	
Input High Voltage, V _{IH}	—	—	—	2.2	—	—	
Output Low (Sink) Current, I _{OL}	—	0.4	0, 5	2	4	—	mA
	Output High (Source) Current, I _{OH}	4.6	0, 5	-1	-2	—	
Input Current, I _{IN}	—	—	0, 5	—	—	± 5	μA
3-State Output Leakage Current, I _{OUT}	L2 Types	0, 5	0, 5	—	—	± 5	
	L3 Types	0, 5	0, 5	—	—	± 5	
Operating Current, I _{DD1} #	—	—	0, 5	—	4	8	mA
Input Capacitance, C _{IN}	—	—	—	—	5	7.5	pF
Output Capacitance, C _{OUT}	—	—	—	—	10	15	

*Typical values are for T_A = 25°C and nominal V_{DD}.

#Outputs open-circuited; cycle time = 1 μs.

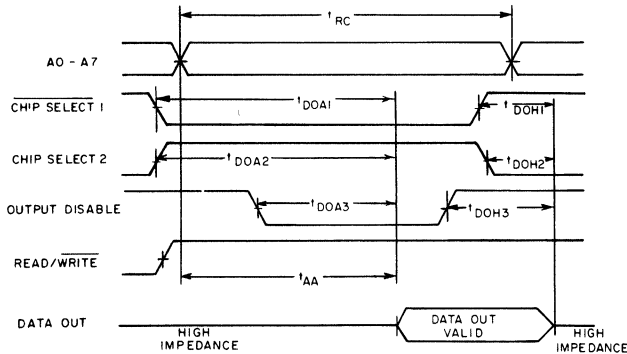
MWS5101A

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V} \pm 5\%$, $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS
	MWS5101AD, MWS5101AE						
	L2 Types			L3 Types			
	Min.†	Typ.*	Max.	Min.†	Typ.*	Max.	
Read Cycle Times (Fig. 1)							
Read Cycle	t_{RC}	250	—	—	350	—	—
Access from Address	t_{AA}	—	150	250	—	200	350
Output Valid from Chip-Select 1	t_{DOA1}	—	150	250	—	200	350
Output Valid from Chip-Select 2	t_{DOA2}	—	150	250	—	200	350
Output Valid from Output Disable	t_{DOA3}	—	—	110	—	—	150
Output Hold from Chip-Select 1	t_{DOH1}	20	—	—	20	—	—
Output Hold from Chip-Select 2	t_{DOH2}	20	—	—	20	—	—
Output Hold from Output Disable	t_{DOH3}	20	—	—	20	—	—

†Time required by a limit device to allow for the indicated function.

*Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .



92CM-30244R4

Fig. 1 - Read cycle timing waveforms

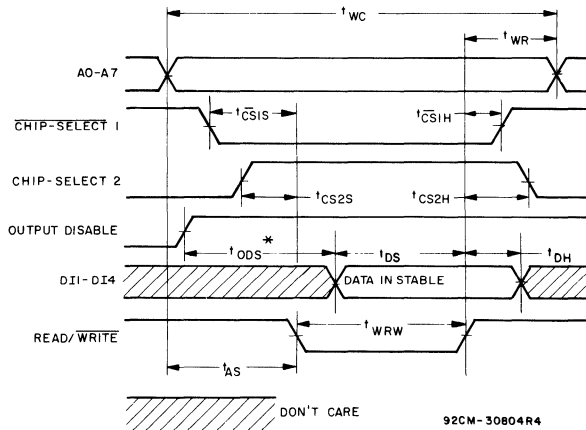
MWS5101A

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 0$ to 70°C , $V_{DD} = 5\text{ V} \pm 5\%$,
 $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$ and 1 TTL Load

CHARACTERISTIC	LIMITS						UNITS	
	MWS5101AD, MWS5101AE							
	L2 Types			L3 Types				
	Min.†	Typ.*	Max.	Min.†	Typ.*	Max.		
Write Cycle Times (Fig. 2)								
Write Cycle	t_{WC}	300	—	—	400	—	—	ns
Address Setup	t_{AS}	110	—	—	150	—	—	
Write Recovery	t_{WR}	40	—	—	50	—	—	
Write Width	t_{WRW}	150	—	—	200	—	—	
Input Data Setup Time	t_{DS}	150	—	—	200	—	—	
Data In Hold	t_{DH}	40	—	—	50	—	—	
Chip-Select 1 Setup	t_{CS1S}	110	—	—	150	—	—	
Chip-Select 2 Setup	t_{CS2S}	110	—	—	150	—	—	
Chip-Select 1 Hold	t_{CS1H}	0	—	—	0	—	—	
Chip-Select 2 Hold	t_{CS2H}	0	—	—	0	—	—	
Output Disable Setup	t_{ODS}	110	—	—	150	—	—	

†Time required by a limit device to allow for the indicated function.
 *Typical values are for $T_A = 25^\circ\text{C}$ and nominal V_{DD} .

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* t_{ODS} IS REQUIRED FOR COMMON I/O OPERATION ONLY, FOR SEPARATE I/O OPERATIONS, OUTPUT DISABLE IS DON'T CARE

Fig 2 - Write cycle timing waveforms

MWS5101A

DATA RETENTION CHARACTERISTICS at $T_A = 0$ to 70°C ; See Fig. 3.

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	VDR (V)	VDD (V)	All Types			
			Min.	Typ.*	Max.	
Minimum Data Retention Voltage, V_{DR}	—	—	—	1.5	2	V
Data Retention Quiescent Current, I_{DD}	L2 Types	—	—	2	10	μA
	L3 Types	—	—	5	50	
Chip Deselect to Data Retention Time, t_{CDR}	—	5	600	—	—	ns
Recovery to Normal Operation Time, t_{RC}	—	5	600	—	—	
VDD to VDR Rise and Fall Time, t_r, t_f	2	5	1	—	—	μs

*Typical values are for $T_A = 25^\circ\text{C}$.

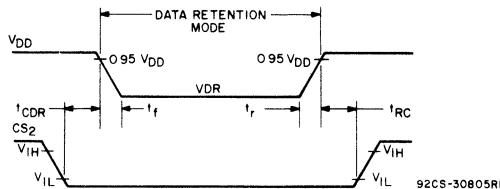


Fig. 3 - Low V_{DD} data retention timing waveforms

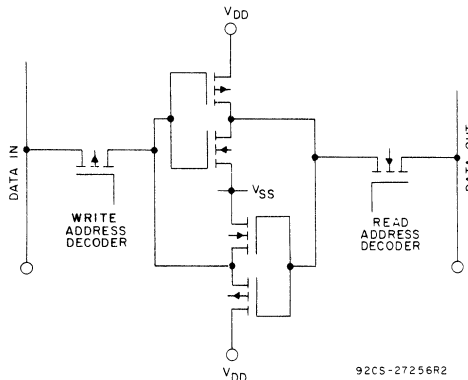


Fig. 4 - Memory cell configuration

MWS5101A

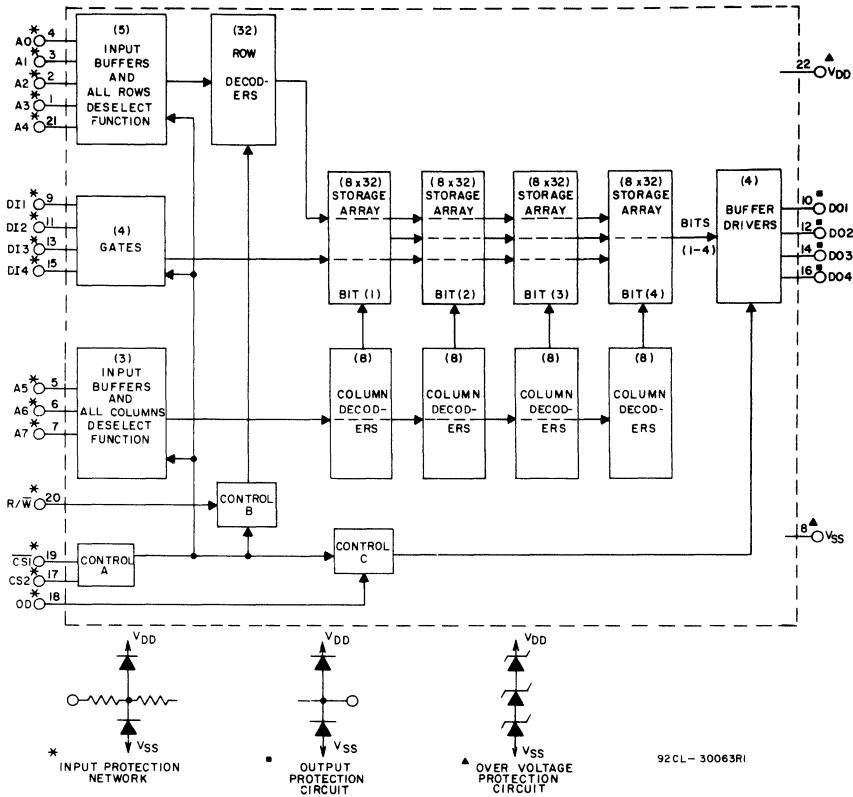


Fig 5 - Functional block diagram for MWS5101A.

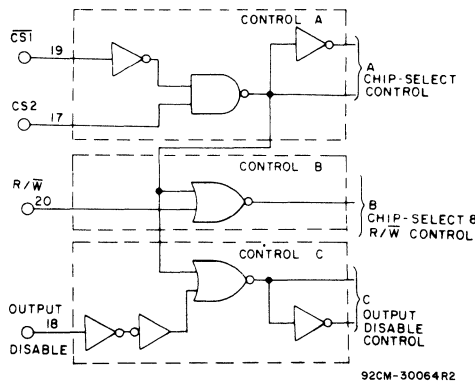


Fig 6 - Logic diagram of controls for MWS5101A.