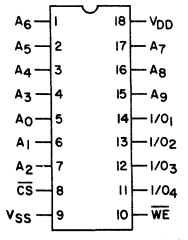
MWS5114



TERMINAL ASSIGNMENT

CMOS 1024-Word by 4-Bit LSI Static RAM

Features:

- *Fully static operation*
- *Industry standard 1024 x 4 pinout (same as pinouts for 6514, 2114, 9114, and 4045 types)*
- *Common data input and output*
- *Memory retention for stand-by battery voltage as low as 2 V min.*
- *All inputs and outputs directly TTL compatible*
- *3-state outputs*
- *Low standby and operating power*

The RCA-MWS5114 is a 1024-word by 4-bit static random-access memory that uses the RCA ion-implanted silicon gate complementary MOS (CMOS) technology. It is designed for use in memory systems where low power and simplicity in use are desirable. This type has common data input and data output and utilizes a single power supply of 4.5 V to 6.5 V.

The MWS5114 is supplied in 18-lead, hermetic, dual-in-line side-brazed ceramic packages (D suffix) and in 18-lead dual-in-line plastic packages (E suffix).

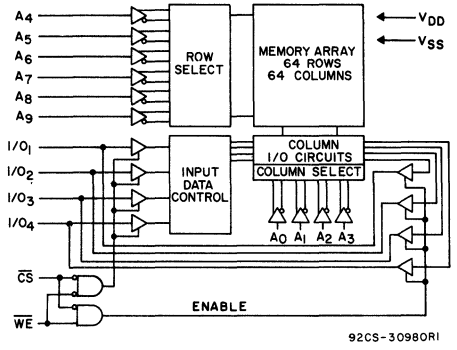


Fig. 1 — Functional block diagram for MWS5114

OPERATIONAL MODES			
FUNCTION	**$\overline{CS}$**	**$\overline{WE}$**	**DATA PINS**
Read	0	1	Output: Dependent on data
Write	0	0	Input
Not Selected	1	X	High-Impedance

File Number **1325**

MWS5114

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +7 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200mW
For T_A = -55 to +100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE D ..... -55 to +125° C
PACKAGE TYPE E ..... -40 to +85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C

OPERATING CONDITIONS at T_A = -40° C to +85° C

For maximum reliability, operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Operating-Voltage Range	4.5	6.5	V
Input Voltage Range	V_{SS}	V_{DD}	

STATIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} ±5%, Except as noted*

CHARACTERISTIC	CONDITIONS			LIMITS									UNITS
	V_O	V_{IN}	V_{DD}	MWS 5114-3			MWS 5114-2			MWS 5114-1			
	(V)	(V)	(V)	MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	MIN.	TYP.•	MAX.	
Quiescent Device Current I_{DD} Max.	—	0,5	5	—	75	100	—	75	100	—	75	250	μA
Output Voltage Low Level V_{OL} Max.	—	0,5	5	—	0	0.1	—	0	0.1	—	0	0.1	V
Output Voltage High Level V_{OH} Min.	—	0,5	5	4.9	5	—	4.9	5	—	4.9	5	—	V
Input Voltage Low Level V_{IL} Max.	0.5,4.5	—	5	—	1.2	0.8	—	1.2	0.8	—	1.2	0.8	V
Input Voltage High Level V_{IH} Min.	0.5,4.5	—	5	2.4	—	—	2.4	—	—	2.4	—	—	V
Output Current (Sink) I_{OL} Min.	0.4	0,5	5	2	4	—	2	4	—	2	4	—	mA
(Source) I_{OH} Max.	4.6	0,5	5	-0.4	-1	—	-0.4	-1	—	-0.4	-1	—	mA
Input Current I_{IN} Max.Δ	—	0,5	5	—	±0.1	±5	—	±0.1	±5	—	±0.1	±5	μA
3-State Output Leakage Current I_{OUT}*	0,5	0,5	5	—	±0.5	±5	—	±0 5	±5	—	±0.5	±5	μA
Operating Device Current I_{DD1}#	—	0,5	5	—	4	8	—	4	8	—	4	8	mA
Input Capacitance C_{IN}	—	—	—	—	5	7.5	—	5	7.5	—	5	7.5	pF
Output Capacitance C_{OUT}	—	—	—	—	10	15	—	10	15	—	10	15	pF

•Typical values are for T_A = 25° C and nominal V_{DD}.
ΔAll inputs in parallel.
#Outputs open circuited; cycle time = 1 μs.
*All outputs in parallel

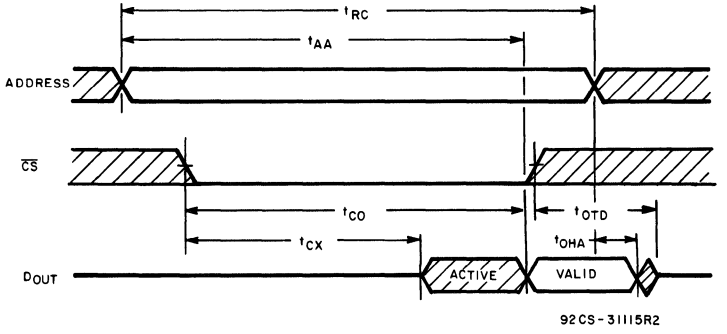
MWS5114

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} = 5 V ±5%, Input t_r, t_f = 10 ns; C_L = 50 pF and 1 TTL Load*

CHARACTERISTIC		LIMITS									UNITS
		MWS 5114-3			MWS 5114-2			MWS 5114-1			
		MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	
Read Cycle Times See Fig. 2											
Read Cycle	t_{RC}	200	160	—	250	200	—	300	250	—	ns
Access	t_{AA}	—	160	200	—	200	250	—	250	300	
Chip Selection to Output Valid	t_{CO}	—	110	150	—	150	200	—	200	250	
Chip Selection to Output Active	t_{CX}	20	100	—	20	100	—	20	100	—	
Output 3-state from Deselection	t_{OTD}	—	75	125	—	75	125	—	75	125	
Output Hold from Address Change	t_{OHA}	50	100	—	50	100	—	50	100	—	

† Time required by a limit device to allow for the indicated function.

*Typical values are for T_A = 25° C and nominal V_{DD}.



NOTE
WE IS HIGH DURING THE READ CYCLE.
TIMING MEASUREMENT REF LEVEL IS 1.5 V

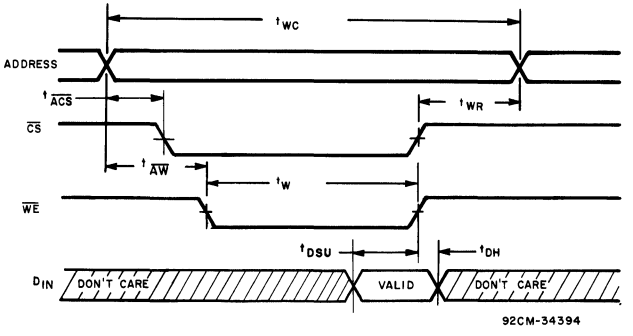
Fig. 2 — Read cycle waveforms.

DYNAMIC ELECTRICAL CHARACTERISTICS *at T_A = 0 to +70° C, V_{DD} = 5V ±5%, Input t_r,t_f = 10 ns; C_L = 50 pF and 1 TTL Load*

CHARACTERISTIC		LIMITS									UNITS
		MWS 5114-3			MWS 5114-2			MWS 5114-1			
		MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	MIN.†	TYP.*	MAX.	
Write Cycle Times See Fig. 3											
Write Cycle	t_{WC}	200	160	—	250	200	—	300	220	—	ns
Write	t_W	125	100	—	150	120	—	200	140	—	
Write Release	t_{WR}	50	40	—	50	40	—	50	40	—	
Address To Chip Select Set-Up Time	$t_{\overline{ACS}}$	0	0	—	0	0	—	0	0	—	
Address To Write Set-up Time	$t_{\overline{AW}}$	25	20	—	50	40	—	50	40	—	
Data to Write Set-up Time	t_{DSU}	75	50	—	75	50	—	75	50	—	
Data Hold From Write	t_{DH}	30	10	—	30	10	—	30	10	—	

† Time required by a limit device to allow for the indicated function.

*Typical values are for T_A = 25° C and nominal V_{DD}.



NOTE: $\overline{WE}$ IS LOW DURING THE WRITE CYCLE
TIMING MEASUREMENT REF. LEVEL IS 1.5 V

Fig. 3 — Write cycle waveforms.

MWS5114

DATA RETENTION CHARACTERISTICS *at T_A = 0 to 70° C; See Fig. 4.*

CHARACTERISTIC		TEST CONDITIONS		LIMITS ALL TYPES			UNITS
		V_{DR} (V)	V_{DD} (V)	MIN.	TYP.*	MAX.	
Minimum Data Retention Voltage	V_{DR}	—	—	2	—	—	V
Data Retention Quiescent Current, I_{DD}	MWS 5114-3	2	—	—	25	50	μA
	MWS 5114-2		—	—	25	50	
	MWS 5114-1		—	—	60	125	
Chip Deselect to Data Retention Time,	t_{CDR}	—	5	300	—	—	ns
Recovery to Normal Operation Time,	t_{RC}	—	5	300	—	—	
V_{DD} to V_{DR} Rise and Fall Time	t_r, t_f	2	5	1	—	—	μs

*Typical values are for T_A = 25° C and nominal V_{DD}.

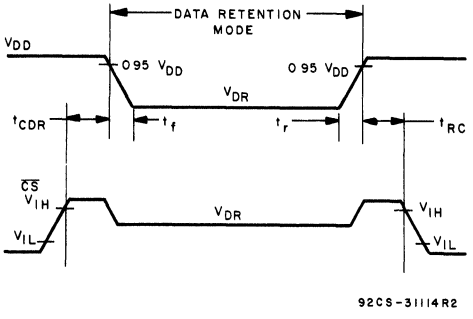


Fig. 4 — Low V_{DD} data retention timing waveforms.