

# MX-COM, INC.

# MX009

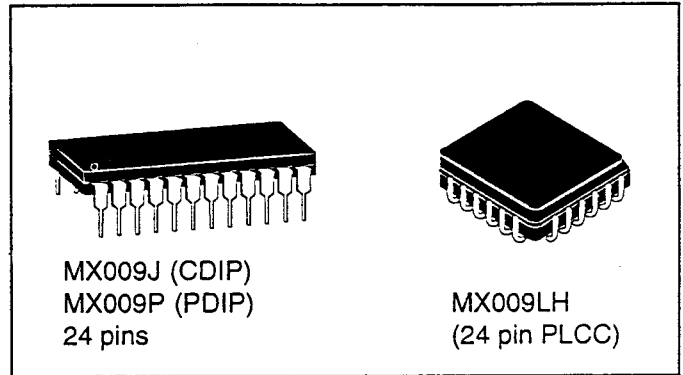
## OCTAL DIGITALLY CONTROLLED AMPLIFIER ARRAY

### Features

- 8 Digitally Controlled Amplifiers
- 15 Gain/Attenuation Steps + Mute
- 7 Trimmers with a  $\pm 3\text{dB}$  Range in 0.43dB Steps
- 1 "Volume" Control with a  $\pm 14\text{dB}$  Range in 2.0 dB Steps
- Individual Control with an 8-Bit Serial Word
- Output Mute/Powersave Function
- Digitally Set Audio Control Levels

### Applications

Cellular and LMR Radios, PABX's, Electronic Mail  
Automatic Test Equipment, Remote Gain Adjustments



## Description

The MX009 Digitally Controlled Amplifier Array replaces trimmers and one volume control in radio and wireline communications applications in which voice or data signals need adjusting. The MX009 is a single-chip LSI circuit comprised of eight discrete, digitally controlled amplifiers, each with 15 distinct gain/attenuation steps plus a MUTE. Control of each amplifier is by an 8-bit serial word.

Seven of the amplifiers have a  $\pm 3\text{dB}$  range stepped in 15 increments of 0.43dB each. The remaining amplifier has a  $\pm 14\text{dB}$  range in 15 steps of 2dB, and is intended for volume control applications. Each digitally controlled amplifier includes a sixteenth "Mute" state which sets the output to bias ( $V_{DD}/2$ ) and powersaves the section addressed. Minimum current drain results from muting all eight sections.

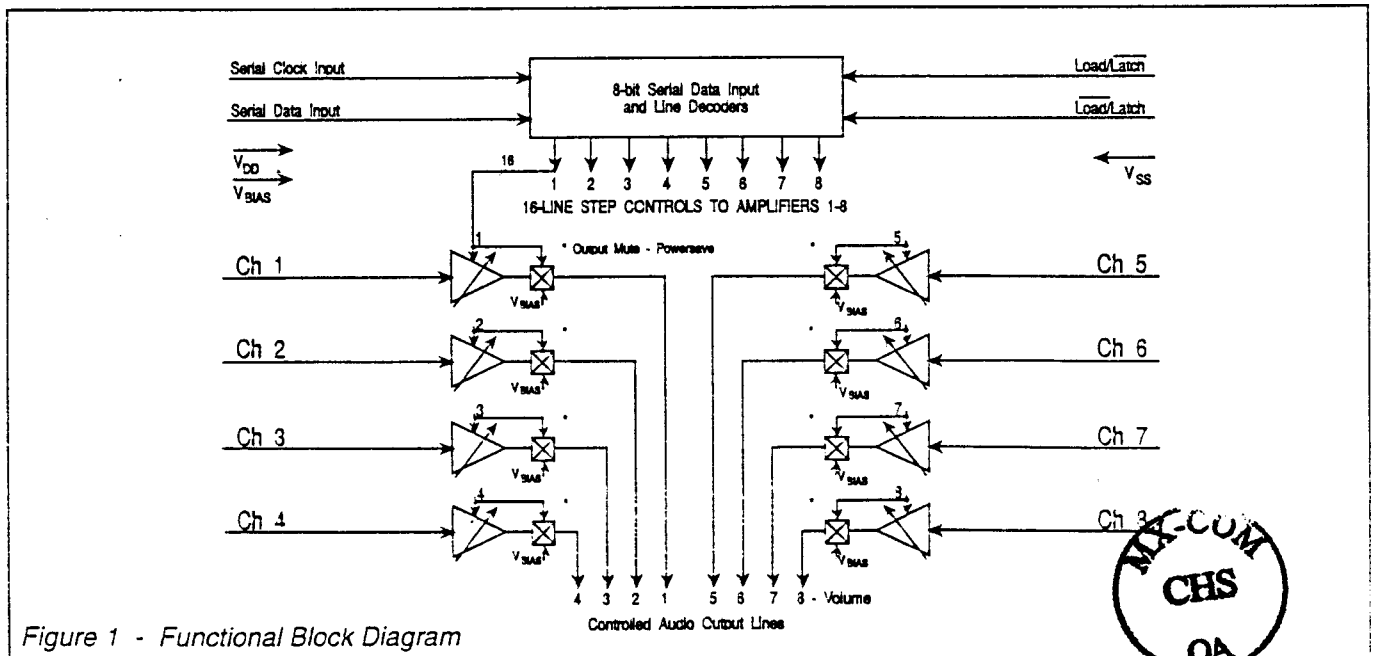
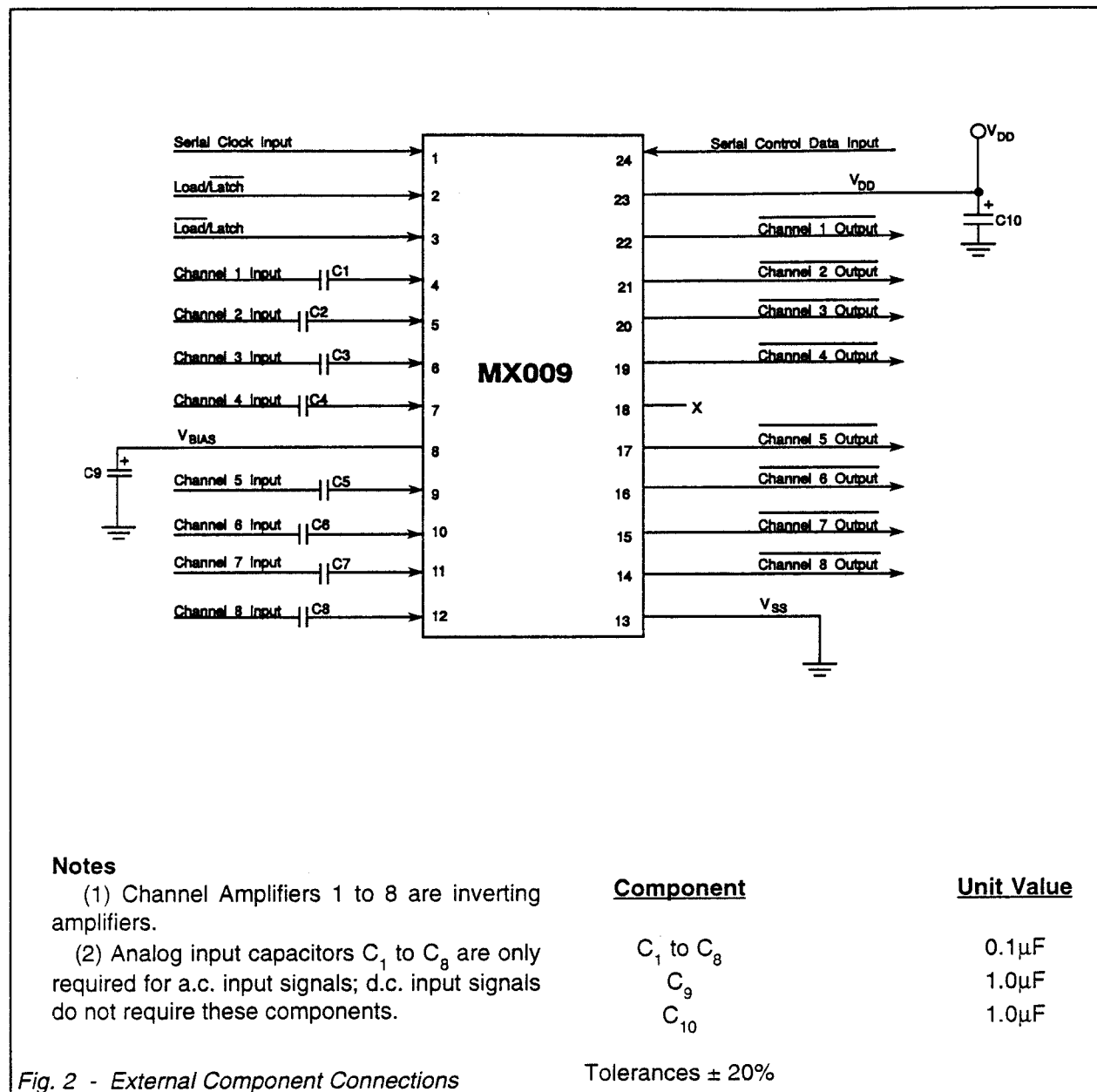


Figure 1 - Functional Block Diagram

## Pin Function Table

| Pin | Function  |
|-----|---|
| 1   | Serial Clock: This external clock pulse input is used to "clock in" the Control Data. See Figure 4, Data Load timing. This input has an internal 1M $\Omega$ pullup resistor.   |
| 2   | $\overline{\text{Load/Latch}}$ : This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "0" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be strobed "0 -> 1 -> 0" to latch the new data in. Data is executed on the falling edge of the strobe. If the $\overline{\text{Load/Latch}}$ input is used this pin should be left open circuit — This input has an internal 1M $\Omega$ pullup resistor.   |
| 3   | $\overline{\text{Load/Latch}}$ : This is the inverted Load/Latch input. This function governs the loading and execution of the control data. During serial data loading this input should be kept at a logical "1" to ensure that data rippling past the latches has no effect. When all 8 bits have been loaded this input should be strobed "1 -> 0 -> 1" to latch the new data in. Data is executed on the rising edge of the strobe. If the $\overline{\text{Load/Latch}}$ input is used this pin should be left open circuit — This input has an internal 1M $\Omega$ pulldown resistor. |
| 4   | Ch 1 Input: Analog Inputs:  |
| 5   | Ch 2 Input: analog signals must be a.c. coupled to these pins, as shown in Figure 2. In the powersave modes the inputs are biased at  |
| 6   | Ch 3 Input: $V_{DD}/2$ . Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps.  |
| 7   | Ch 4 Input: to +15dB in 2.0 dB steps.   |
| 8   | $V_{BIAS}$ : The output of the on-chip bias circuitry, held at $V_{DD}/2$ . This pin should be decoupled to $V_{SS}$ as shown in Figure 2.  |
| 9   | Ch 5 Input: Analog Inputs   |
| 10  | Ch 6 Input:   |
| 11  | Ch 7 Input:   |
| 12  | Ch 8 Input:   |
| 13  | $V_{SS}$ : Negative supply rail (GND).  |
| 14  | $\overline{\text{Ch 8}}$ Output: Analog Outputs: These are the individual "Gain Controlled" amplifier outputs.  |
| 15  | $\overline{\text{Ch 7}}$ Output: Ch1 to Ch7 range from -3dB to +3dB in 0.43dB steps. Ch8 could be   |
| 16  | $\overline{\text{Ch 6}}$ Output: used as a volume control, ranging from -14dB to +14dB in 2.0dB steps.  |
| 17  | $\overline{\text{Ch 5}}$ Output: In the powersave modes the selected output is biased at $V_{DD}/2$ .   |
| 18  | No internal connection. Do not use.   |
| 19  | $\overline{\text{Ch 4}}$ Output: Analog Outputs   |
| 20  | $\overline{\text{Ch 3}}$ Output:  |
| 21  | $\overline{\text{Ch 2}}$ Output: Note that amplifiers Ch1 to Ch8  |
| 22  | $\overline{\text{Ch 1}}$ Output: are "inverting amplifiers."  |
| 23  | $V_{DD}$ : Positive supply. A single +5-volt power supply is required.  |
| 24  | Control (Data) Input: Operation of the 8 amplifier channels (Ch1 - Ch8) is controlled by the 8 bits of data entered serially at this pin. The data is entered (bit 7 to bit 0) on the rising edge of the external Serial Clock. The data format is described in Tables 1, 2 and Figure 4. This input has an internal 1M $\Omega$ pullup resistor.   |

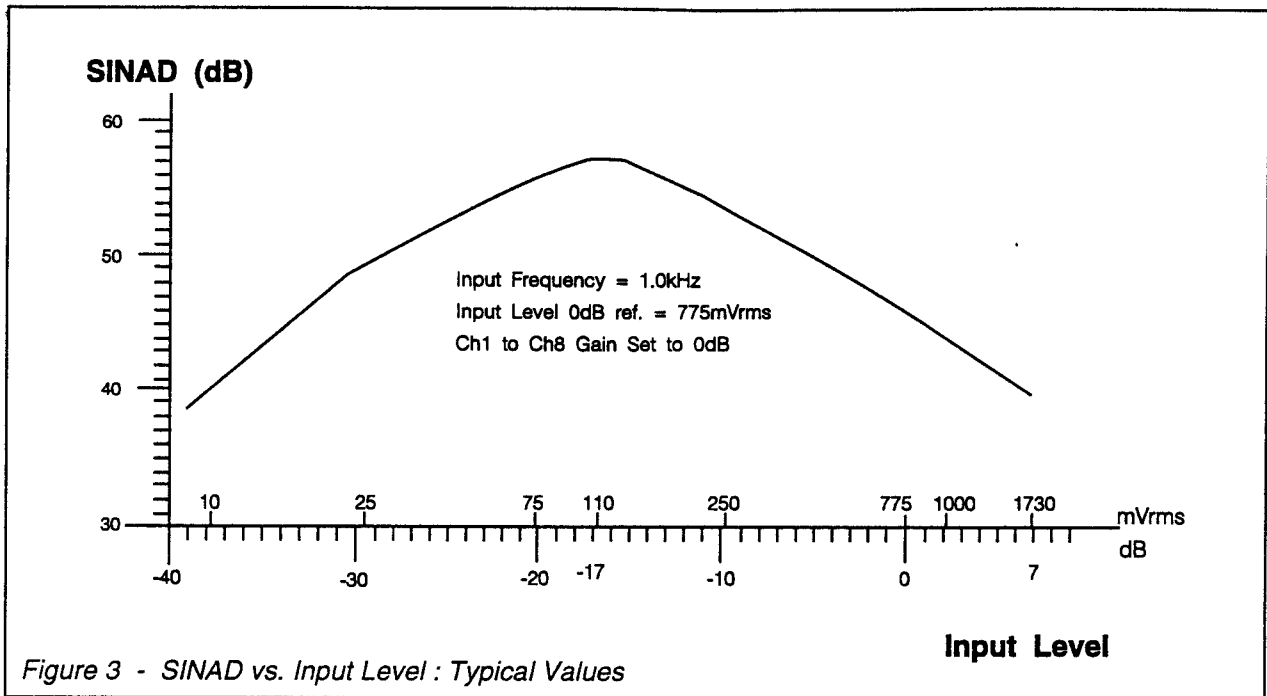
## Application Notes



## Application Recommendations

To avoid noise and instability the following practices are recommended:

- (a) Use a clean, well-regulated power supply.
- (b) Keep leads short.
- (c) Inputs and outputs should be shielded wherever possible.
- (d) Analog tracks should not run parallel to digital tracks.
- (e) A "Ground Plane" connected to  $V_{ss}$  will assist in eliminating external pick-up on the channel input and output pins.
- (f) Avoid running High Level Outputs adjacent to Low Level Inputs.
- (g) Input signal amplitudes should be applied with regard to Figure 3.



## Control Data and Timing

The gain of each amplifier block (Channels 1 to 8) in the MX009 is set individually by an 8-bit data word (bit 7 to bit 0). This 8-bit word, consisting of 4 Address bits (bit 7 to bit 4) and 4 Gain Control bits (bit 3 to bit 0) is serially loaded to the Control Data Input using the external data clock. Data is loaded to the MX009 on the rising edge of the Serial Clock. Loaded data is executed on the falling edge of the Load/Latch pulse and on the rising edge of the Load/Latch pulse. Table 1 shows the format of each 4-bit Address word. Table 2 shows the format of each Gain Control word and Figure 4 shows the data loading operation and timing.

Table 1 Address Word Format

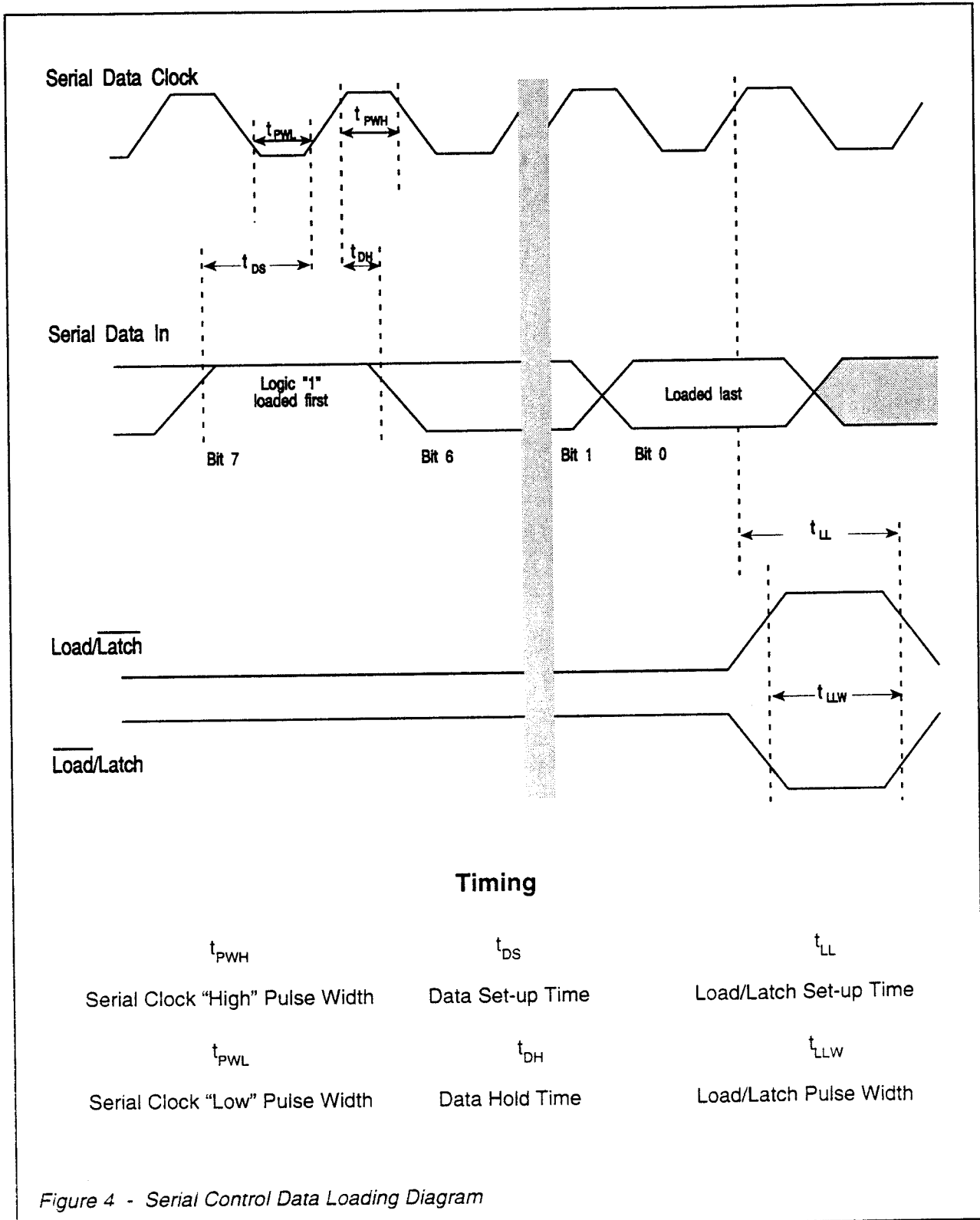
| Bit 7<br>MSB | Bit 6 | Bit 5 | Bit 4<br>LSB | Channel<br>Selected |
|--------------|-------|-------|--------------|---------------------|
| 1            | 0     | 0     | 0            | 1                   |
| 1            | 0     | 0     | 1            | 2                   |
| 1            | 0     | 1     | 0            | 3                   |
| 1            | 0     | 1     | 1            | 4                   |
| 1            | 1     | 0     | 0            | 5                   |
| 1            | 1     | 0     | 1            | 6                   |
| 1            | 1     | 1     | 0            | 7                   |
| 1            | 1     | 1     | 1            | 8                   |

Table 2 Gain Control Word Format

| Bit 3<br>MSB | Bit 2 | Bit 1 | Bit 0<br>LSB | Stage 1 to 7<br>2dB | Stage 8<br>0.43dB |
|--------------|-------|-------|--------------|---------------------|-------------------|
| 0            | 0     | 0     | 0            | Powersave           | Powersave         |
| 0            | 0     | 0     | 1            | -3.0                | -14.0dB           |
| 0            | 0     | 1     | 0            | -2.571              | -12.0dB           |
| 0            | 0     | 1     | 1            | -2.143              | -10.0dB           |
| 0            | 1     | 0     | 0            | -1.714              | -8.0dB            |
| 0            | 1     | 0     | 1            | -1.286              | -6.0dB            |
| 0            | 1     | 1     | 0            | -0.857              | -4.0dB            |
| 0            | 1     | 1     | 1            | -0.428              | -2.0dB            |
| 1            | 0     | 0     | 0            | 0                   | 0.0dB             |
| 1            | 0     | 0     | 1            | 0.428               | 2.0dB             |
| 1            | 0     | 1     | 0            | 0.857               | 4.0dB             |
| 1            | 0     | 1     | 1            | 1.286               | 6.0dB             |
| 1            | 1     | 0     | 0            | 1.714               | 8.0dB             |
| 1            | 1     | 0     | 1            | 2.143               | 10.0dB            |
| 1            | 1     | 1     | 0            | 2.571               | 12.0dB            |
| 1            | 1     | 1     | 1            | 3.0                 | 14.0dB            |

## Data Loading

The 8-bit data word is loaded bit 7 first and bit 0 last. Bit 7 must be a logic "1" to address the chip. If bit 7 in the word is a logic "0" that 8-bit word will not be executed. Figure 4 (below) shows the timing information required to load and operate this device.



# Specifications

## Absolute Maximum Ratings

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not implied.

|  |                                     |
|--|-------------------------------------|
| Supply voltage   | -0.3V to 7.0V                       |
| Input voltage at any pin<br>(ref $V_{SS} = 0V$ )       | -0.3V to ( $V_{DD} + 0.3V$ )        |
| Sink/source current (supply pins)                      | $\pm 30mA$                          |
| (other pins)   | $\pm 20mA$                          |
| Total device dissipation<br>(@ $T_{AMB} 25^{\circ}C$ ) | 800mW Max.                          |
| Derating   | 10mW/ $^{\circ}C$                   |
| Operating temperature:                                 | -40 $^{\circ}C$ to + 85 $^{\circ}C$ |
| Storage temperature:                                   | -55 $^{\circ}C$ to +125 $^{\circ}C$ |

## Operating Limits

All device characteristics are measured under the following conditions unless otherwise specified:

$$V_{DD} = 5.0V$$

$$T_{AMB} = 25^{\circ}C$$

Audio level 0dB ref = 775 mVrms.

| Characteristics                               | See Note              | Min.  | Typ. | Max.      | Unit       |
|---|-----------------------|-------|------|-----------|------------|
| <b>Static Values</b>                          |                       |       |      |           |            |
| Supply Voltage ( $V_{DD}$ )                   |                       | 4.5   | 5.0  | 5.5       | V          |
| Supply Current                                | -Powersave            | —     | 0.16 | 1.0       | mA         |
|   | -All Stages Operating | —     | 4.0  | 8.0       | mA         |
| <b>Dynamic Values</b>                         |                       |       |      |           |            |
| Input Logic "1"                               |                       | 3.5   | —    | —         | V          |
| Input Logic "0"                               |                       | —     | —    | 1.5       | V          |
| Digital Input Impedances                      |                       | 0.5   | 1.0  | —         | M $\Omega$ |
| <b>Amplifier Stages (General)</b>             |                       |       |      |           |            |
| Bandwidth (-3dB)                              |                       | 15.0  | —    | --        | kHz        |
| Output Impedance                              |                       | —     | 0.8  | 3.0       | k $\Omega$ |
| Total Harmonic Distortion                     | 1                     | —     | 0.35 | 0.5       | %          |
| Output Noise Level (per stage)                | 2                     | --    | 65.0 | --        | $\mu Vrms$ |
| Onset of Clipping                             | 3                     | —     | 1.73 | —         | Vrms       |
| Gain Variation                                | 4                     | --    | --   | 0.1       | dB         |
| Interstage Isolation                          |                       | —     | 60.0 | --        | dB         |
| <b>"Trimmer" Stages (Ch 1 - Ch 7)</b>         |                       |       |      |           |            |
| Gain  |                       | -3.0  | —    | +3.0      | dB         |
| Gain Steps (15 in No.)                        |                       | —     | 0.43 | —         | dB         |
| Step Error                                    | 5                     | —     | —    | $\pm 0.2$ | dB         |
| Input Impedance                               |                       | 100.0 | —    | —         | k $\Omega$ |
| <b>"Volume" Stage (Ch 8)</b>                  |                       |       |      |           |            |
| Gain  |                       | -14.0 | —    | +14.0     | dB         |
| Gain Steps (15 in No.)                        |                       | —     | 2.0  | —         | dB         |
| Step Error                                    | 5                     | —     | —    | $\pm 0.4$ | dB         |
| Input Impedance                               |                       | 50.0  | —    | —         | k $\Omega$ |
| <b>Timing (See Figure 4)</b>                  |                       |       |      |           |            |
| Serial Clock "High" Pulse Width ( $t_{PWH}$ ) |                       | 250   | —    | —         | ns         |
| Serial Clock "Low" Pulse Width ( $t_{PWL}$ )  |                       | 250   | —    | —         | ns         |
| Data Set-up Time ( $t_{DS}$ )                 |                       | 150   | —    | —         | ns         |
| Data Hold Time ( $t_{DH}$ )                   |                       | 50    | —    | —         | ns         |
| Load/Latch Set-up Time ( $t_{LL}$ )           |                       | 250   | —    | —         | ns         |
| Load/Latch Pulse Width ( $t_{LLW}$ )          |                       | 150   | —    | —         | ns         |
| Serial Data Clock Frequency                   |                       | —     | —    | 2.0       | MHz        |

### Notes

1. Gain Set 0dB. Input Level 1kHz -3.0dB (549mVrms).
2. a.c. short-circuit input. measured in a 30 kHz bandwidth.
3. See Figure 3.
4. Over temperature and supply voltage range.
5. With reference to a 1.0 kHz signal.

### Package Outlines

The MX009J cerdip package is shown in Figure 5. The MX009P PDIP version is shown in Figure 6, and the "LH" in Figure 7. For identification purposes the MX009LH has an ident spot adjacent to pin 1 and a chamfered corner between pins 3 and 4.

### Handling Precautions

The MX009 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

Figure 5 - MX009J 24-pin Cerdip Package

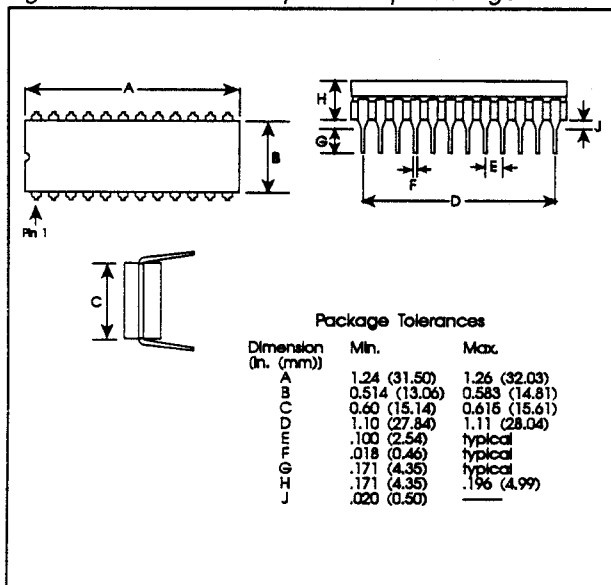


Figure 6 - MX009P 24-pin PDIP Package

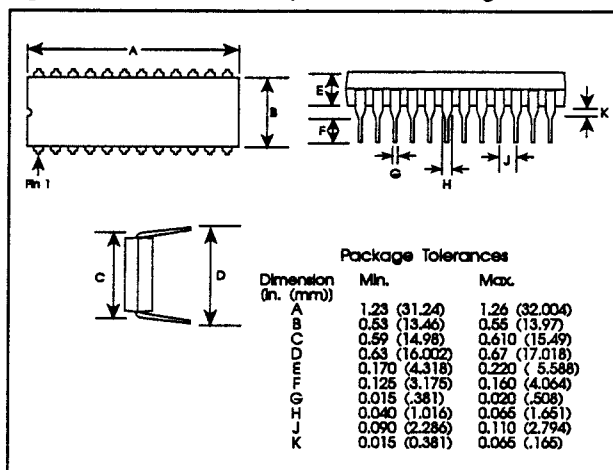
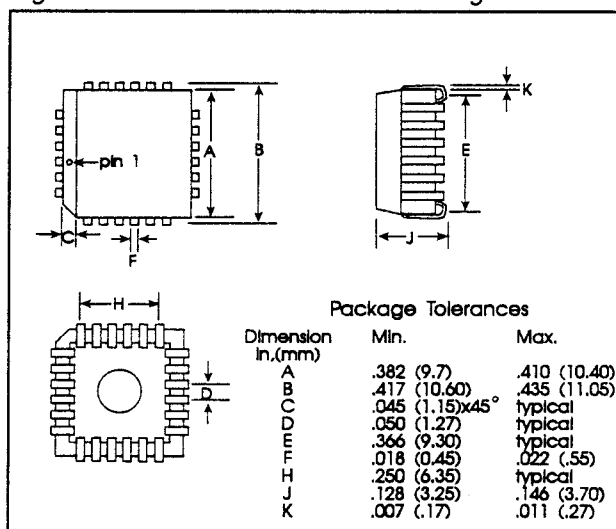


Figure 7 - MX009LH PLCC-24 Package





**CML Microcircuits**

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## CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc (*Consumer Microcircuits Limited (UK)*, *MX-COM, Inc (USA)* and *CML Microcircuits (Singapore) Pte Ltd*) have undergone name changes and, whilst maintaining their separate new names (*CML Microcircuits (UK) Ltd*, *CML Microcircuits (USA) Inc* and *CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.

These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

### CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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