

Description

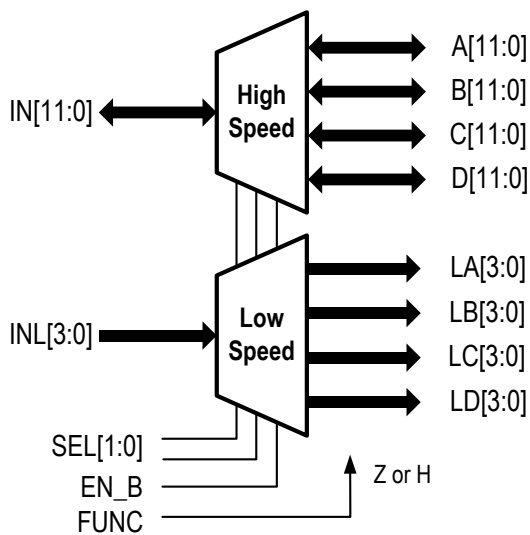
Important: All parameters in this short-form datasheet are prior to device characterization and are currently subject to change. Final parameters will be updated after device characterization.

The MX0141VA0 is comprised of a high-speed, 1:4 multiplexer (mux) path and a low-speed, 1:4 mux path.

The high-speed path is a bidirectional 12-bit port 1:4 mux. The low-speed path is a unidirectional 4-bit port 1:4 mux. Both high-speed and low-speed paths support SSTL_12 and SSTL_18 signaling.

Both paths are controlled in an identical manner using the input control signals: SEL1, SEL0, and EN_B. For example, when EN_B is asserted LOW, one of the high-speed [ABCD] ports is connected to IN while all the remaining ports are tri-stated. When input EN_B is HIGH all four [ABCD] ports are tri-stated.

Figure 1. Block Diagram



Typical Applications

- SATA drive memory expansion for both ONFI3 and TOGGLE2 Flash medium
- General purpose 1:4 multiplexing logic for compact, low-power product solutions

Common High/Low MUX

- 1:4 mux (separate high-speed and low-speed groups)
- SSTL18 and SSTL12 signaling through mux
- Mux $R_{ON} = 8\Omega$ at 0.9V condition
- Pinout allows easy routing when two of these parts are placed directly over each other on the top and bottom of the circuit board
- “Break before make” switching
- 4 x 7.5 mm 98-FCCSP package with 0.5mm ball pitch

High-Speed MUX Features

- 533MT/s
- 12-bit bus width, each port
- Bidirectional ports
- Tri-state for deselected ports
- Pin-to-pin output skew < 50ps
- Propagation delay < 100ps
- Insertion loss < 2dB

Low-Speed MUX Features

- 50MT/s
- 4-bit bus width, each port
- Unidirectional ports
- Either tri-state or weak pull-up for deselected ports as selected via the FUNC pin

Table 1. Characteristics of HS and LS Paths

Feature	HS Path	LS Path
Port speed	533MT/s	50MT/s
Port size	12-bit	4-bit
Direction	Bidirectional IN \leftrightarrow A, B, C, or D	Unidirectional INL \rightarrow LA, LB, LC, or LD
Control pins	SEL[1:0], EN_B	SEL[1:0], EN_B, FUNC

1. Pin Descriptions

Table 2. Pin Descriptions

Pin Name	Type	Description
IN[11:0]	Bidirectional	Host high-speed signals
INL[3:0]	Input	Host upstream low-speed signals ^[a]
A[11:0]	Bidirectional	Port A high-speed signals
B[11:0]	Bidirectional	Port B high-speed signals
C[11:0]	Bidirectional	Port C high-speed signals
D[11:0]	Bidirectional	Port D high-speed signals
LA[3:0]	Output	Port A downstream low-speed signals ^[a]
LB[3:0]	Output	Port B downstream low-speed signals ^[a]
LC[3:0]	Output	Port C downstream low-speed signals ^[a]
LD[3:0]	Output	Port D downstream low-speed signals ^[a]
SEL[1:0]	Input	Control inputs
EN_B	Input	Control input
FUNC	Input	Z/H select for low-speed ports (see section 4.3 for details) ^[a]

[a] The voltages on these pins must always be equal to or lower than the voltage on VDD. This also applies during device power up sequencing.

2. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the MX0141VA0 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{DD}	Power supply voltage		$V_{SS} < V_{DD}$	3.0	V
V_{IH}	High-level input voltage		–	$V_{DD} + 0.5$	V
V_{IL}	Low-level input voltage		$V_{SS} - 0.3$	–	V
T_J	Junction temperature		–	150	°C
T_S	Storage temperature		-65	150	°C
HBM	ESD Human Body Model		–	2000	V
CDM	ESD Charged Device Model		–	1000	V
MM	ESD Machine Model		–	200	V

3. Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Power supply voltage	2.375	2.5	2.625	V
V_{IH}	High-level input voltage	V_{SS}	–	V_{DD}	V
V_{IL}	Low-level input voltage	V_{SS}	–	V_{DD}	V
T_A	Ambient temperature	0	–	85	°C

4. Theory of Operation

4.1 Control Logic – High-Speed Ports

The SEL0, SEL1, and EN_B pins control the connection between the IN port and the selected A, B, C, or D high-speed port as defined in Table 5. The IN, A, B, C, and D ports are bidirectional. “Z” indicates tri-state and all bits follow the IOL_{HS} specification.

Table 5. Control of High-Speed Ports

Control		High-Speed Ports				
SEL[1:0]	EN_B	IN	A	B	C	D
00	0	A	IN	Z	Z	Z
01	0	B	Z	IN	Z	Z
10	0	C	Z	Z	IN	Z
11	0	D	Z	Z	Z	IN
XX	1	Z	Z	Z	Z	Z

4.2 Control Logic – Low-Speed Ports

The SEL0, SEL1, EN_B, and FUNC pins control the connection between the INL port and the selected LA, LB, LC, and LD low-speed ports as defined in Table 6. “Z” indicates tri-state and all bits follow the IOL_{HS} specification. “H” indicates that all bits follow the R_{LS} specification with the internal pull-up side set to the FUNC input pin voltage. INL is a unidirectional signal multiplexed to the selected LA, LB, LC, or LD port.

Table 6. Control of Low-Speed Ports

Control			Low-Speed Ports			
FUNC	SEL[1:0]	EN_B	LA	LB	LC	LD
0	00	0	INL	Z	Z	Z
0	01	0	Z	INL	Z	Z
0	10	0	Z	Z	INL	Z
0	11	0	Z	Z	Z	INL
0	XX	1	Z	Z	Z	Z
1	00	0	INL	H	H	H
1	01	0	H	INL	H	H
1	10	0	H	H	INL	H
1	11	0	H	H	H	INL
1	XX	1	H	H	H	H

4.3 FUNC Pin Description

The FUNC pin is used to choose either the “Z” tri-state or a weak pull-up for the low-speed outputs when deselected.

Example 1: The FUNC pin is set to less than 0.3V. In this example, deselected low-speed outputs will be “Z” = tri-state.

Example 2: The FUNC pin is set to greater than 0.9V. In this example, deselected low-speed mux outputs will be pulled to the FUNC voltage level through individual internal pull-up resistors of value R_{LS} . For example, if FUNC is set to 1.8V, then deselected low-speed mux outputs will be pulled up to 1.8V through individual internal pull-up resistors of the value R_{LS} .

Example 3: The FUNC pin is set to a voltage between 0.3V and 0.9V. In this example, the FUNC input is set to an illegal voltage level and the FUNC pin functionality is undetermined.

5. Package Drawings

98-FCCSP package information is available on the IDT website at www.idt.com/package/AVG98.

6. Marking Diagram

The following package marking diagram is for illustration purposes only.

LINE 1 LINE 2 LINE 3 LINE 4	Line 1 – IDTMX0141 Line 2 – VA0AVG Line 3 – #YYWW\$ where # is the step; YYWW is the last two digits of the year followed by two digits for the workweek; and \$ is the assembly location Line 4 – Lot number
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7. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Packaging	Temperature
MX0141VA0AVG	MX0141VA0, 4.0 x 7.5 mm 98-FCCSP (AVG98)	3	Tray	0° to +85°C
MX0141VA0AVG8	MX0141VA0, 4.0 x 7.5 mm 98-FCCSP (AVG98)	3	Tape and Reel	0° to +85°C

8. Revision History

Revision Date	Description of Change
May 1, 2017	Implementation of the following edit corresponding to edit in full <i>MX0141VA0 Datasheet</i> approved revision dated April 19, 2017: <ul style="list-style-type: none"> ▪ Deletion of note regarding availability being limited to samples in section 7.
April 6, 2017	Initial release of short-form datasheet.



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