GENERAL DESCRIPTION

MX1323AS is a secondary side switch IC designed for flyback converter. This IC emulate the behavior of diode rectifier for reduces power dissipation. MX1323AS works in CCM、DCM and quasi-resonant operation modes. Ruggedness and noise immunity are accomplished using an advanced blanking scheme and double pulse suppression which allow reliable operation in all operating modes.

MX1323AS senses the internal drain-source voltage of the MOSFET, and output ideal drive signal with less external components. It provides high performance solutions for 3.3-12V output voltage application.

MX1323AS is offered in SOP-8 package.

FEATURES

- Internal 60V 10mΩ trench MOSFET
- Up to 200kHz operation frequency
- 80ns turn on propagation delay and 15ns turn off delay
- Lower quiescent current consumption
- CCM/DCM and Quasi-resonant operation modes compatible
- VDD under voltage lock out
- 4.5A sink current to turn off MOSFET fast

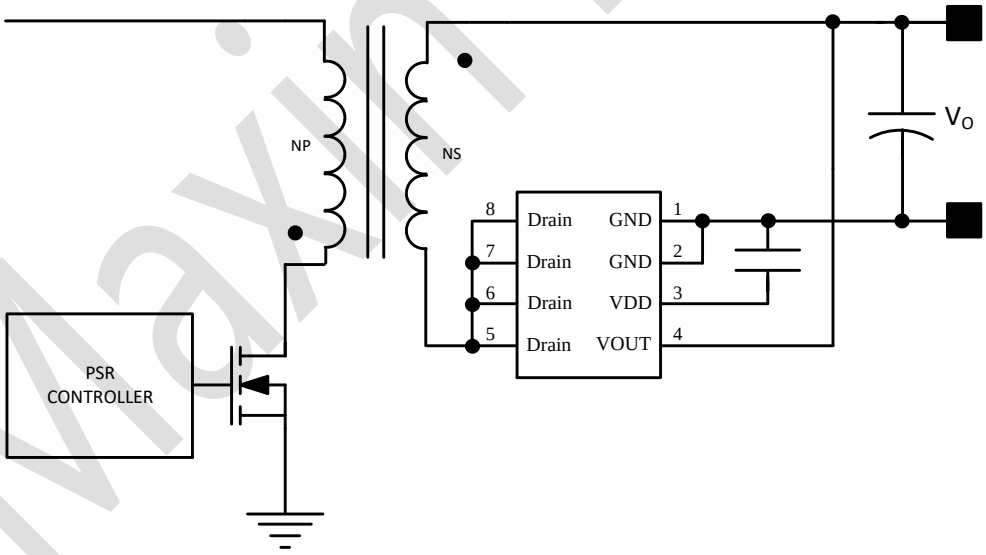
Applications

Cell Phone Charger

Auxiliary Power Adapter

PD/QC Charger

Typical Application



General information

Ordering information

Part Number	Description
MX1323AS	SOP8，Halogen-free，RoHS

Package dissipation rating

Package	RθJA（℃/W）
SOP8	90

Note: Drain Pin Connected to 200mm^2 PCB copper clad.

Absolute maximum ratings

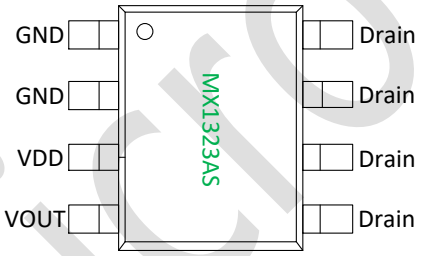
Parameter	Value
Drain Voltage (off state)	60
VDD Voltage	-0.3 to 7V
VOUT Voltage	-0.3 to 25V
Min/Max Operating Junction Temperature TJ	-40 to 150℃
Min/Max Storage Temperature T_{STG}	-55 to 150℃
ESD(HBM)	±2kV
Lead Temperature (Soldering, 10secs)	260℃

Note: stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Recommended operating condition

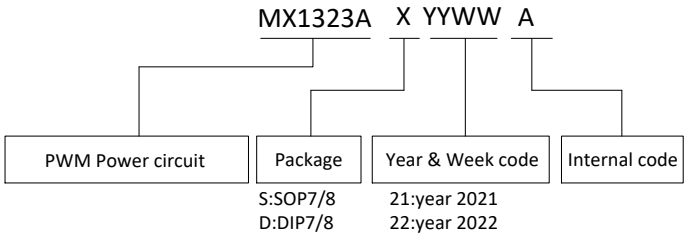
Symbol	Parameter	Range
VDD	VDD supply voltage	3.3-12V
PD	Power dissipation @TA=25℃	1.1W
Output power	5V3A /9V2.2A/12V1.7Atypical	20W

Terminal assignments

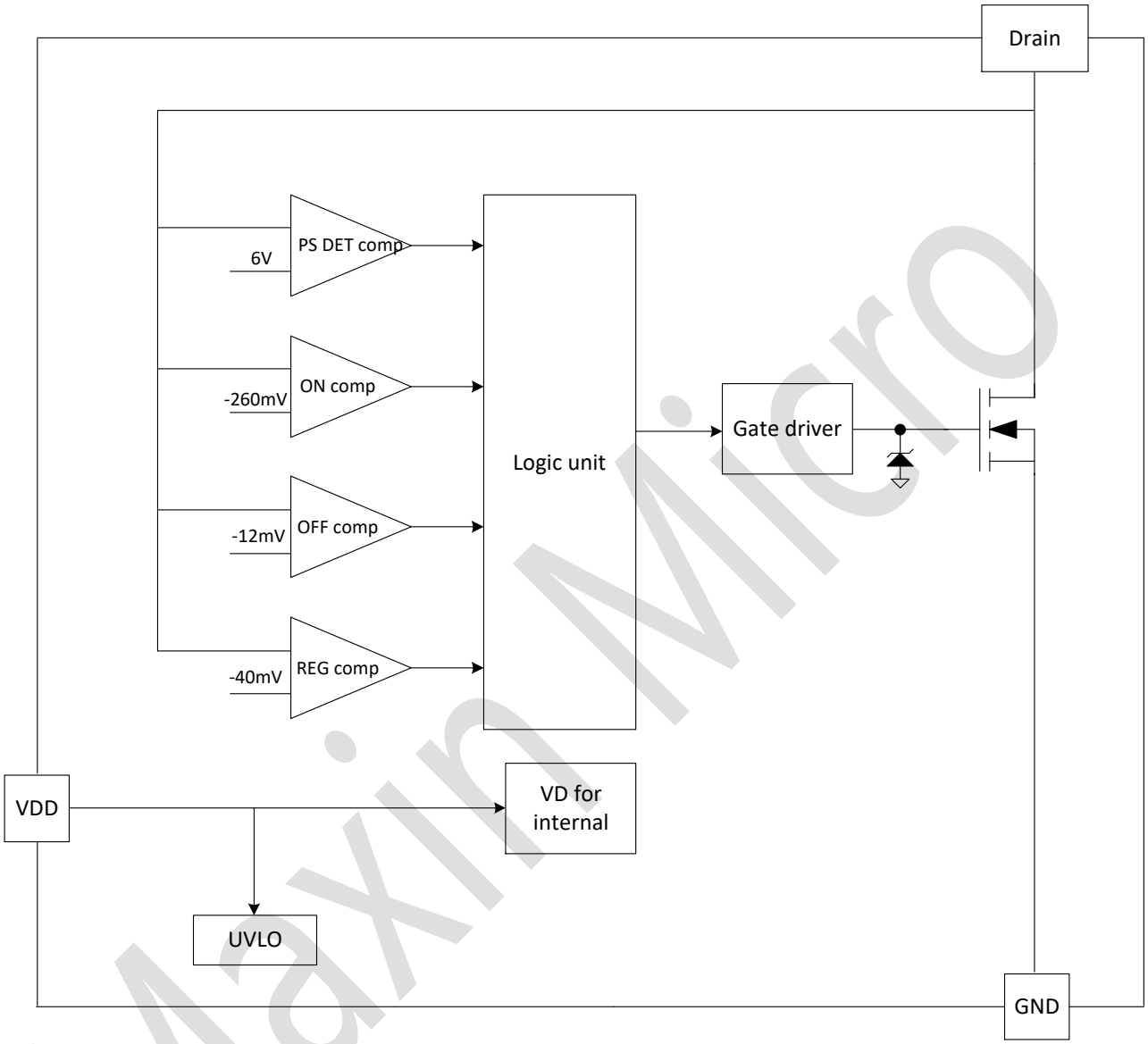


PIN NO.	PIN name	Description
1/2	GND	Power ground，the source of internal MOSFET.
3	VDD	Power supply.
4	VOUT	Output voltage detect pin.
5/6/7/8	Drain	Internal MOSFET drain side.

Marking information



Block Diagram



Electrical characteristics

（TA=25℃，VDD=5V，unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
VDD supply voltage						
I_VDD	Quiescent current	VDD=6.0V	140	180	250	μA
UVLO_ON	VDD under voltage lockout enter	VDD rising up	2.4	2.5	2.6	V
UVLO_OFF	VDD under voltage lockout exit		2.8	2.9	3.0	V
I_OUTC	VOUT charging current	VOUT=5V, VDD=3.5V		65		mA
Control circuitry section						
V_{ON_TH}	Turn on threshold (V_{DRAIN}-V_{SOURCE})		-300	-260	-240	mV
T_{ON_DELAY}	Turn on propagation delay	CLOAD=5nF		80		ns
		CLOAD=10nF		90		ns
V_{OFF_TH}	Turn off threshold (V_{SOURCE}-V_{DRAIN})		-20	-12	-9	mV
T_{OFF_DELAY}	Turn off propagation delay	CLOAD=5nF		15		ns
		CLOAD=10nF		25		ns
$V_{REG(DRV)}$	Drive regulation voltage		-50	-40	-32	mV
T_{ON_MIN}	Minimum on time		550	650	800	ns
T_{OFF_MIN}	Minimum off time		0.9	1.2	2.5	μs
$V_{PS\_ON\_DET}$	Primary side on detection voltage			6		V
$T_{PS\_ON\_DET}$	Primary side on detection blanking time			300		ns
MOSFET						
RDS_ON	Static Drain to Source on resistance			10		mΩ
VDS	Drain to Source breakdown voltage		60			V

Operation description

MX1323AS detects the drain to source voltage of internal MOSFET. When the secondary winding is on, the current flow the parasitic diode of MOSFET. If the drain voltage is lower than the turn on threshold voltage V_{ON_TH}, the internal drive circuit turn on the MOSFET after a turn on delay time T_{ON_DELAY}. Then the lower conduction loss can be achieved.

UVLO and Power Supply

MX1323AS remains in the UVLO condition until the voltage on the VDD exceeds the voltage UVLO_ON. During the time the gate drive circuit is inactive. The UVLO mode is accessible from any other state of operation whenever MX1323AS supply voltage condition of VDD is smaller than UVLO_OFF occurs.

MX1323AS supply voltage is monitored by the UVLO circuit. It is possible to turn off the circuit by pulling VDD voltage below the turn off threshold voltage. To prevent noise problems, a bypass ceramic capacitor connected to VDD and GND.

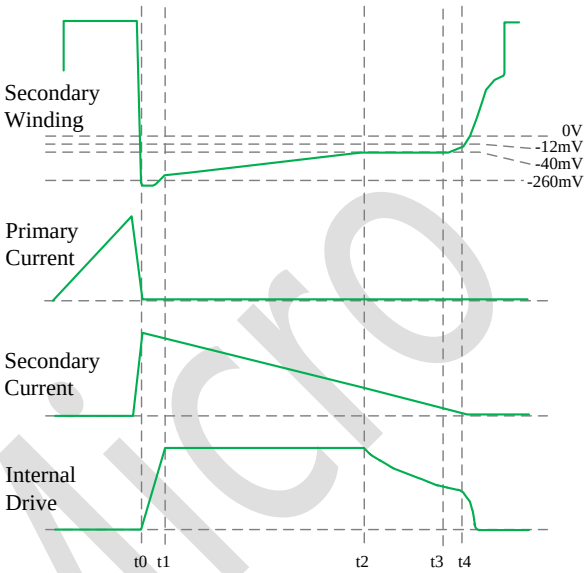
Minimum ON time

When the internal MOSFET is turned on and some ringing noise may be generated. If that noise falls below the threshold VOFF_TH before minimum on time expires, the internal MOSFET will keep on until the end of the minimum on time.

Turn On and Turn OFF Phase

When second winding is on, current will start flowing through its body diode, generating a negative voltage between drain and source. When the voltage up to the turn on threshold V_{TH_ON}, internal circuit will drive the gate of internal MOSFET on, which will in turn cause the conduction voltage to drop down. The minimum on time will prevent the turn off from some amount of ringing. And the Drain to Source voltage will shrink as the secondary current decreases. Then the Drian to Source voltage will be maintained -40mV by adjusting internal drive voltage.

When the current flowing close to 0A, the -40mV will not be maintained by internal driver. The Drain to Source voltage continue rising which to reach the threshold V_{OFF_TH} (-12mV typical), the internal MOSFET will be turned off after the propagation delay time T_{OFF_DELAY}. After the internal MOSFET is turned off, it is necessary to detect that the Drian to Source voltage reach about 6V or more and after a continuation time greater than $T_{PS\_ON\_DET}$ (300ns typical), a valid primary side turn on is confirmed to avoid false turn on caused by quasi-resonant. The following figure shows the timing of turn on and turn off.



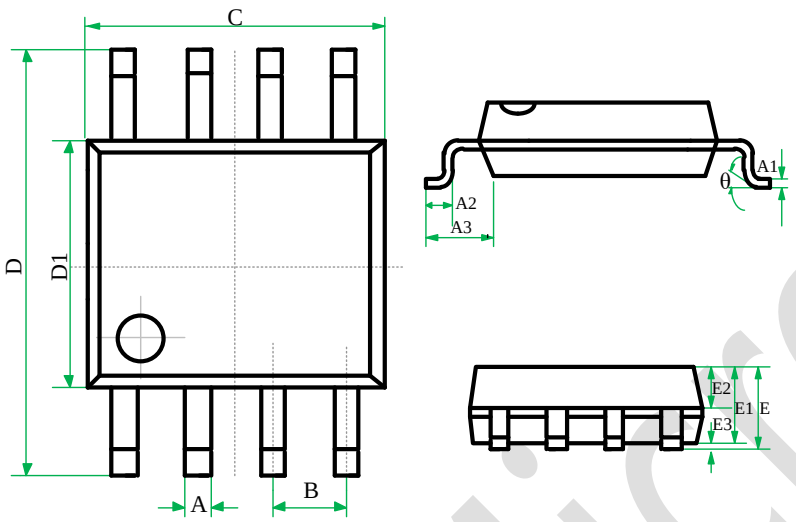
The timing of turn on and turn off

Minimum ON time

The aera of the secondary current loop including the MX1323AS and the output capacitor should be as small as possible to reduce EMI radiation. And the PCB trace must be wide and short for thermal consideration.

The bypass capacitor on VDD should be placed as close as possible to the VDD pin. And the negative node of VDD capacitor should be connected directly to the GND pin.

Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.39	-	0.48	0.0154	-	0.0189
A1	0.21	-	0.28	0.008	-	0.011
A2	0.50	-	0.80	0.020	-	0.031
A3	1.05BSC			0.041BSC		
B	1.27BSC			0.050BSC		
C	4.70	4.90	5.10	0.185	0.193	0.201
D	5.80	6.00	6.20	0.228	0.236	0.244
D1	3.70	3.90	4.10	0.146	0.154	0.161
E	-	-	1.75	-	-	0.069
E1	1.30	1.40	1.50	0.051	0.055	0.059
E2	0.60	0.65	0.70	0.024	0.026	0.028
E3	0.10	-	0.225	0.004	-	0.009
θ	0	-	8°	0	-	8°

SOP8 for MX1323AS

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.