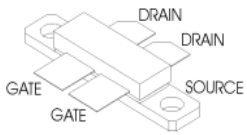
MX1506VP LDMOS TRANSISTOR

Document Number: MX1506VP
Preliminary Datasheet V1.0

60W, 50V High Power RF LDMOS FETs

MX1506VP



Description

The MX1506VP is a 60-watt, highly rugged, thermally enhanced, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5 GHz.

It is featured for high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as FM radio, VHF TV and Aerospace applications.

- Typical Performance (On Innogration narrow band fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 200 mA, CW.

Frequency	Gp (dB)	P_{out} (W)	η_D@P_{out} (%)
915 MHz	23	60	60

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 1200-1400MHz(L band)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)
- 960-1215MHz(Avionics)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+125	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, Pout=60W CW,	$R_{\theta JC}$	1.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class

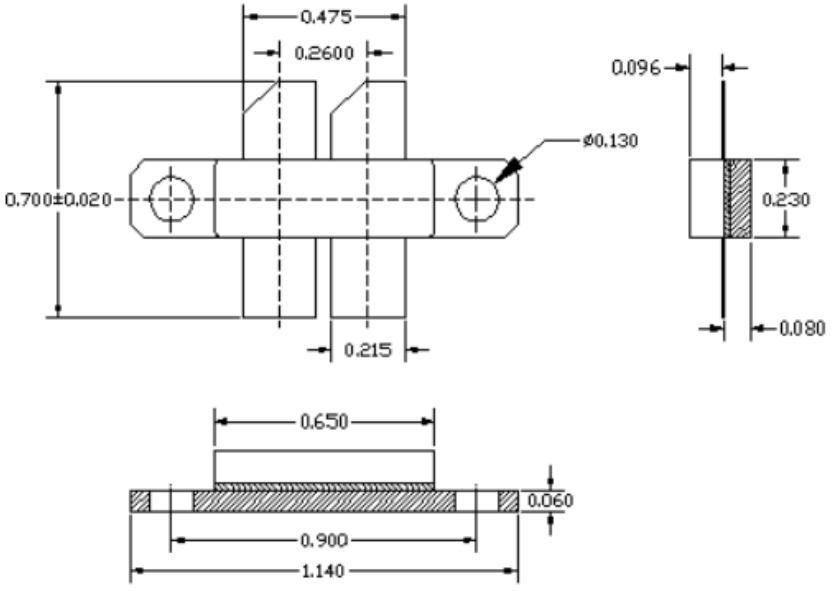
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

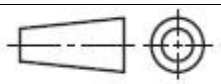
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0Ma	$V_{(BR)DSS}$		125		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	V_{GS}(th)	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.57	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		900		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		28.3		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		11.9		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		0.38		pF
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 200mA, f = 915 MHz, CW Signal Measurements, Pin=25dBm					
Power Gain@Pout	Gp	——	23	——	dB
Output Power	Pout		60		W
Drain Efficiency@Pout	η_D	——	60	——	%
Input Return Loss	IRL	——	-7	——	dB
Ruggedness at all phase angle	VSWR		10:1		

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/-.005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					**03/12/2013**

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2018/3/3	Rev 1.0	Preliminary Datasheet Creation

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