

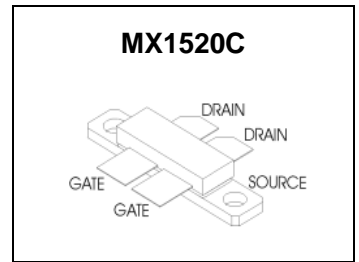
MX1520C LDMOS TRANSISTOR

Document Number: MX1520C
Product Datasheet V1.0

200W, 28V High Power RF LDMOS FETs

Description

The MX1520C is a 200-watt high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 1.5 GHz.



- **Typical performance(on 108-512MHz wideband board with device soldered)**

Signal: Two-tone space 1.6MHz , Vgs=2.75V, Vds=28V, Idq=900mA

Freq(MHz)	Pin(dBm)	Pav(W)	Ids(A)	Gain(dB)	Eff(%)	IMD3
48	23	40	4.56	23	31	-30
58	22.2	40	4.3	23.8	33	-32
68	22	40	4.06	24	35	-32
88	21.6	40	3.75	24.4	38	-32
108	21.4	40	3.57	24.6	40	-33
150	21.8	40	3.51	24.2	41	-32
200	21.5	40	3.52	24.5	40	-37
225	22.4	40	3.56	23.6	40	-38
250	23.1	40	3.6	22.9	39	-39
300	23	40	3.65	23	39	-40
350	22.2	40	3.63	23.8	39	-37
400	22.6	40	3.56	23.4	40	-33
450	23.1	40	3.64	22.9	39	-34
512	22.7	40	3.81	23.3	37	-32

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+65	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+32	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C

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Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ\text{C}$, $T_J = 200^\circ\text{C}$, DC test	$R_{\theta JC}$	0.35	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (per half section)

Drain-Source Voltage $V_{GS} = 0$, $I_{DS} = 1.0\text{mA}$	$V_{(BR)DSS}$	65			V
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{V}$, $V_{GS} = 0\text{V}$)	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current ($V_{GS} = 10\text{V}$, $V_{DS} = 0\text{V}$)	I_{GSS}	—	—	1	μA
Gate Threshold Voltage ($V_{DS} = 28\text{V}$, $I_D = 600\mu\text{A}$)	$V_{GS(th)}$	—	1.98	—	V
Gate Quiescent Voltage ($V_{DD} = 28\text{V}$, $I_D = 220\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$	—	2.53	—	V
Drain source on state resistance ($V_{DS} = 0.1\text{V}$, $V_{GS} = 10\text{V}$)	$R_{ds(on)}$		100		$\text{m}\Omega$
Common Source Input Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{ISS}		92		pF
Common Source Output Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{OSS}		39		pF
Common Source Feedback Capacitance ($V_{GS} = 0\text{V}$, $V_{DS} = 28\text{V}$, $f = 1\text{MHz}$)	C_{RSS}		1.58		pF

Functional Tests (In Demo Test Fixture, 50 ohm system) $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 220\text{mA}$, $f = 1300\text{MHz}$, CW Signal Measurements.

Power Gain	G_p	—	18	—	dB
Drain Efficiency@P1dB	η_D	—	65	—	%
1 dB Compression Point	P_{-1dB}	—	200	—	W
Input Return Loss	IRL	—	-7	—	dB

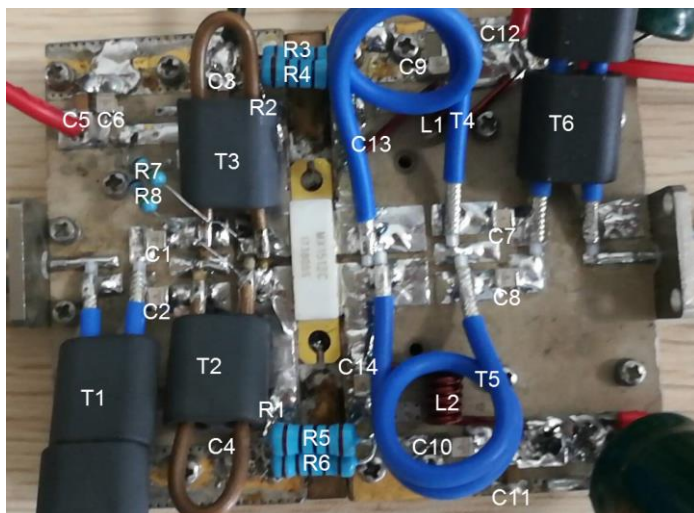
Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28\text{Vdc}$, $I_{DQ} = 220\text{mA}$, $f = 1300\text{MHz}$

VSWR 10:1 at 200W CW Output Power	No Device Degradation
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Figure 1: 108-512MHz wideband application circuit picture



Bill of Materials

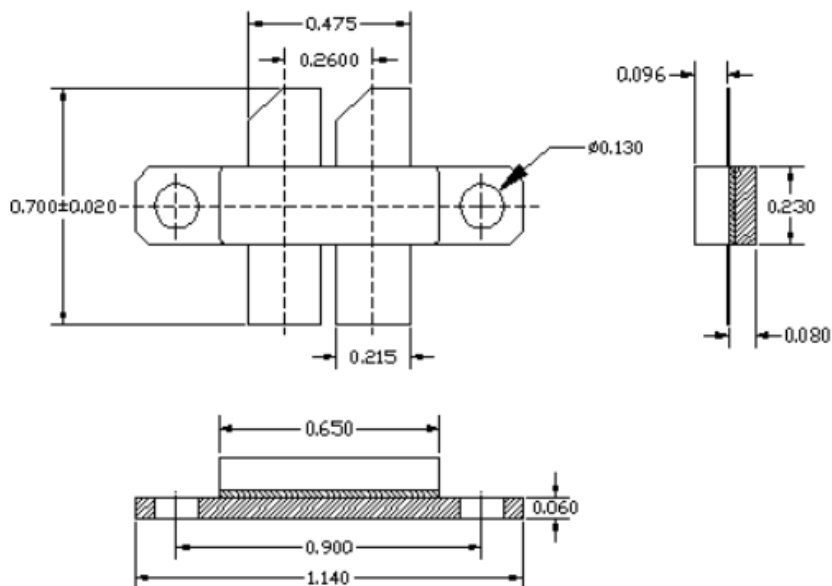
C1,C2,C6, C7,C8,C9, C10,C13, C14	1000PF	ATC100B
C3,C4,C5, C11,C12	1UF	1UF/50V
R1,R2	10Ω	1206
R3,R4,R5, R6	1000Ω	
R7,R8	51Ω	
T1,T6	50Ω,90mm	No.61
T2,T3	12Ω,70mm	No.61
T4,T5	25Ω,120mm	
L1,L2	5 Turns	D=3mm

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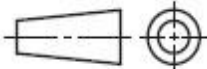
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Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads



Tolerance .XX +/-0.01 .XXX +/- .005 inches

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-LB/LBB					03/12/2013

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2017/10/13	Rev 1.0	Product Datasheet Creation

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