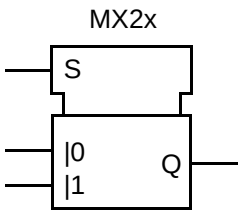
Description

MX2x is a family of two-to-one digital multiplexers.

Logic Symbol



Truth Table

S	I0	I1	Q
L	L	X	L
L	H	X	H
H	X	L	L
H	X	H	H

HDL Syntax

Verilog ..... MX2x *inst_name* (Q, I0, I1, S);

VHDL..... *inst_name*: MX2x port map (Q, I0, I1, S);

Pin Loading

Pin Name	Equivalent Loads			
	MX21	MX22	MX24	MX26
I0	1.0	1.0	2.1	2.1
I1	1.1	1.0	2.1	2.1
S	2.2	2.2	4.2	4.2

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX21	3.0	TBD	5.9
MX22	4.0	TBD	7.3
MX24	7.0	TBD	13.0
MX26	8.0	TBD	15.8

a. See page 2-15 for power equation.

AMI5HG 0.5 micron CMOS Gate Array

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
MX21	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.35 0.40	0.46 0.54	0.58 0.69	0.71 0.85	0.81 0.97
	From: S To: Q	t_{PLH} t_{PHL}	0.40 0.51	0.50 0.63	0.62 0.78	0.76 0.95	0.87 1.08
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
MX22	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.37 0.44	0.51 0.61	0.61 0.73	0.71 0.85	0.81 0.97
	From: S To: Q	t_{PLH} t_{PHL}	0.43 0.53	0.57 0.70	0.67 0.83	0.77 0.95	0.86 1.07
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
MX24	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.33 0.42	0.46 0.58	0.57 0.69	0.67 0.80	0.75 0.93
	From: S To: Q	t_{PLH} t_{PHL}	0.40 0.51	0.52 0.67	0.62 0.79	0.72 0.90	0.82 1.00
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
MX26	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.40 0.47	0.54 0.65	0.64 0.78	0.72 0.90	0.80 1.01
	From: S To: Q	t_{PLH} t_{PHL}	0.44 0.58	0.58 0.74	0.69 0.87	0.78 0.99	0.87 1.11

Delay will vary with input conditions. See page 2-17 for interconnect estimates.