MX23C6410

5V 64M-BIT Mask ROM
PDIP Package Only

FEATURES

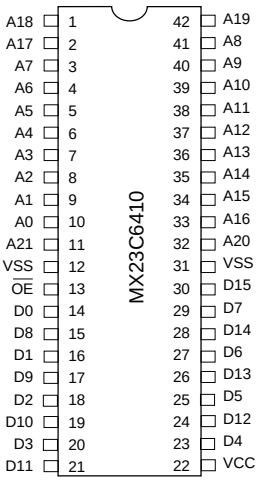
- Bit organization
  - 4M x 16 (word mode)
- Fast access time
  - Random access: 100ns (max.)
- Current
  - Operating: 70mA
- Supply voltage
  - 5V±10%
- Package
  - 42 pin PDIP (600mil)

ORDER INFORMATION

Part No.	Access Time	Package
MX23C6410PC-10	100ns	42 pin PDIP
MX23C6410PC-12	120ns	42 pin PDIP
MX23C6410PC-15	150ns	42 pin PDIP

PIN CONFIGURATION

42 PDIP (Word mode only & without CE pin)



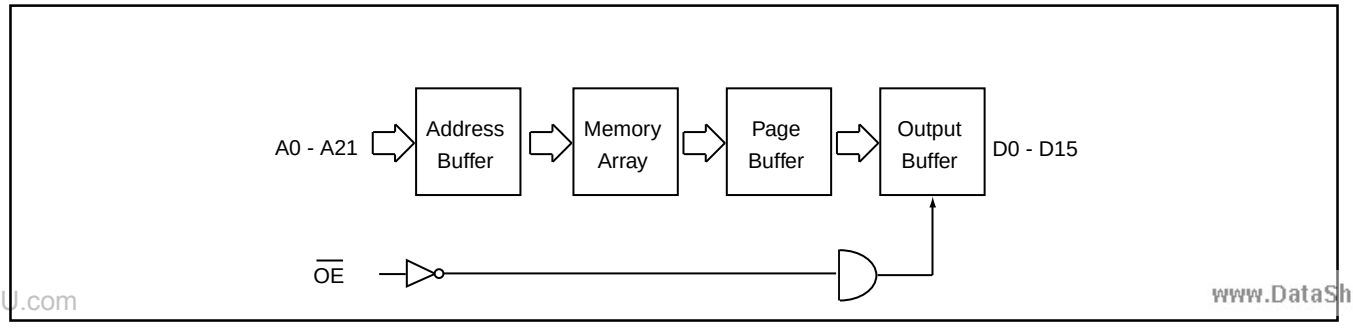
PIN DESCRIPTION

Symbol	Pin Function
A0~A21	Address Inputs
D0~D15	Data Outputs
$\overline{OE}$	Output Enable Input
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

MODE SELECTION

$\overline{OE}$	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	High Z	High Z	-	Active
L	Output	D0~D7	D8~D15	Word	Active

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Supply Voltage Relative to VSS	VCC	-0.5V to 6.5V
Voltage on any Pin Relative to VSS	VIN	-0.8V to VCC+2.0V
Ambient Operating Temperature	Topr	0℃ to 70℃
Storage Temperature	Tstg	-65℃ to 125℃

DC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -1.0mA
Output Low Voltage	VOL	-	0.4V	IOL = 2.1mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC1	-	70mA	f=5MHz, all output open
Input Capacitance	CIN	-	10pF	Ta = 25℃, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25℃, f = 1MHZ

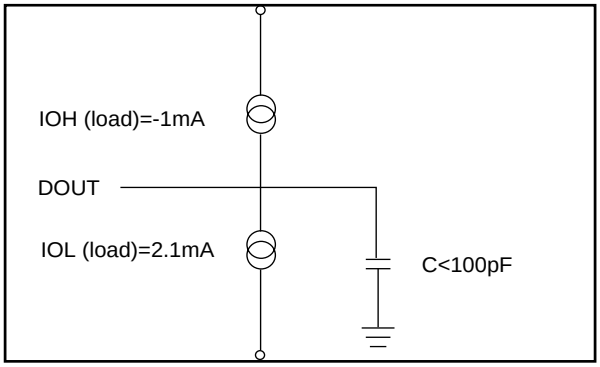
AC CHARACTERISTICS (Ta = 0℃ ~ 70℃, VCC = 5V±10%)

Item	Symbol	23C6410-10		23C6410-12		23C6410-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	0ns	-	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note:Output high-impedance delay (tHZ) is measured from $\overline{OE}$ going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

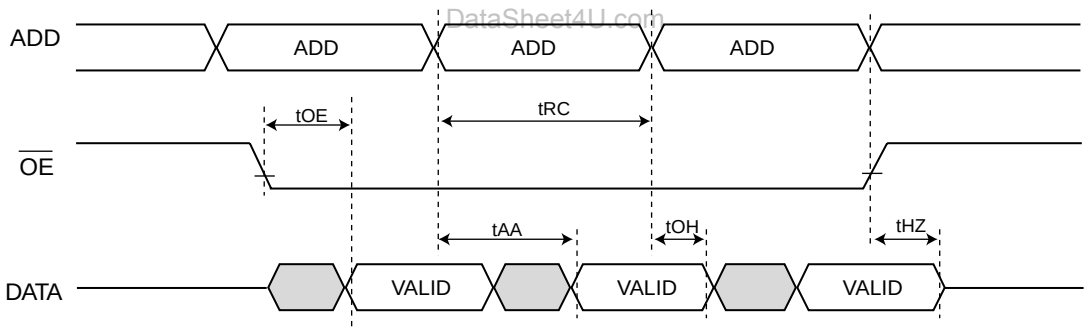
Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	0.8V and 2.0V
Output Load	See Figure



Note:No output loading is present in tester load board.
Active loading is used and under software programming control.
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

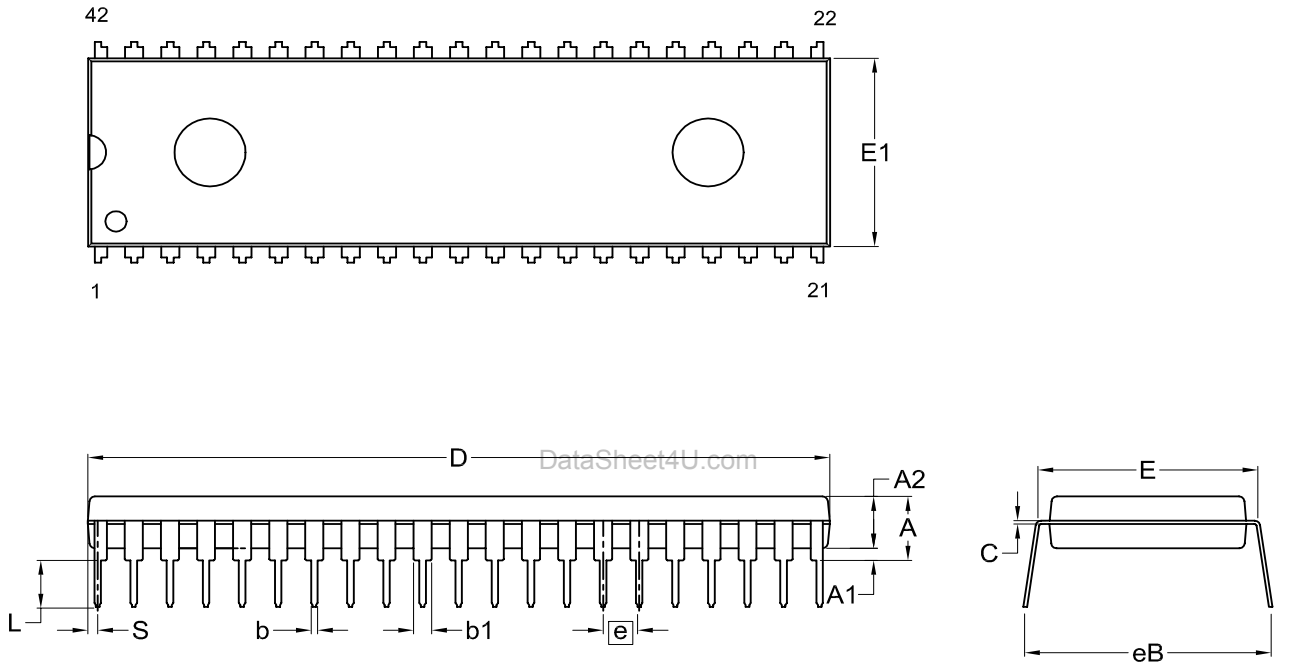
RANDOM READ



Note: $\overline{OE}$ are enable

PACKAGE INFORMATION

Title: Package Outline for PDIP 42L (600MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.25	3.73	0.38	1.14	0.20	51.31	15.11	13.84		15.75	2.92	0.38
	Nom.	---	---	3.94	0.46	1.27	0.25	51.94	15.24	13.97	2.54	16.51	3.30	0.64
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	52.57	15.37	14.10		17.27	3.68	0.89
Inch	Min.	—	0.010	0.147	0.015	0.045	0.008	2.020	0.595	0.545		0.620	0.115	0.015
	Nom.	—	—	0.155	0.018	0.050	0.010	2.045	0.600	0.550	0.100	0.650	0.130	0.025
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	2.070	0.605	0.555		0.680	0.145	0.035

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.5	7				01-20-03

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	The VCC Range of 100ns speed grade was changed, 5V ± 5%--> 5V ± 10%	P1	JUL/27/2001
1.2	1. Add supply voltage relative to VSS	P2	JUL/25/2002
1.3	1. Modify Package Information	P4	NOV/21/2002
1.4	1. Modify Package Information	P4	JUN/20/2003

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