Sequential 4G-Bits XtraROM for Amusement

1. FEATURES

- Organization
  - 256M x 16bit
  - Page Size : 512words(support sequential read)
- Memory Area: Please refer to *"7. MEMORY AREA"*
- Read Operation
  - Latency : 15us
  - Read Cycle Time : 40ns
- Voltage Supply : 3.0V ~ 3.6V
- Current
  - Read : 120mA
  - Stand-by : 200uA
- Command/Address/Data Multiplexed Port
- Package : 70-pin SSOP
- All devices are RoHS compliant

2. GENERAL DESCRIPTION

The MX23J4G76 is a single 3.3V XtraROM, density 4Gbit, factory pre-programmed ROM with Macronix NBit technology.

It utilizes the 16 bit multiplexed I/O bus for command, address, and data inputs/outputs.

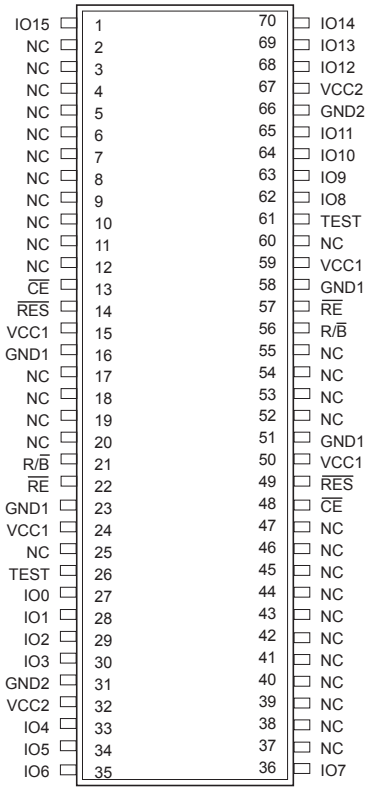
Simple design structure makes the cost of the device and competitive over the other types of code-storage memory IC.

3. ORDER INFORMATION

Part No.	Read Cycle Time	Package
MX23J4G76MC-40G	40ns	70 SSOP

4. PIN CONFIGURATIONS

70 SSOP

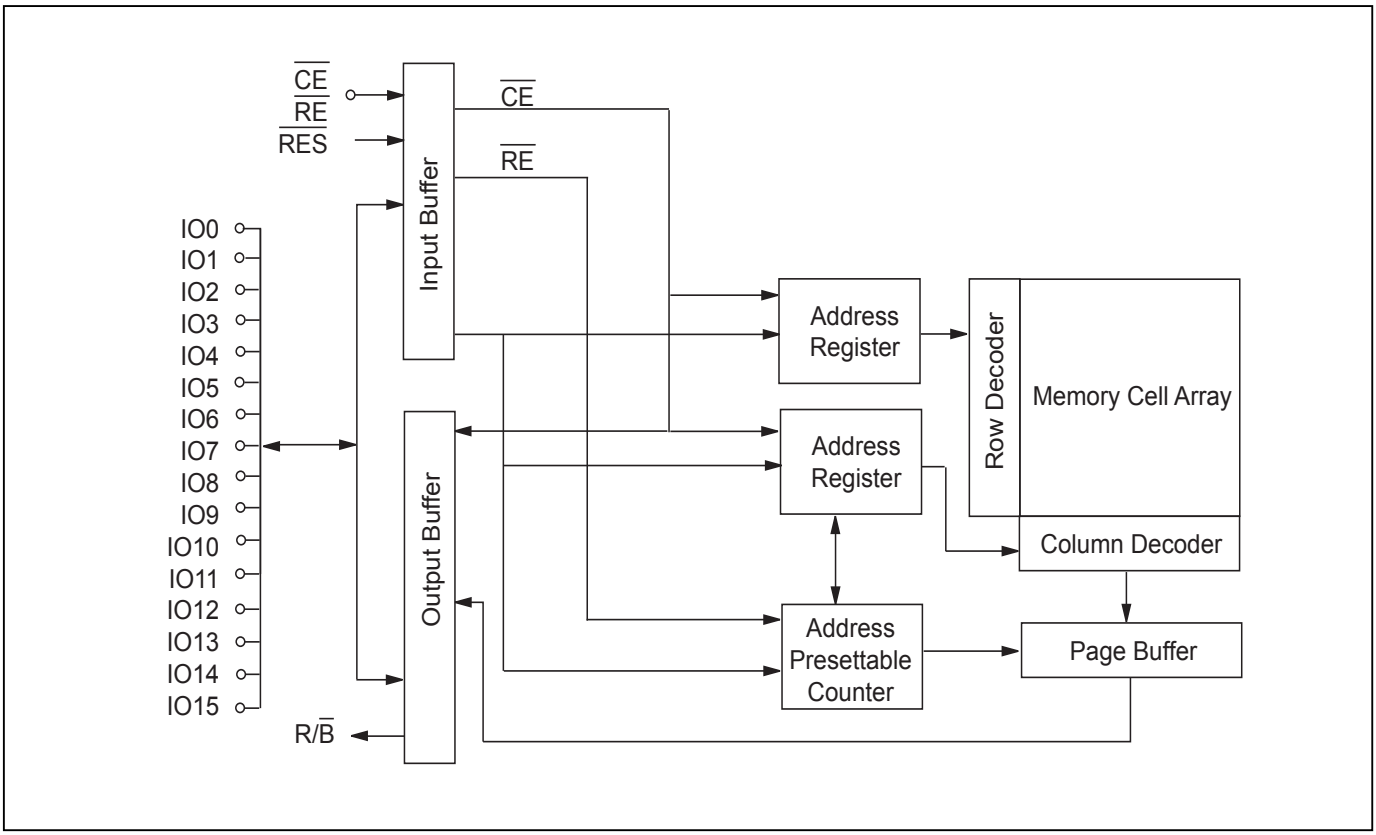


5. PIN DESCRIPTION

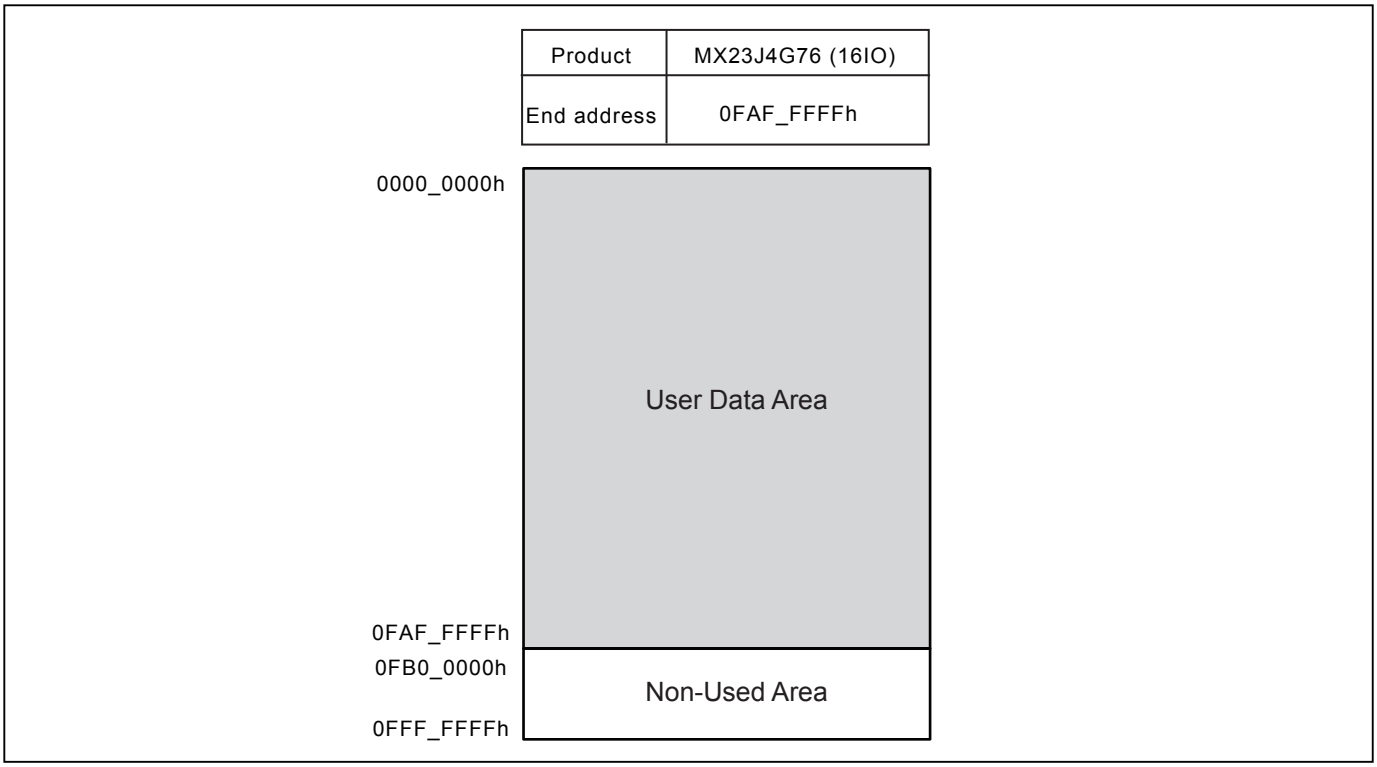
Symbol	Type	Pin Function
$\overline{CE}$	I	Chip Enable
IO0~IO15	I/O	Command / Address / Data Multiplexed I/O Port
$\overline{RE}$	I	Read Clock
VCC1	I	Power (3.3V)
VCC2	I	Power (3.3V, for I/O)
GND1	I	Ground
GND2	I	Ground (for I/O)
NC (Note 3)		All pins = Connected to Floating
		All pins = Connected to GND
R/$\overline{B}$	OD	Ready/Busy output pin (Note 1)
$\overline{RES}$	I	RESET (Low Active)
TEST	I	Test Pin (Note 2)

Note 1 : R/$\overline{B}$ (2 pins)=connected in PC board.
R/$\overline{B}$ open drain.
Note 2 : TEST pin can be connected to GND, VCC or Open.
Note 3 : All NC pins = Connected to Floating
or All NC pins = Connected to GND

6. BLOCK DIAGRAM



7. MEMORY AREA



8. ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	V_{IN}	-0.5V to 4.6V
Ambient Operating Temperature	Topr	0°C to 85°C
Storage Temperature	Tstg	-55°C to 125°C

9. DC CHARACTERISTICS

Table 1. DC Characteristics (T_{opr} = 0~85°C, VCC = 3.0~3.6V)

Item	Symbol	Test Conditions	Min.	Max.	Unit
Input High Voltage	V_{IH}	-	2	V_{CC}+0.5V	V
Input Low Voltage	V_{IL}	-	-0.5	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -400uA	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	0.4	V
Operating Current *	I_{CC}	$\overline{CE}$ = V_{IL}, I_{OUT} = 0mA, t_{CS} = 100ns, t_{CH} = 100ns, t_{CEPH} = 100ns, t_{CYC} = 50ns, t_{WH} = 25ns, t_{WL} = 25ns	-	120	mA
Standby Current (CMOS)	I_{STB}	$\overline{CE}$ = V_{CC} - 0.2V, IO=Hi-z, $\overline{RE}$ = V_{CC} - 0.2V	-	200	uA
Input Leakage Current	I_{LI}	V_{IN} = 0 to V_{CC}(max)	-	±10	uA
Output Leakage Current	I_{LO}	V_{OUT} = 0 to V_{CC}(max)	-	±10	uA

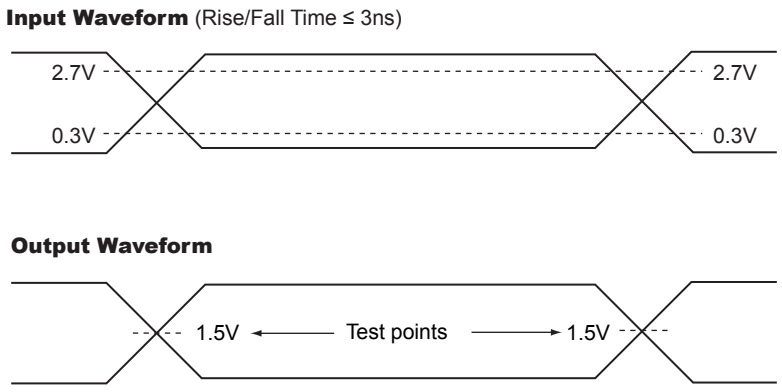
* note: output load : 30pF
* Recommended Operation Condition, Vcc Rise Time 30mV/mS

10. AC CHARACTERISTICS

Table 2. AC TEST CONDITION

Parameter	Test Condition
Input Pulse Level	0.3V to 2.7V
Input Rise and Fall Times	3ns
Output Timing Levels	1.5V/1.5V
Output Load	90uA + 30pF

AC Test Conditions



Input Pulse Levels : 0.3V to 2.7V

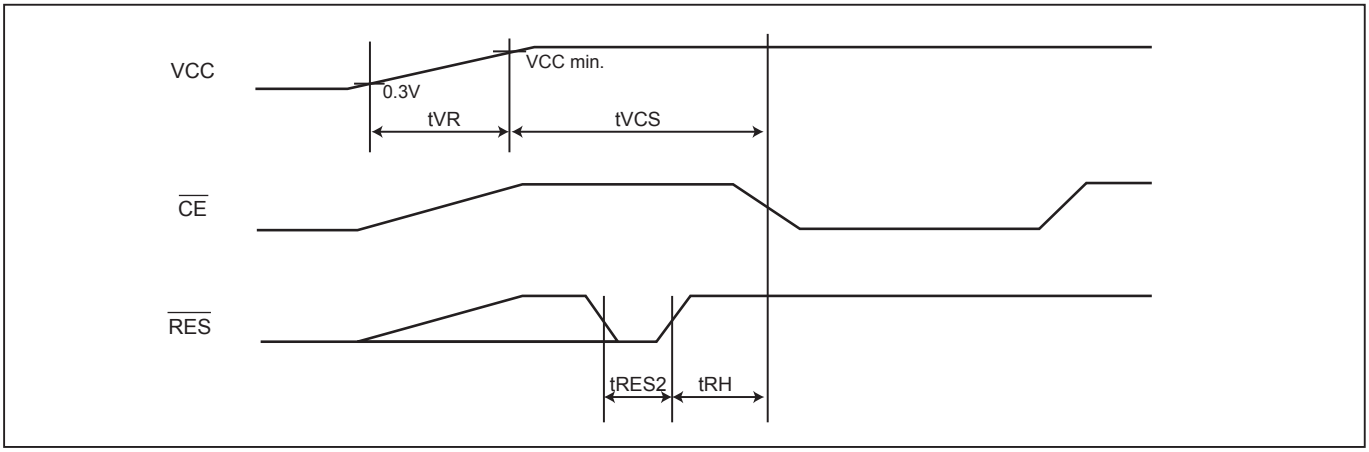
Output Load : 90uA + 30pF

Table 3. AC Characteristics for Command Input (T_{opr} = 0~85°C, VCC = 3.0~3.6V)

Parameter	Symbol	Min.	Unit
$\overline{CE}$ Setup Time	t_{CS}	50	ns
$\overline{CE}$ Hold Time	t_{CH}	50	ns
$\overline{CE}$ High Pulse Width	t_{CEPH}	100	ns
Data-in Setup Time	t_{DIS}	5	ns
Data-in Hold Time	t_{DIH}	5	ns
Data-out Hold Time *	t_{DOH}	10	ns
Read cycle time	t_{CYC}	40	ns
$\overline{RE}$ High Pulse Width	t_{WH}	16	ns
$\overline{RE}$ Low Pulse Width	t_{WL}	20	ns
Ready to $\overline{RE}$ low	t_{RR}	20	ns
$\overline{RES}$ Low Pulse Width	t_{RES}	100	ns
$\overline{RES}$ High Time Before Read	t_{RH}	1	ms

* $\overline{RES}$ filter glitch which pulse width is less than 5ns.

POR SEQUENCE



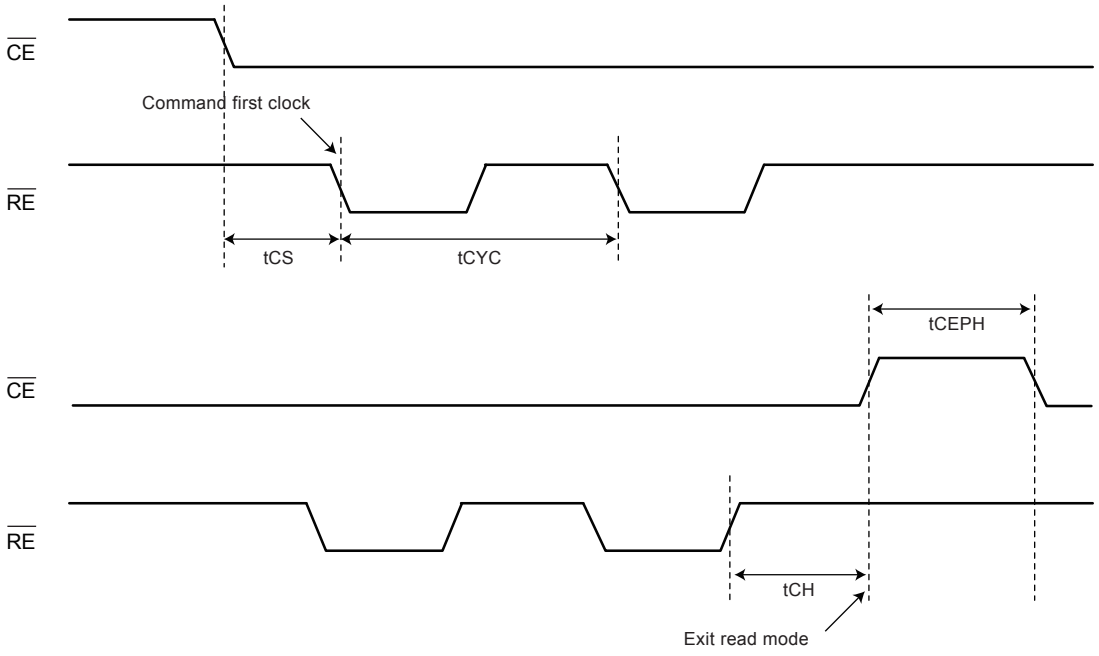
POR Timing Waveform

Symbol	Parameter	Min.	Max.	Unit
tVR	VCC Rise Time	50	500000	us/V
tR	Input Signal Rise Time		20	us/V
tF	Input Signal Fall Time		20	us/V
tVCS	VCC Setup Time	2		ms
tRES2	$\overline{RES}$ Low Time 2	100		ns
tRH	$\overline{RES}$ High Time Before Read	1		ms

Table 4. AC Characteristics for Data Output (T_{opr} = 0~85°C, VCC = 3.0~3.6V)

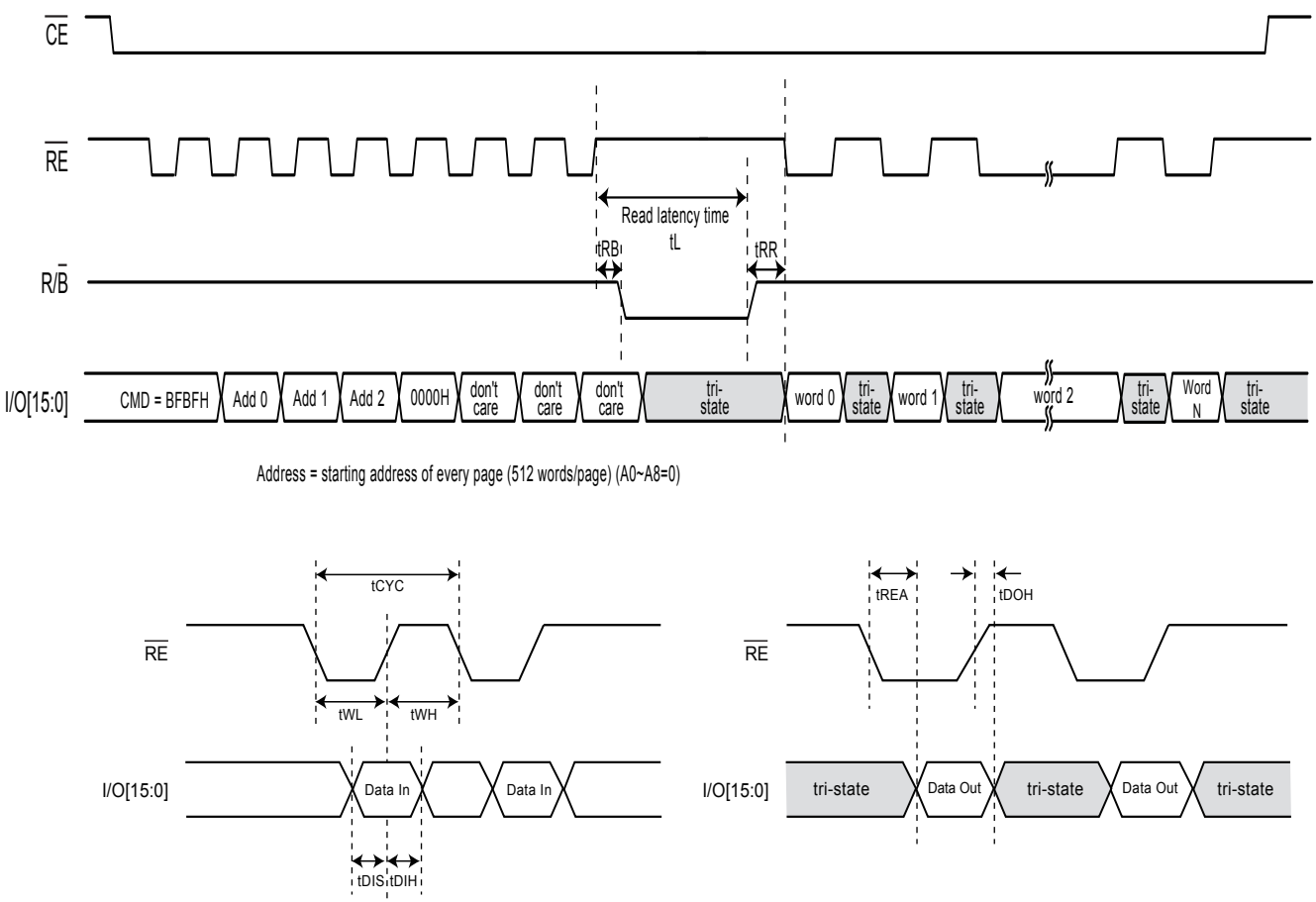
Parameter	Symbol	Min.	Max.	Unit
Read Latency Time *1	t_L	-	15	us
RE Access Time	t_{REA}	-	18	ns
RE High to Busy	t_{RB}	-	250*2	ns

Note: *1 The read latency will only be needed at the first page read.
*2 tRB=250ns max. including Tf at 10Kohm pull-up condition.



* $\overline{CE}$ must be keep in low during page read

AC Timing Condition



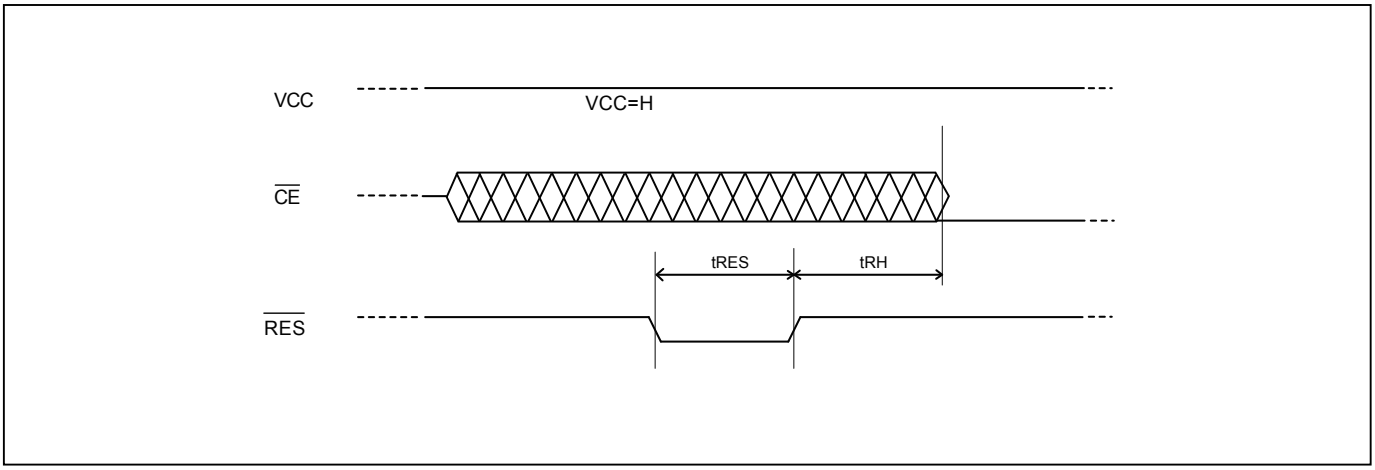
Data-in:
* Command/address data-in are latched by rising edge of $\overline{RE}$.
* Data out is triggered by falling edge of $\overline{RE}$.
* Data out is continued to next page automatically with sustained $\overline{RE}$.
* Read operation can be interrupted by $\overline{CE}$ going to high.

Command Input and Data Output Timing Waveform

Table 5. Read Command Definitions

Command	Bus cycles	1st bus cycle	2nd bus cycle	3rd bus cycle	4th bus cycle	5th bus cycle	6th bus cycle	7th bus cycle	8th bus cycle
		command	address	address	address	address	address	address	address
Read Mode	8	BFBFH	Addr0	Addr1	Addr2	0000H	don't care	don't care	don't care

Addr0 : A24~A27 (IO0/8=A24, IO1/9=A25, IO2/10=A26, IO3/11=A27)
Addr1 : A16~A23 (IO0/8=A16, IO1/9=A17, IO2/10=A18, IO3/11=A19, IO4/12=A20, IO5/13=A21, IO6/14=A22, IO7/15=A23)
Addr2 : A8~A15 (IO0/8=A8, IO1/9=A9, IO2/10=A10, IO3/11=A11, IO4/12=A12, IO5/13=A13, IO6/14=A14, IO7/15=A15)
Note : The starting address of every page (A8~A0) is 0, Each page has 512 words

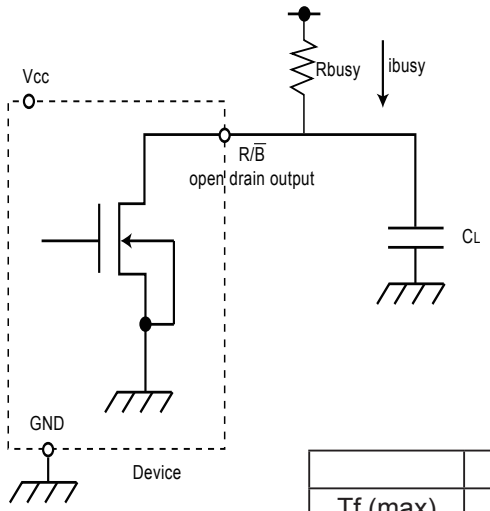


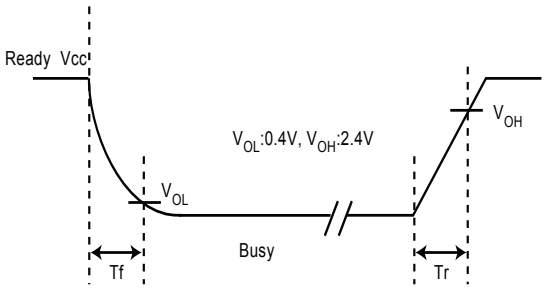
RES Timing Waveform

READY/$\overline{BUSY}$

The device has a R/$\overline{B}$ output that provides a hardware method of indicating the device is ready for read. The R/$\overline{B}$ is normally high but transitions to low after read command is issued. It returns to high when the internal controller has finish the read operation.

The pin is an open-drain driver thereby allowing two or more R/$\overline{B}$ outputs to be Or-tied. A5KΩ ~ 50KΩ pull-up resistor is required to allow R/$\overline{B}$ to transition high indicating the device is ready for read.



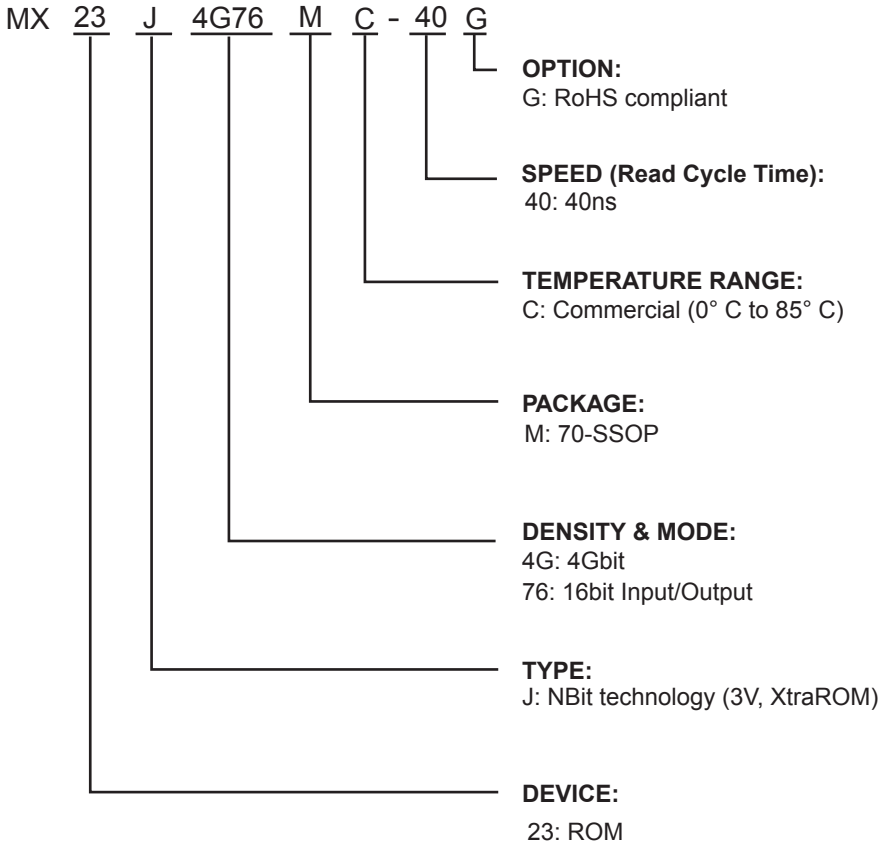


	5K	10K	100K
Tf (max)	450 ns	200 ns	200 ns
Tr (max)	1.5 us	2.5 us	7.5 us

* Data is based on C_L=30PF + 8 R/$\overline{B}$ pad, every R/$\overline{B}$ pin loading is 2.5PF.

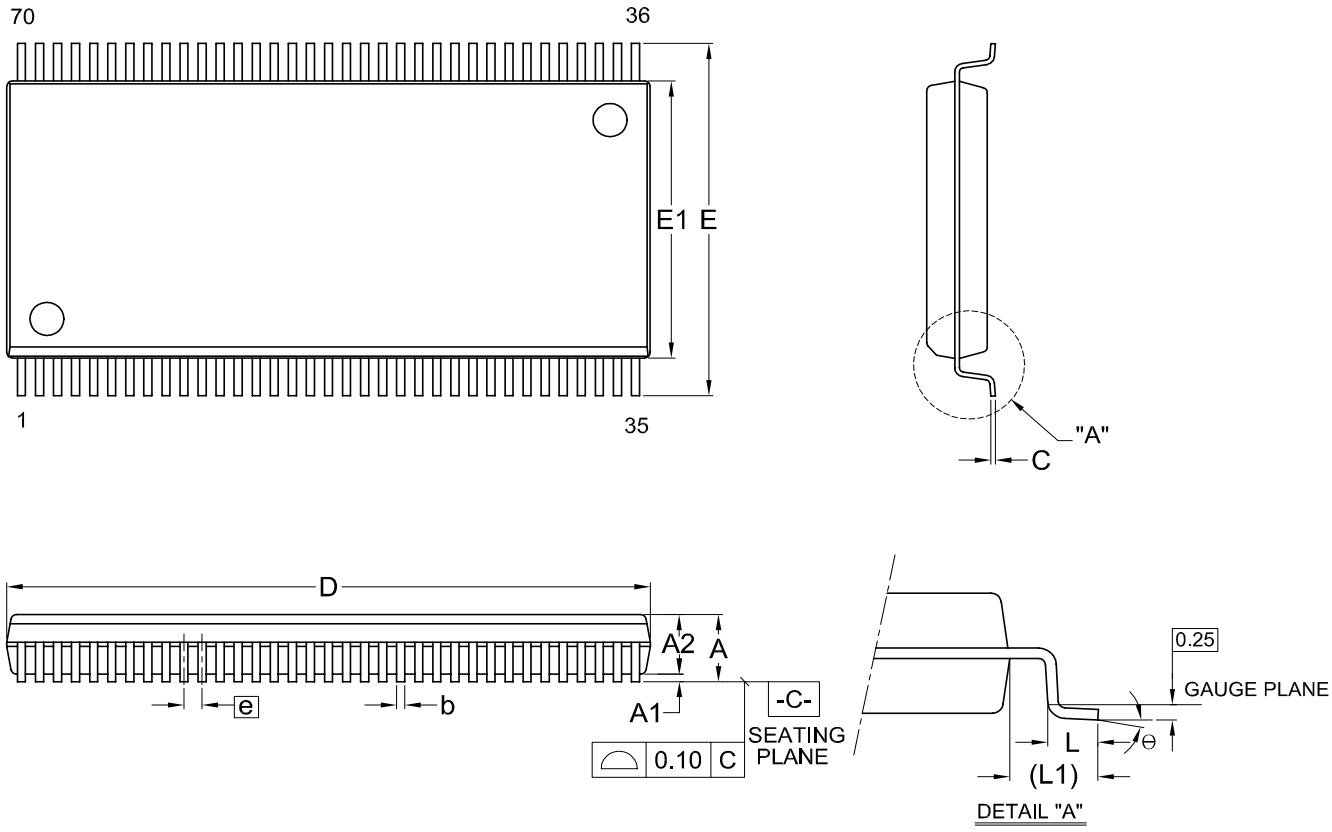
Note:
1. Rbusy must be higher than 5KΩ.
2. A schmitt trigger is suggested to provide on the user input port due to the slow slew rate of the tr and tf.

11. PART NAME DESCRIPTION



12. PACKAGE INFORMATION

Doc. Title: Package Outline for SSOP 70L (500MIL)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	Θ
mm	Min.	---	0.10	2.56	0.30	0.17	28.37	15.73	12.47	---	0.61	1.51	0
	Nom.	---	0.15	2.69	0.35	0.20	28.50	16.03	12.60	0.80	0.81	1.71	5
	Max.	3.05	0.23	2.82	0.43	0.25	28.63	16.33	12.73	---	1.01	1.91	10
Inch	Min.	---	0.004	0.101	0.012	0.007	1.117	0.619	0.491	---	0.024	0.060	0
	Nom.	---	0.006	0.106	0.014	0.008	1.122	0.631	0.496	0.031	0.032	0.068	5
	Max.	0.120	0.009	0.111	0.017	0.010	1.127	0.643	0.501	---	0.040	0.075	10

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1503	8	MO-174			

REVISION HISTORY

Revision No.	Description	Page	Date
0.01	1. Modified Addr0 of Table 5. Read Command Definitions	P6	NOV/18/2010
0.02	1. Added "MEMORY AREA"	P2	MAR/11/2011
0.03	1. Modified PIN CONFIGURATIONS of 70SSOP	P1	MAY/16/2011
1.0	1. Removed "ADVANCED INFORMATION"	P1	NOV/01/2011
1.1	1. Added POR SEQUENCE	P5	MAY/08/2012
	2. Added Part Name Description	P10	
	3. Modified NC1 pin (pin 26, 61) as TEST pin NC1 pin (pin 20, 55) as NC pin	P1	
	4. Modified AC Test Conditions	P4	
	5. Modified table 2 from "Input and Output Timing Levels" to "Output Timing Levels"	P4	
	6. Added note *2 for tRB	P6	

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