

64M-BIT PAGE MODE MASK ROM

FEATURES

- Bit organization
 - 8M x 8 (byte mode)
 - 4M x 16 (word mode)
- Fast access time
 - Random access:70ns (max.)
 - Page access:25ns (max.)
- Page size
 - 8 words per page
- Current
 - Operating:20mA
 - Standby:15uA
- Supply voltage
 - 2.7V ~ 3.6V
- Package
 - 48 pin TSOP (12mm x 20mm)
- Temperature
 - 0°C ~ 70°C
- Process
 - 0.18um

PIN DESCRIPTION

Symbol	Pin Function
A0~A21	Address Inputs
D0~D14	Data Outputs
D15/A-1	D15 (Word Mode)/ LSB Address (Byte Mode)
CE#	Chip Enable Input
OE#	Output Enable Input
BYTE#	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

PIN CONFIGURATION

48 TSOP (Top View)



ORDER INFORMATION

Part No.	Speed	Package	Grade	Remark
MX23L6410ATC-70	70ns	48 pin TSOP	Commercial	
MX23L6410ATC-90	90ns	48 pin TSOP	Commercial	
MX23L6410ATC-70G	70ns	48 pin TSOP	Commercial	Pb-free
MX23L6410ATC-90G	90ns	48 pin TSOP	Commercial	Pb-free

MODE SELECTION

CE#	OE#	Byte#	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.3V to 3.9V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -400uA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	0.7xVCC	VCC+0.3	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current	ICC	-	20mA	f=5MHz, CE#=VIL, OE#=VIH all output open
Standby Current (CMOS)	ISTB	-	15uA	CE#>VCC-0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 2.7V~3.6V)

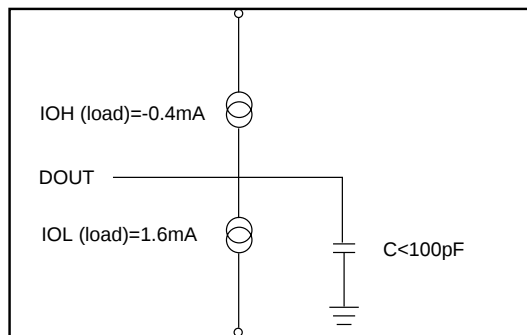
Item	Symbol	<u>23L6410A-70</u>		<u>23L6410A-90</u>	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	70ns	-	90ns	-
Address Access Time	tAA	-	70ns	-	90ns
Chip Enable Access Time	tCE	-	70ns	-	90ns
Page Access Time	tPA	-	25ns	-	25ns
Output Enable Time	tOE	-	25ns	-	25ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note:

1. Output high-impedance delay (tHZ) is measured from OE# or CE# going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5ns
Input Timing Level	1.5V
Output Timing Level	1.5V
Output Load	See Figure



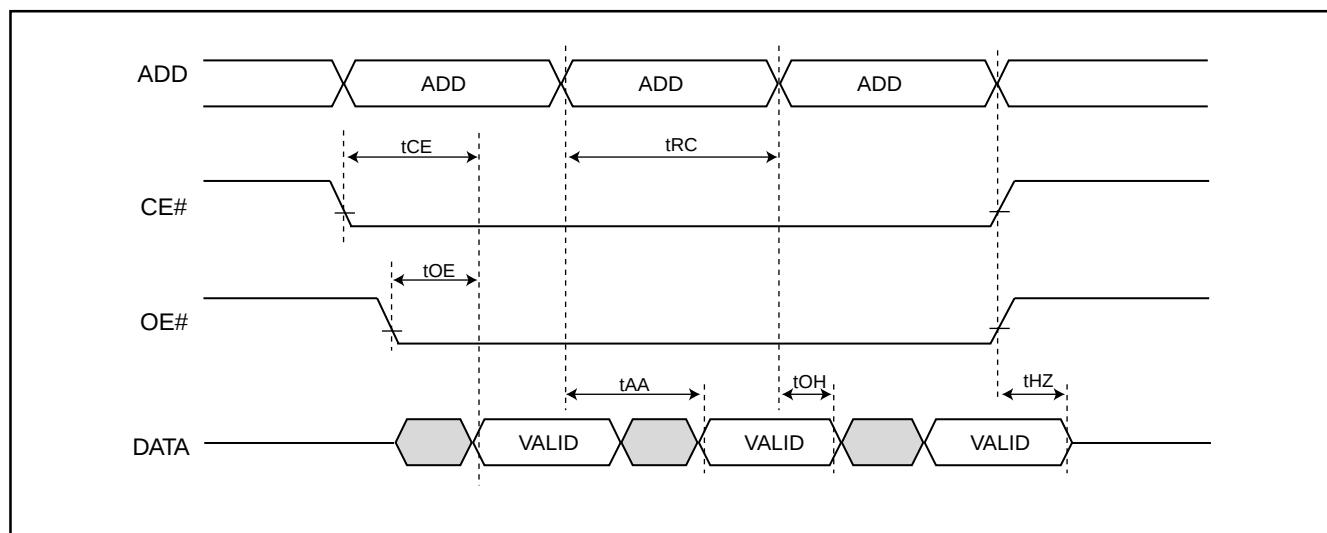
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

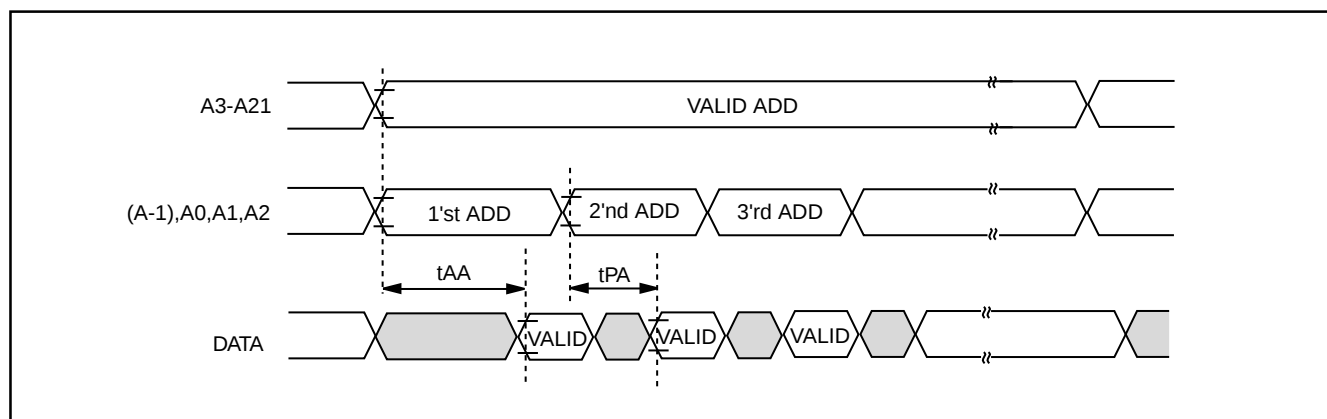
Output loading capacitance includes load board's and all stray capacitance.

TIMING DIAGRAM

RANDOM READ

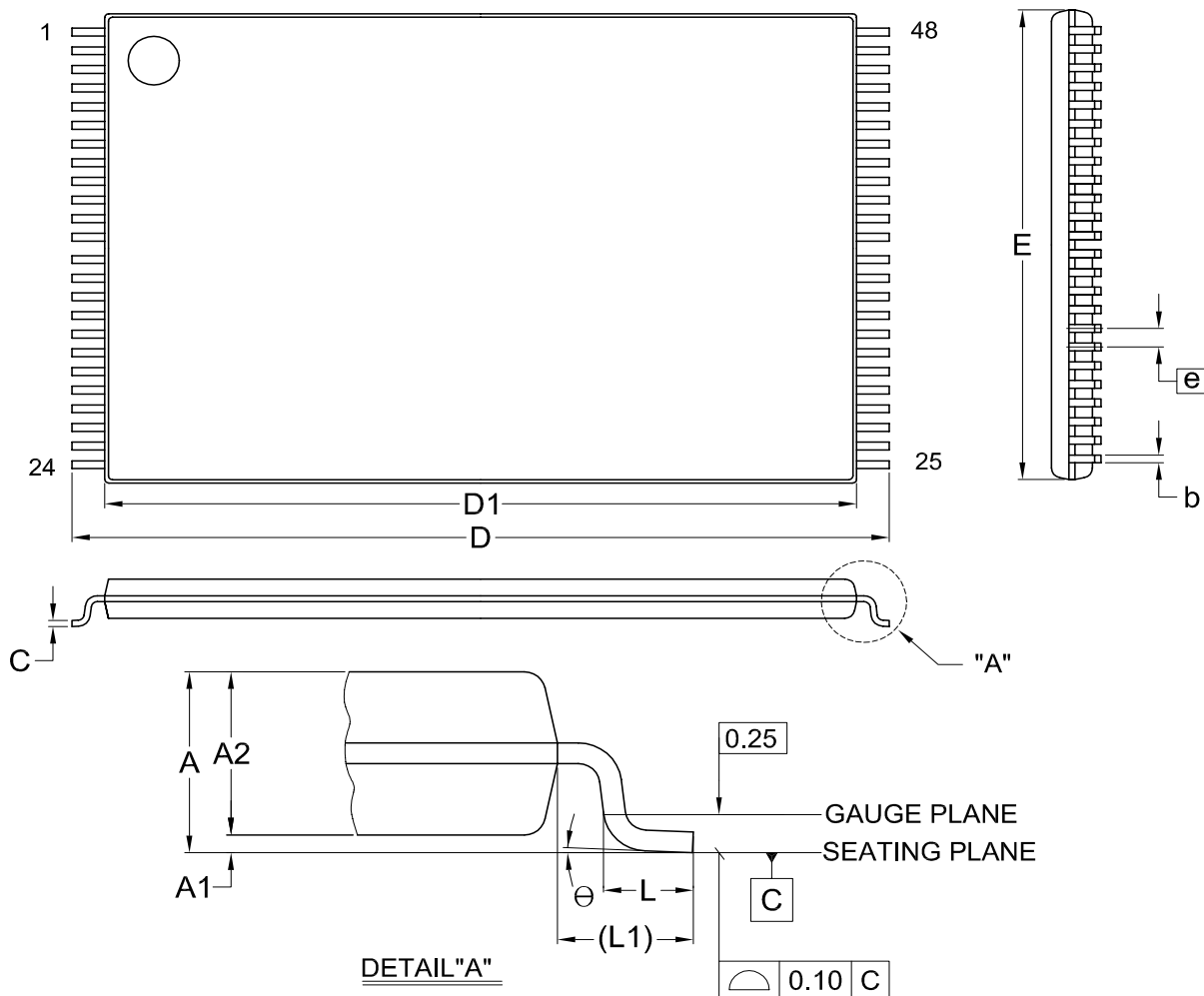


PAGE READ



PACKAGE INFORMATION

Title: Package Outline for TSOP(I) 48L (12X20mm)NORMAL FORM



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
UNIT	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	11.90	---	0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.13	20.00	18.40	12.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	12.10	---	0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.469	---	0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.472	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.476	---	0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1607	8	MO-142			2007/08/03



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REVISION HISTORY

Revision #	Description	Page	Date
1.1	1. Added statement	P8	NOV/07/2006
1.2	1. Removed 44-SOP package information	P1	JAN/10/2007



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