



MX23L6422

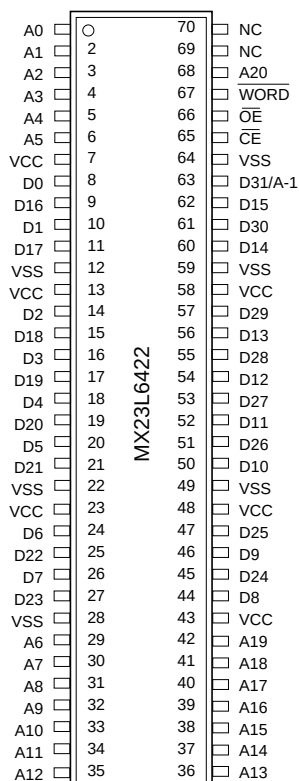
3.3 Volt 64M-BIT (4M x 16 / 2M x 32) Mask ROM with Page Mode

FEATURES

- Bit organization
 - 4M x 16 (byte mode)
 - 2M x 32 (double word mode)
- Fast access time
 - Random access: 110ns (max.) for 3.15~3.6V
120ns (max.) for 3.0~3.6V
 - Page access: 30ns (max.)
- Page Size
 - 8 double words per page
- Current
 - Operating: 60mA (max.)
 - Standby: 20uA (max.)
- Supply voltage
 - 3.3V±10%
- Package
 - 70 pin SSOP
 - 100 pin TQFP (14mm x 14mm)
 - 86 pin TSOP(2)

PIN CONFIGURATION

70 SSOP



ORDER INFORMATION

Part No.	Access Time	Page Access Time	Package
MX23L6422MC-11	110ns	30ns	70 pin SSOP
MX23L6422MC-12	120ns	50ns	70 pin SSOP
MX23L6422VC-11	110ns	30ns	100 pin TQFP
MX23L6422VC-12	120ns	50ns	100 pin TQFP
MX23L6422YC-12	120ns	50ns	86 pin TSOP

PIN DESCRIPTION

Symbol	Pin Function
A0~A20	Address Inputs
D0~D30	Data Outputs
D31/A-1	D31 (Double Word Mode)/ LSB Address (Word Mode)
CE	Chip Enable Input
OE	Output Enable Input
Word	Double Word/ Word Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

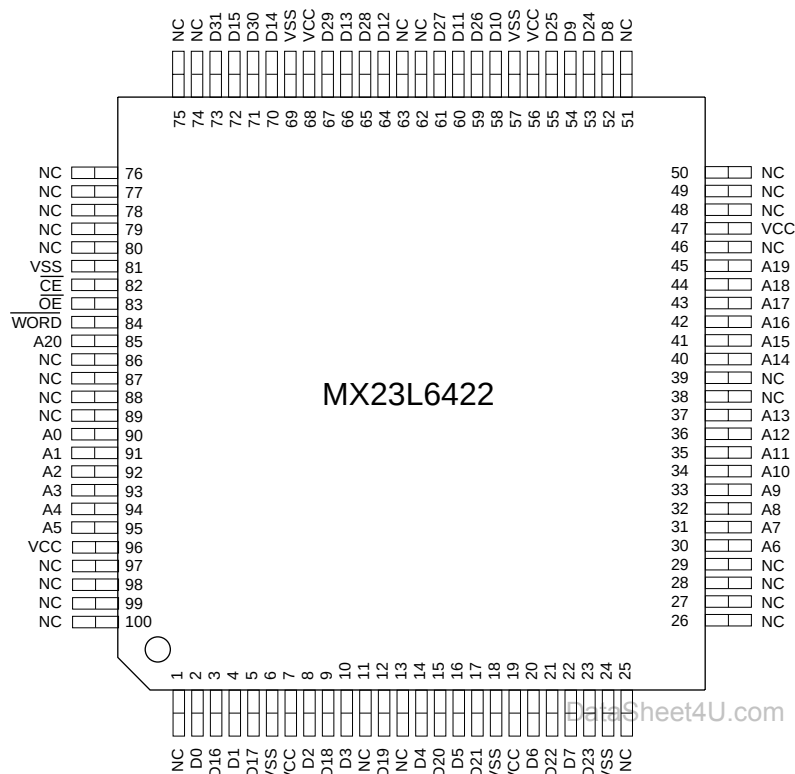
MODE SELECTION

CE	OE	Word	D31/A-1	D0~D15	D16~D31	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D15	D16~D31	Double Word	Active
L	L	L	Input	D0~D15	High Z	Word	Active

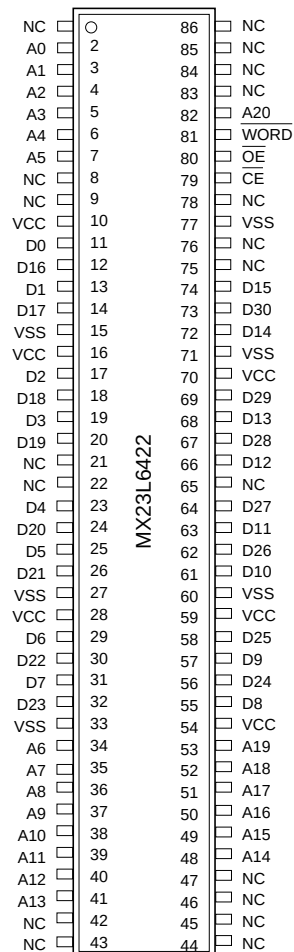


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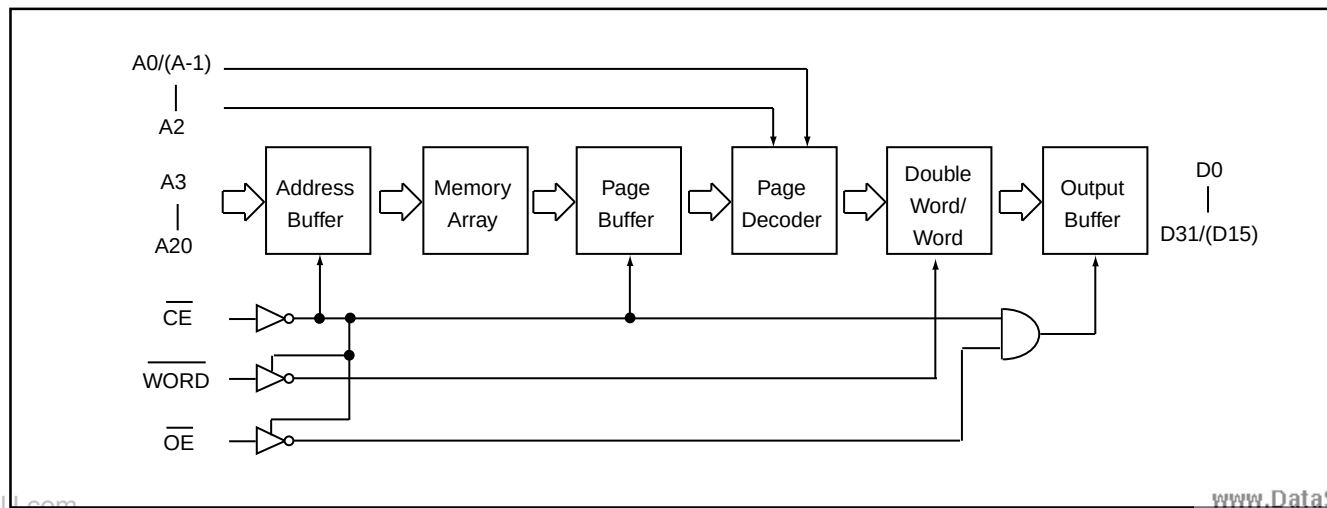
100TQFP



86TSOP(2)



BLOCK DIAGRAM





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ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-1.3V to 4.1V
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -1.3V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

DC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	10uA	0V, VCC
Output Leakage Current	ILO	-	10uA	0V, VCC
Operating Current	ICC1	-	60mA	tRC = 110ns, all output open, with normal sequential access testing pattern
Standby Current (TTL)	ISTB1	-	1mA	$\overline{CE} = VIH$
Standby Current (CMOS)	ISTB2	-	20uA	$\overline{CE} > VCC - 0.2V$
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ



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AC CHARACTERISTICS (Ta = 0 °C ~ 70 °C, VCC = 3.3V±10%)

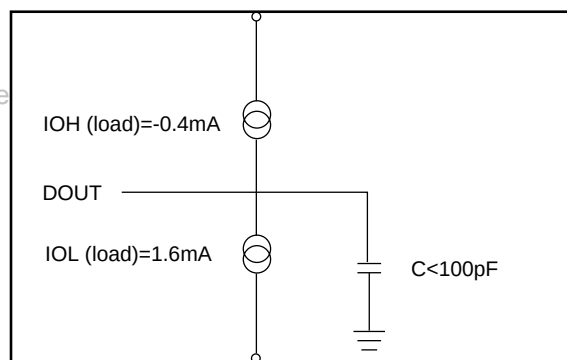
Item	Symbol	23L6422-11*		23L6422-12	
		MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	110ns	-	120ns	-
Address Access Time	tAA	-	100ns	-	120ns
Chip Enable Access Time	tACE	-	110ns	-	120ns
Page Mode Access Time	tPA	-	30ns	-	50ns
Output Enable Time	tOE	-	30ns	-	50ns
Output Hold After Address	tOH	0ns	-	0ns	-
Output High Z Delay	tHZ	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

* 110ns for 3.15~3.6V

AC Test Conditions

Input Pulse Levels	0.4V~ 2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

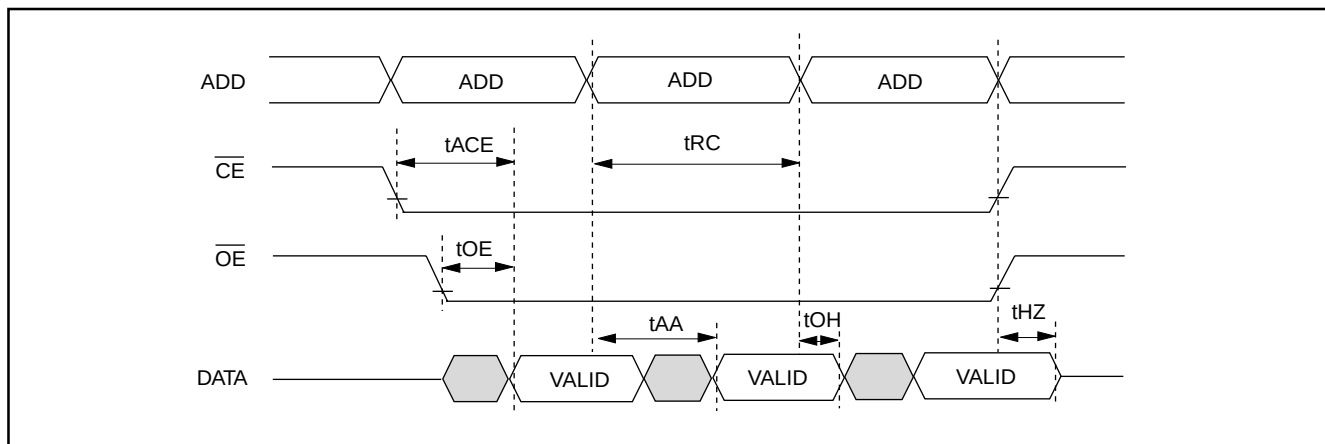
Output loading capacitance includes load board's and all stray capacitance.



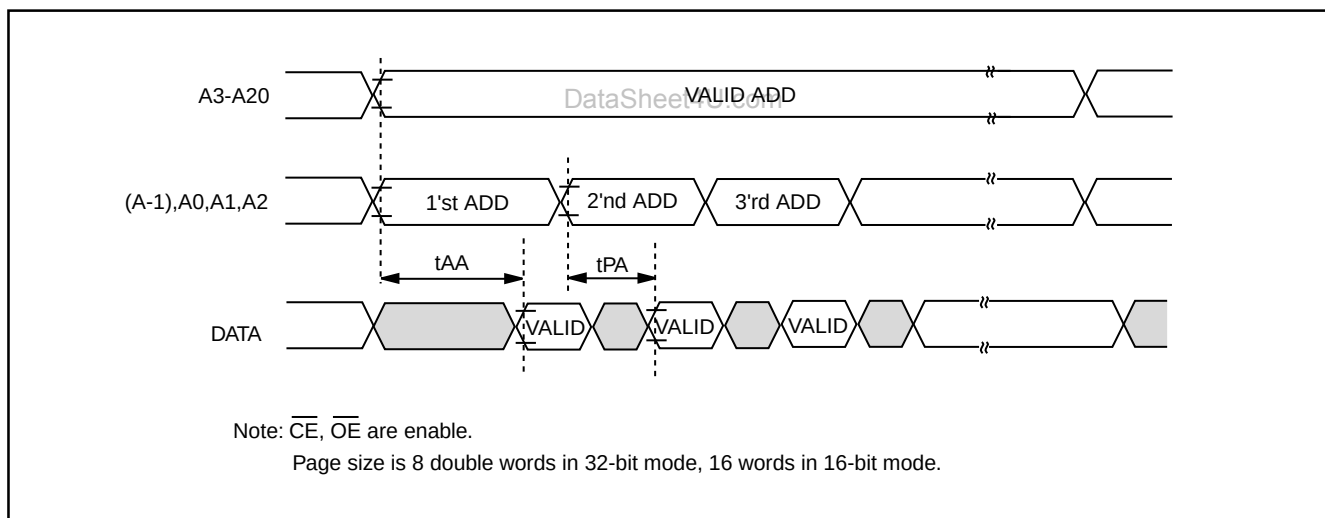
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TIMING DIAGRAM

RANDOM READ



PAGE READ



**MX23L6422****REVISION HISTORY**

REVISION	DESCRIPTION	PAGE	DATE
2.1	AC CHARACTERISTICS tOH 10ns-->0ns	P4	JAN/29/1999
2.2	Add new 86pin TSOP(2) package	P1	APR/09/1999
	Add 100ns speed grade	P1,2	
	Delete 115ns speed grade	P4	
2.3	Change 100ns speed grade to 110ns	P4	SEP/14/1999
2.4	Add 110ns(max.) for 3.15~3.6V ; 120ns(max.) for 3.0~3.6V	P1	DEC/29/1999
2.5	Modify Operating Current : 40mA-->60mA	P1,3	JAN/13/2000

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MACRONIX INTERNATIONAL Co., LTD.

HEADQUARTERS:

TEL: +886-3-578-6688

FAX: +886-3-563-2888

EUROPE OFFICE:

TEL: +32-2-456-8020

FAX: +32-2-456-8021

JAPAN OFFICE:

TEL: +81-44-246-9100

FAX: +81-44-246-9105

SINGAPORE OFFICE:

TEL: +65-348-8385

FAX: +65-348-8096

TAIPEI OFFICE:

TEL: +886-2-509-3300

FAX: +886-2-509-2200

MACRONIX AMERICA, INC.

TEL: +1-408-453-8088

FAX: +1-408-453-8488

CHICAGO OFFICE:

TEL: +1-847-963-1900

FAX: +1-847-963-1909

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