64M-BIT [64M x 1] CMOS SERIAL MASK-ROM

FEATURES

GENERAL

- 67,108,864 x 1 bit structure
- Single Power Supply Operation
  - 3.0 to 3.6 volt for read operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  - Fast access time: 25MHz serial clock (50pF + 1TTL Load)
- Low Power Consumption
  - Low active read current: 10mA (typical) at 25MHz
  - Low standby current: 30uA (typical, CMOS)

**** 6MHz for Die Form only***

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code, 3-byte address, 1-byte byte address

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI Input
  - Serial Data Input
- SO Output
  - Serial Data Output
- PACKAGE
  - 28-pin SOP (330mil)

GENERAL DESCRIPTION

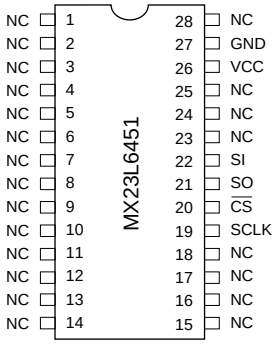
The MX23L6451 is a CMOS 67,108,864 bit serial Mask ROM, which is configured as 8,388,608 x 8 internally. The MX23L6451 features a serial peripheral interface and software protocol allowing operation on a simple 3- wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial peripheral interface access to the device is enabled by $\overline{CS}$ input.

The MX23L6451 provides sequential read operation on the whole chip.

When the device is not in operation and $\overline{CS}$ is high, it is put in standby mode and draws less than 30uA DC current.

PIN CONFIGURATIONS

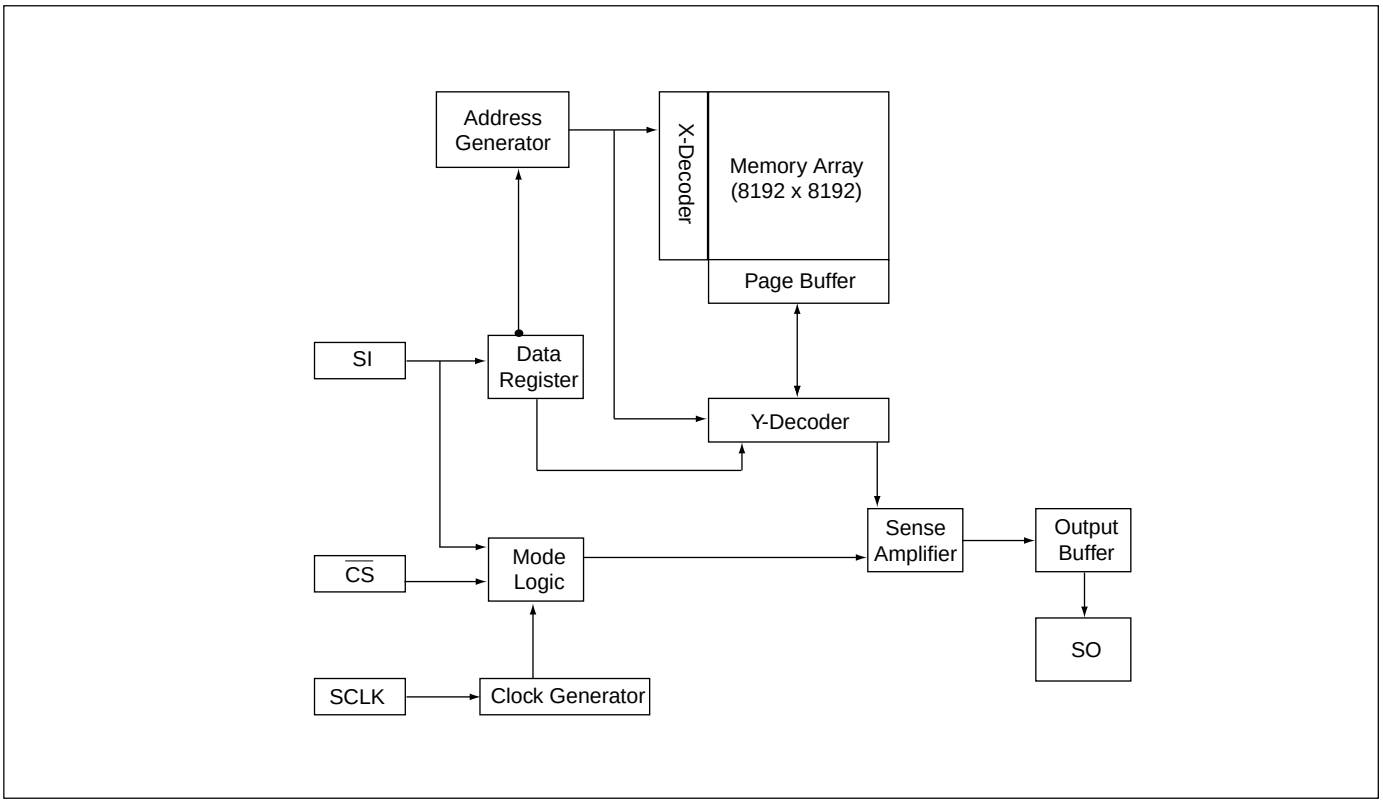
28-PIN SOP (330 mil)



PIN DESCRIPTION

SYMBOL	DESCRIPTION
$\overline{CS}$	Chip Select
SI	Serial Data Input
SO	Serial Data Output
SCLK	Clock Input
VCC	+ 3.3V Power Supply
GND	Ground
NC	No Internal Connection

BLOCK DIAGRAM



ORDER INFORMATION

Part No.	Access Time	Package	Remark
MX23L6451MC-40G	40ns	28 pin SOP	Pb-free
MX23L6451HC-15	150ns	Die	

COMMAND DEFINITION

Command	Read Array (byte)
1st	52H
2nd	AD1
3rd	AD2
4th	AD3
5th	BA
6th	X
7th	X
8th	X
9th	X
Action	n bytes read out until $\overline{CS}$ goes high

Note:
1.X is dummy cycle and is necessary
2.AD1 to AD3 are address input data
3.BA is byte address

1-byte command code								
	Bit7(MSB)	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3-byte address(0 to 1FFFH)								
AD1:	X	X	A22	A21	A20	A19	A18	A17
AD2:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:	X	X	X	X	X	X	A8	A7
1-byte byte address(0 to 7FH)								
BA:	X	A6	A5	A4	A3	A2	A1	A0

DEVICE OPERATION

1.When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next CS falling edge. In standby mode, SO pin of this LSI should be High-Z.
2.When correct command is inputted to this LSI, this LSI becomes active mode and keeps the active mode until next CSB rising edge.

COMMAND DESCRIPTION

(1) Read Array

This command is sent with the 4-byte address (command included), and the byte address, followed by four dummy bytes sent to give the device time to stabilize. The device will then send out data starting at the byte address until CS goes high. The clock to clock out the data is supplied by the master serial interface. The read operation is executed on a segment (512 bytes) basis. If the end of the segment is reached then the device will wrap around to the beginning of the next segment with no delays incurred during the segment boundary crossover. As with crossing over segment boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

(2) Standby Mode

When CS is high and there is no operation in progress, the device is put in standby mode. Typical standby current is less than 30uA.

DATA SEQUENCE

Output data is serially sent out through SO pin, synchronized with the rising edge of SCLK, whereas input data is serially read in through SI pin, synchronized with the rising edge of SCLK. The bit sequence for both input and output data is bit 7 (MSB) first, then bit 6, bit 5, ..., and bit 0.(LSB)

ADDRESS SEQUENCE

The address assignment is described as follows :

BA: Byte address Bit sequence:	X	A6	A5	A4	A3	A2	A1	A0
AD1:First Address Bit sequence:	X	X	A22	A21	A20	A19	A18	A17
AD2:Second Address Bit sequence:	A16	A15	A14	A13	A12	A11	A10	A9
AD3:Thrid Address Bit sequence:	X	X	X	X	X	X	A8	A7

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-55°C to 125°C
Applied Input Voltage	-0.5V to 4.6V
Applied Output Voltage	-0.5V to 4.6V
VCC to Ground Potential	-0.5V to 4.6V

NOTICE:

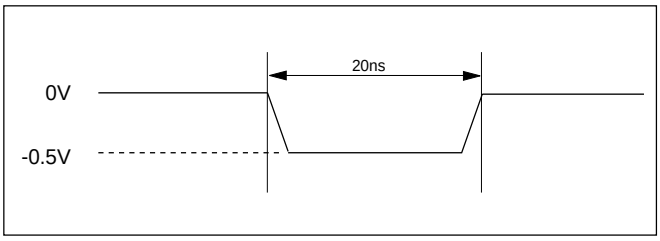
1.Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

2.Specifications contained within the following tables are subject to change.

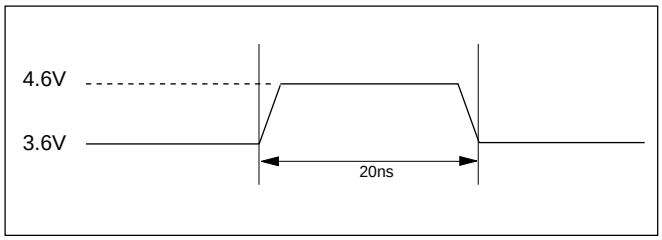
3.During voltage transitions, all pins may overshoot to 4.6V or -0.5V for period up to 20ns.

4.All input and output pins may overshoot to VCC+0.5V while VCC+0.5V is smaller than or equal to 4.6V.

Maximum Negative Overshoot Waveform



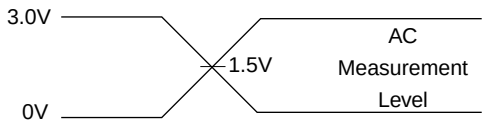
Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

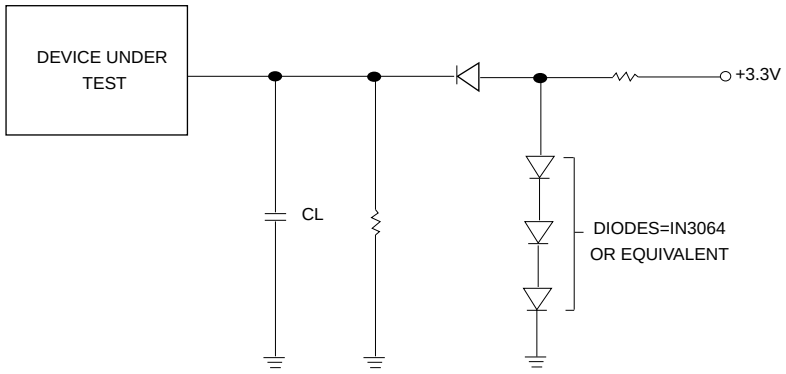
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			10	pF	VOUT = 0V

INPUT TEST WAVEFORMS AND MEASURESMENT LEVEL



Note:Input pulse rise and fall time are < 10ns

OUTPUT LOADING



CL=50pF Including jig capacitance

DC CHARACTERISTICS (Temperature = 0°C to 70°C, VCC = 3.0V ~ 3.6V)

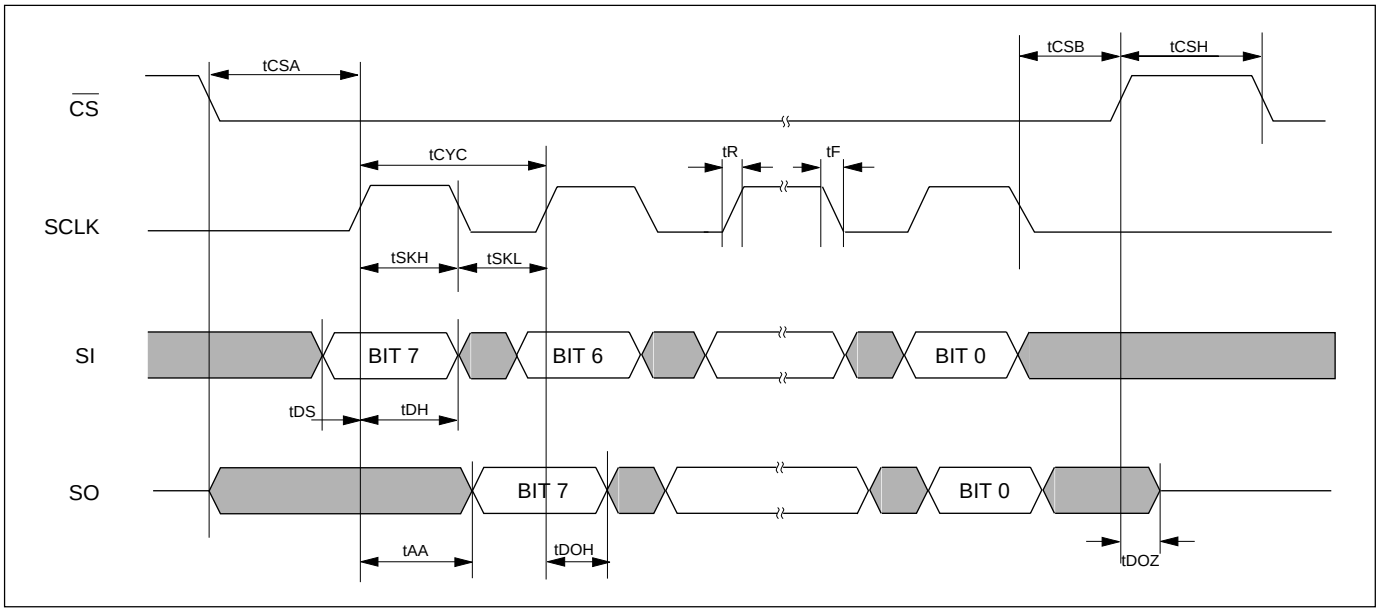
SYMBOL	PARAMETER	MIN.	TYP	MAX.	UNITS	TEST CONDITIONS
IIL	Input Load Current			±10	uA	VCC = VCC Max VIN = VCC or GND
ILO	Output Leakage Current			±10	uA	VCC = VCC Max VIN = VCC or GND
ISB1	VCC Standby Current (CMOS)			30	uA	VCC = VCC Max $\overline{CS}$ = VCC ± 0.2V
ISB2	VCC Standby Current (TTL)		1	3	mA	VCC = VCC Max $\overline{CS}$ = VIH
ICC1	VCC Read		10	30	mA	f=25MHz
VIL	Input Low Voltage	-0.5		0.8	V	
VIH	Input High Voltage	2.0		VCC+0.5	V	
VOL	Output Low Voltage			0.4	V	IOL = 500uA
VOH	Output High Voltage	2.4			V	IOH = -100uA

AC CHARACTERISTICS (Temperature = 0°C to 70°C, VCC = 3.0V ~ 3.6V)

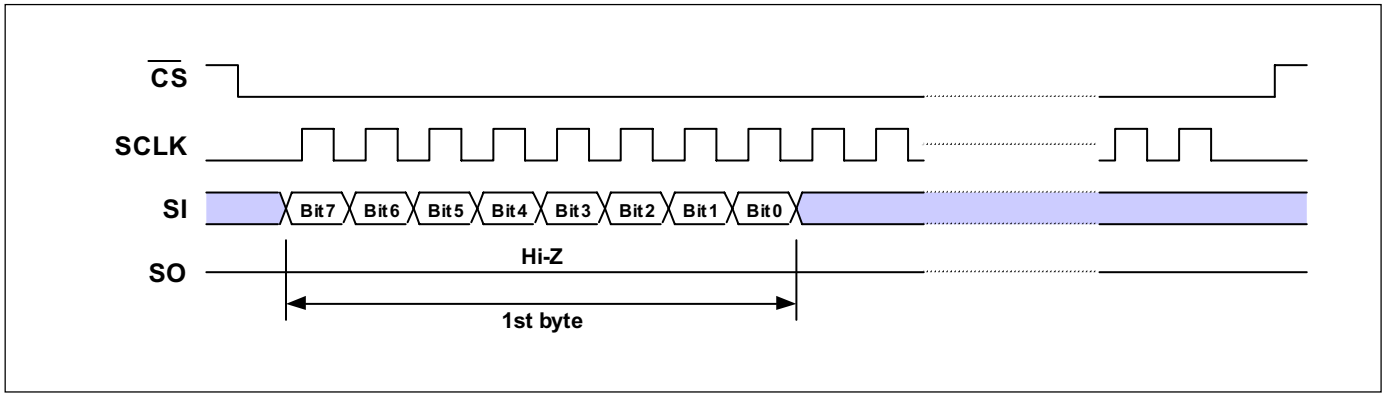
SYMBOL	PARAMETER	Min.	Typ.	Max.	Units	Conditions
fSCLK	Clock Frequency			25	MHz	
tCYC	Clock Cycle Time	40			ns	
tSKH	Clock High Time	20			ns	
tSKL	Clock Low Time	20			ns	
tR	Clock Rise Time			5	ns	
tF	Clock Fall Time			5	ns	
tCSA	$\overline{CS}$ Lead Clock Time	40			ns	
tCSB	$\overline{CS}$ Lag Clock Time	40			ns	
tCSH	$\overline{CS}$ High Time	80			ns	
tDS	SI Setup Time	5			ns	
tDH	SI Hold Time	20			ns	
tAA	Access Time			30	ns	
tDOH	SO Hold Time	5			ns	
tDOZ	SO Floating Time	0		20	ns	

NOTES:
1. Typical value is calculated by simulation.

SERIAL DATA INPUT/OUTPUT TIMING

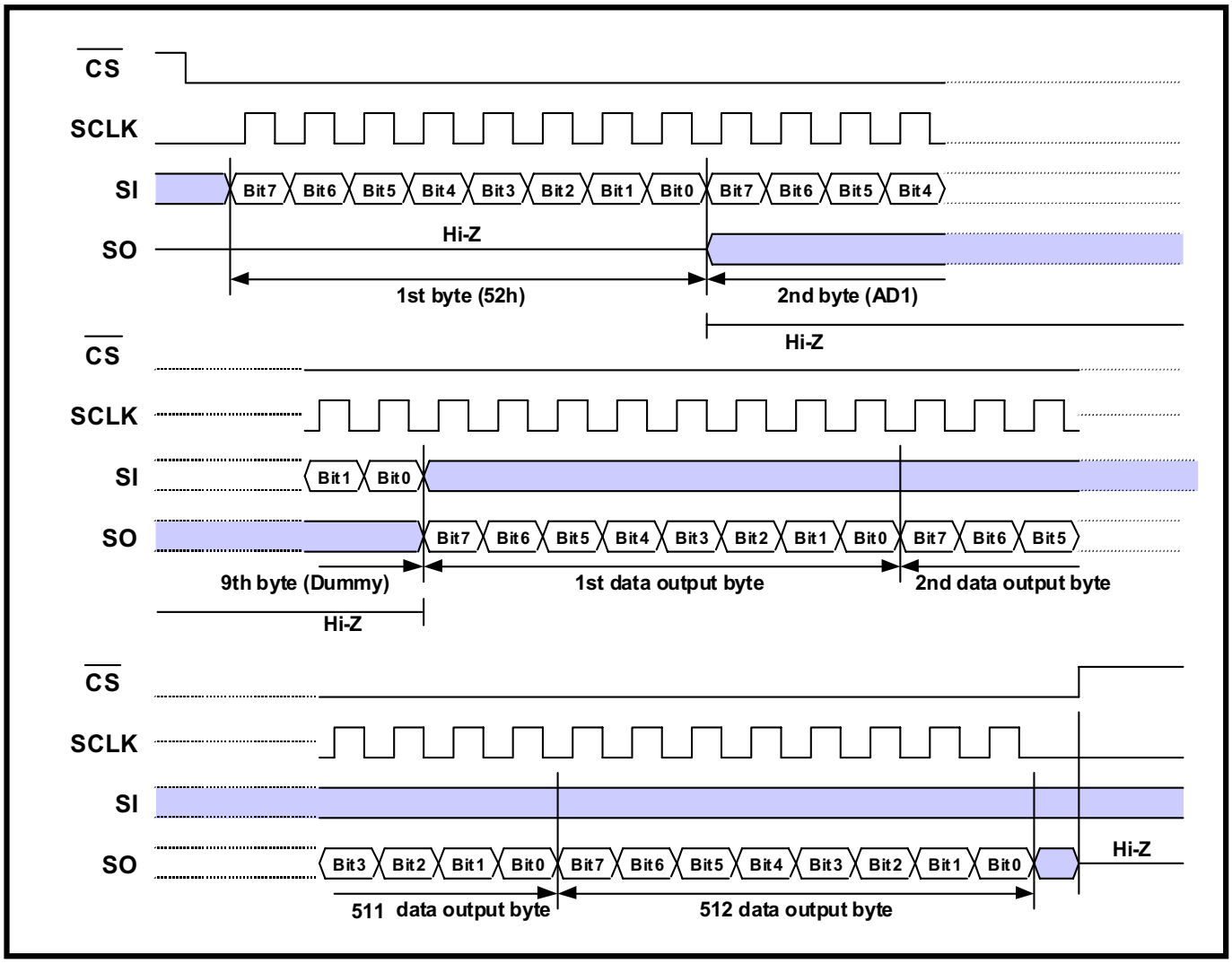


STANDBY TIMING WAVEFORM



When incorrect command is inputted to this LSI, this LSI becomes standby mode and keeps the standby mode until next $\overline{CS}$ falling edge. In standby mode, SO pin of this LSI should be High-Z. While $\overline{CS}$=VIH, current=standby current, while $\overline{CS}$=VIL and commands are issuing, or commands are invalid, current=5mA(typ.) to 15mA(max.).

READ ARRAY TIMING WAVEFORM

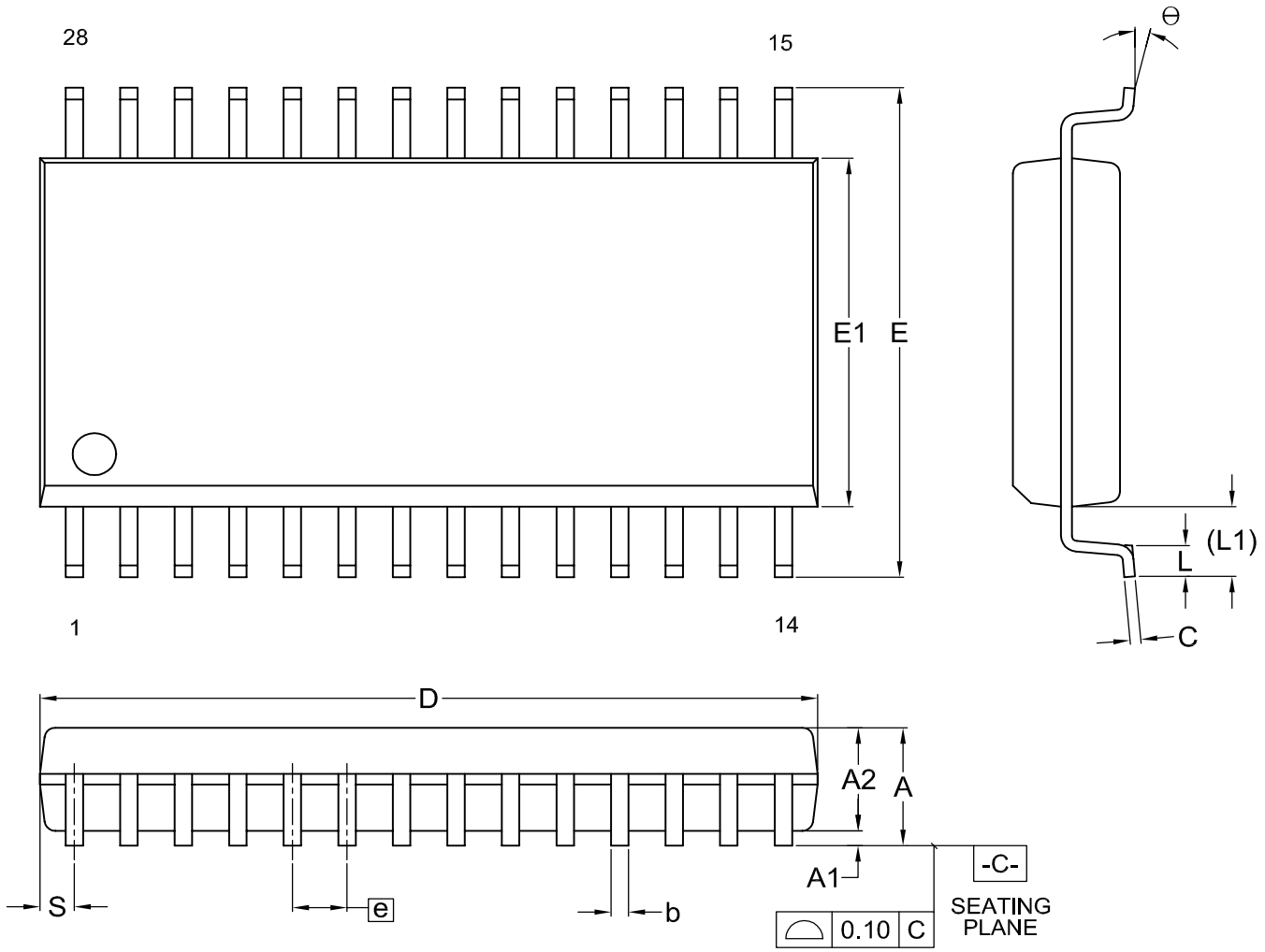


NOTES:

1. 1st Byte='52h'
2. 2nd Byte=Address 1(AD1), A17=BIT 0, A18=BIT1, A19=BIT2, A20=BIT3, A21=BIT4, A22=BIT5.
3. 3rd Byte=Address 2(AD2), A9=BIT0, A10=BIT1,.....A16=BIT7
4. 4th Byte=Address 3(AD3), A7=BIT0, A8=BIT1
5. 5th Byte=Byte Address(BA), A0=BIT0, A1=BIT1,.....A6=BIT6
6. 6th-9th Bytes for SI ==> Dummy Bytes (Don't care)
7. From Byte 10, SO Would Output Array Data

PACKAGE IMFORMATION

Title: **Package Outline for SOP 28L (330MIL)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	Θ
mm	Min.	---	0.05	2.39	0.36	0.20	17.98	11.51	8.28		0.56	1.51	0.67	0
	Nom.	---	0.20	2.49	0.41	0.25	18.11	11.81	8.40	1.27	0.76	1.71	0.80	5
	Max.	2.84	0.36	2.59	0.51	0.30	18.24	12.12	8.53		0.96	1.91	0.92	8
Inch	Min.	---	0.002	0.094	0.014	0.008	0.708	0.453	0.326		0.022	0.059	0.026	0
	Nom.	---	0.008	0.098	0.016	0.010	0.713	0.465	0.331	0.050	0.030	0.067	0.031	5
	Max.	0.112	0.014	0.102	0.020	0.012	0.718	0.477	0.336		0.038	0.075	0.036	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1403	9	MO-059			09-07-'05

REVISION HISTORY

Revision	Description	Page	Date
1.0	1. Remove "Advanced Information"	P1	MAY/12/2004
	2. Change pin8:GND-->NC, pin9:VCC-->NC	P1	
1.1	1. Add "6MHz for Die Form only"	P1	JUL/01/2004

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