MX25L12850F

3V, 128M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
RPMC FLASH MEMORY

Contents

3V 128M-BIT [x 1/x 2/x 4] CMOS MXSMIO® (SERIAL MULTI I/O) RPMC FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- 128Mb: 134,217,728 x 1 bit structure or 67,108,864 x 2 bits (two I/O mode) structure or 33,554,432 x 4 bits (four I/O mode) structure
- Protocol Support
  - Single I/O, Dual I/O and Quad I/O
- Latch-up protected to 100mA from -1V to Vcc +1V
- Fast read for SPI mode
  - Support fast clock frequency for read operation as 104MHz
  - Support Fast Read, 2READ, DREAD, 4READ, QREAD instructions
- Default Quad I/O enable (QE bit=1), and can not be change
- Equal Sectors with 4K byte each, or Equal Blocks with 32K byte each or Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Programming :
  - 256byte page buffer
  - Quad Input/Output page program(4PP) to enhance program performance
- Typical 100,000 erase/program cycles
- 20 years data retention

RPMC FEATURES

- **Support Replay Protection Monotonic Counter (RPMC)**
  - Four 32-bit Monotonic counters
  - Volatile HMAC Key register
  - Non-volatile Root Key register

  RPMC related information is available at
  https://downloadcenter.intel.com/Detail_Desc.aspx?agr=Y&DwnldID=22646

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Block lock protection
  - The BP0-BP3 and T/B status bit defines the size of the area to be protection against program and erase instructions
- Additional 4K bit security OTP
  - Features unique identifier
  - factory locked identifiable, and customer lockable
- Command Reset
- Program/Erase Suspend and Resume operation
- Electronic Identification
  - JEDEC 1-byte manufacturer ID and 2-byte device ID
  - RES command for 1-byte Device ID
  - REMS command for 1-byte manufacturer ID and 1-byte device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input/Output
- SO/SIO1
  - Serial Data Input/Output
- SIO2
  - Serial Data Input/Output
- SIO3
  - Serial Data input/Output
- PACKAGE
  - 8-pin SOP (200mil)
  - 8-land WSON (6x5mm)
  - 8-pin PDIP (300mil)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L12850F is 128Mb bits serial Flash memory, which is configured as 16,777,216 x 8 internally. When it is in two or four I/O mode, the structure becomes 67,108, 864 bits x 2 or 33,554,432 bits x 4. MX25L12850F feature a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

When it is in two I/O read mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in four I/O read mode, the SI pin, SO pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data output.

The MX25L12850F MXSMIO® (Serial Multi I/O) provides sequential read operation on whole chip.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis for erase command is executed on sector (4K-byte), block (32K-byte), or block (64K-byte), or whole chip basis.

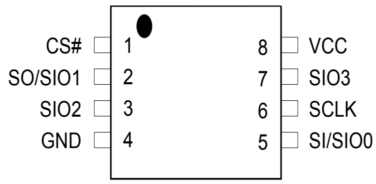
To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode.

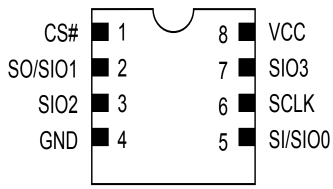
The MX25L12850F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

3. PIN CONFIGURATIONS

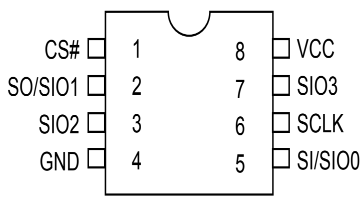
8-PIN SOP (200mil)



8-WSON (6x5mm)



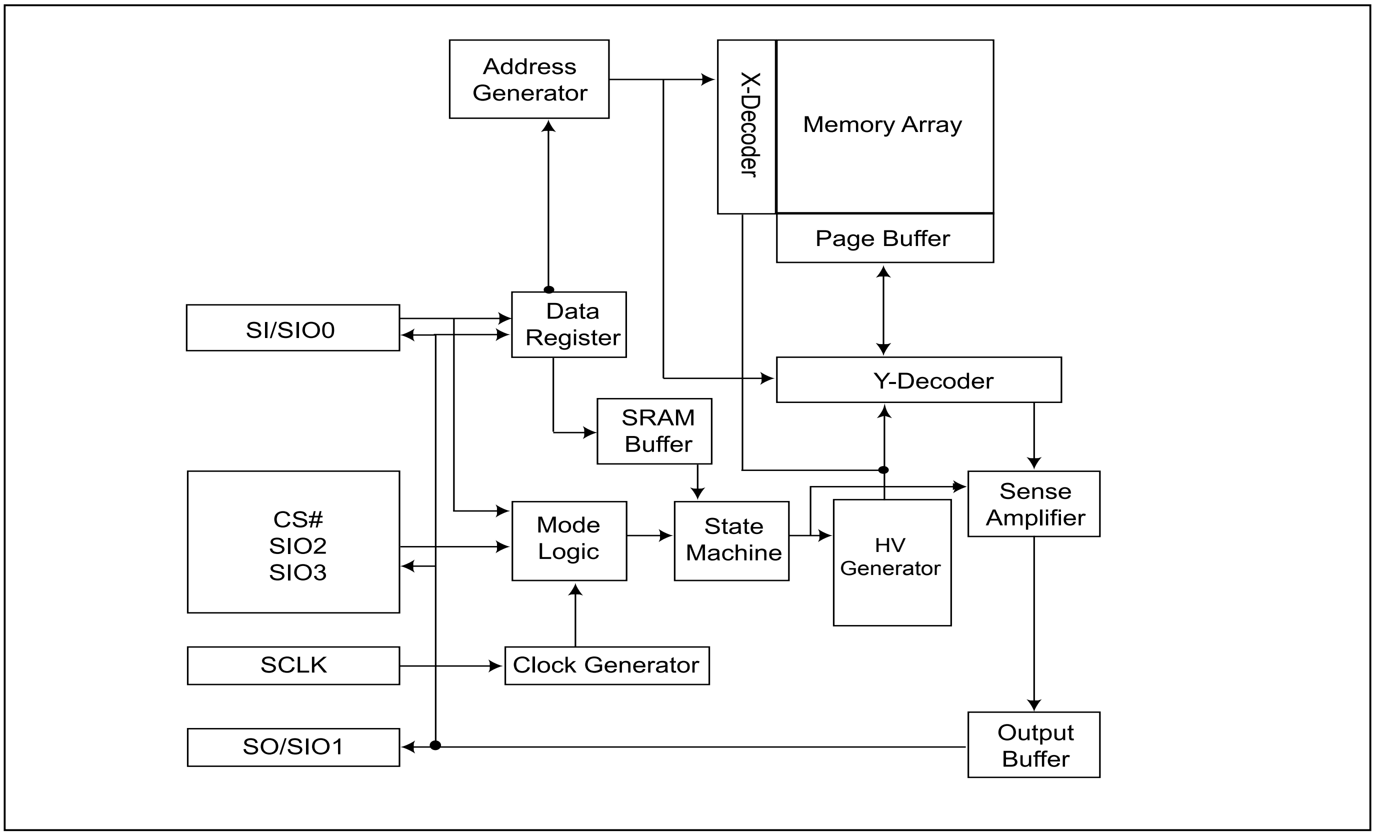
8-PIN PDIP (300mil)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input & Output
SO/SIO1	Serial Data Input & Output
SCLK	Clock Input
SIO2	Serial Data Input & Output
SIO3	Serial Data Input & Output
VCC	+ 3V Power Supply
GND	Ground

5. BLOCK DIAGRAM



6. DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.
- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before other command to change data.
- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from deep power down mode command (RDP) and Read Electronic Signature command (RES), and softreset command.

I. Block lock protection

- The Software Protected Mode (SPM) use (BP3, BP2, BP1, BP0 and T/B) bits to allow part of memory to be protected as read only. The protected area definition is shown as *"Table 1. Protected Area Sizes"*, the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits.

Table 1. Protected Area Sizes

Protected Area Sizes (T/B bit = 0)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 255th)
0	0	1	0	2 (2 blocks, block 254th-255th)
0	0	1	1	3 (4 blocks, block 252nd-255th)
0	1	0	0	4 (8 blocks, block 248th-255th)
0	1	0	1	5 (16 blocks, block 240th-255th)
0	1	1	0	6 (32 blocks, block 224th-255th)
0	1	1	1	7 (64 blocks, block 192nd-255th)
1	0	0	0	8 (128 blocks, block 128th-255th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

Protected Area Sizes (T/B bit = 1)

Status bit				Protect Level
BP3	BP2	BP1	BP0	128Mb
0	0	0	0	0 (none)
0	0	0	1	1 (1 block, protected block 0th)
0	0	1	0	2 (2 blocks, protected block 0th~1th)
0	0	1	1	3 (4 blocks, protected block 0th~3rd)
0	1	0	0	4 (8 blocks, protected block 0th~7th)
0	1	0	1	5 (16 blocks, protected block 0th~15th)
0	1	1	0	6 (32 blocks, protected block 0th~31st)
0	1	1	1	7 (64 blocks, protected block 0th~63rd)
1	0	0	0	8 (128 blocks, protected block 0th~127th)
1	0	0	1	9 (256 blocks, protected all)
1	0	1	0	10 (256 blocks, protected all)
1	0	1	1	11 (256 blocks, protected all)
1	1	0	0	12 (256 blocks, protected all)
1	1	0	1	13 (256 blocks, protected all)
1	1	1	0	14 (256 blocks, protected all)
1	1	1	1	15 (256 blocks, protected all)

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit one-time program area for setting device unique serial number - Which may be set by factory or system customer.

- Security register bit 0 indicates whether the chip is locked by factory or not.

- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with Enter Security OTP command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing Exit Security OTP command.

- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to *"Table 8. Security Register Definition"* for security register bit definition and *"Table 2. 4K-bit Secured OTP Definition"* for address range definition.

- Note: Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed.

Table 2. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

7. Memory Organization

Table 3. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector	Address Range	
255	511	4095	FFF000h	FFFFFFh
		⋮		
		4088	FF8000h	FF8FFFh
	510	4087	FF7000h	FF7FFFh
		⋮		
		4080	FF0000h	FF0FFFh
254	509	4079	FEF000h	FEFFFFh
		⋮		
		4072	FE8000h	FE8FFFh
	508	4071	FE7000h	FE7FFFh
		⋮		
		4064	FE0000h	FE0FFFh
253	507	4063	FDF000h	FDFFFFh
		⋮		
		4056	FD8000h	FD8FFFh
	506	4055	FD7000h	FD7FFFh
		⋮		
		4048	FD0000h	FD0FFFh

2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

8. DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, this device becomes standby mode and keeps the standby mode until next CS# falling edge. In standby mode, SO pin of this device should be High-Z.

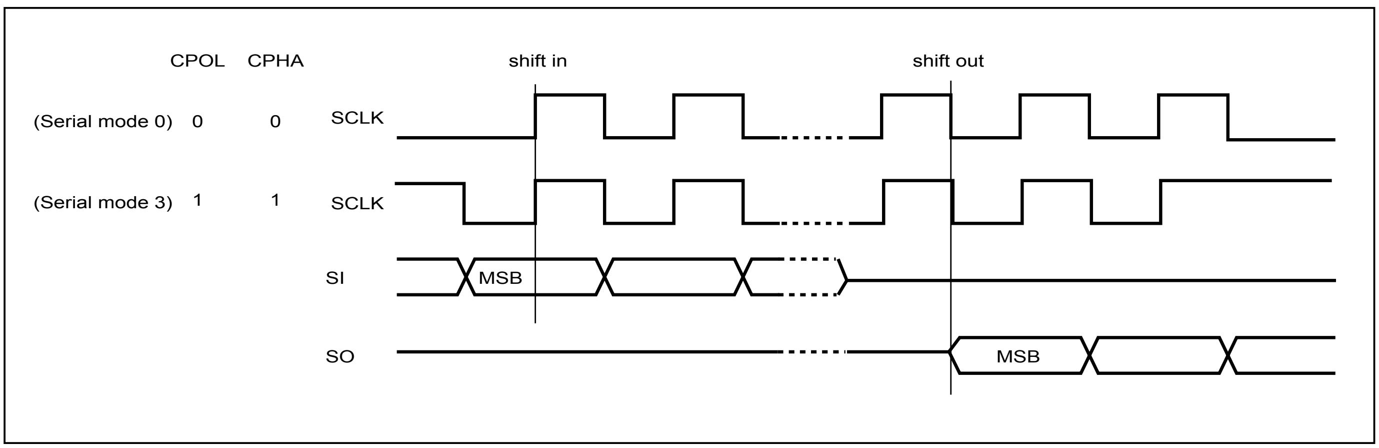
3. When correct command is inputted to this device, this device becomes active mode and keeps the active mode until next CS# rising edge.

4. Input data is latched on the rising edge of Serial Clock (SCLK) and data shifts out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as "Serial Modes Supported".

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, 2READ, DREAD, 4READ, QREAD, RDSFDP, RES, REMS, RDCR the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE32K, BE, CE, PP, 4PP, DP, ENSO, EXSO, WRSCUR, SUSPEND, RESUME, NOP, RSTEN, RST the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. During the progress of Write Status Register, Program, Erase operation, to access the memory array is neglected and not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

Figure 2. Serial Input Timing

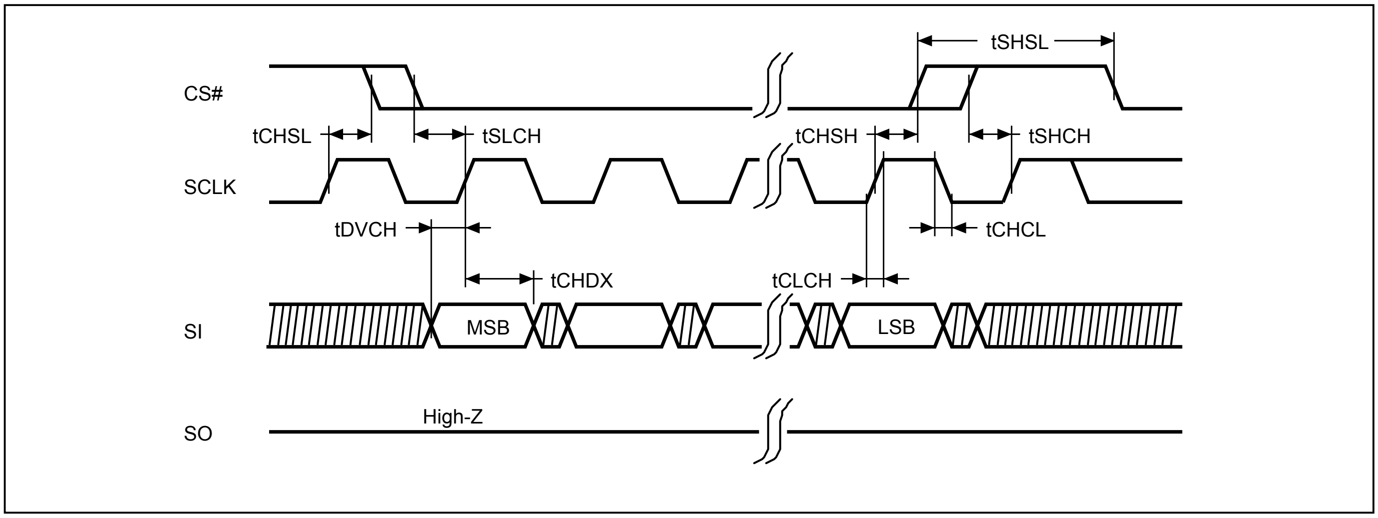
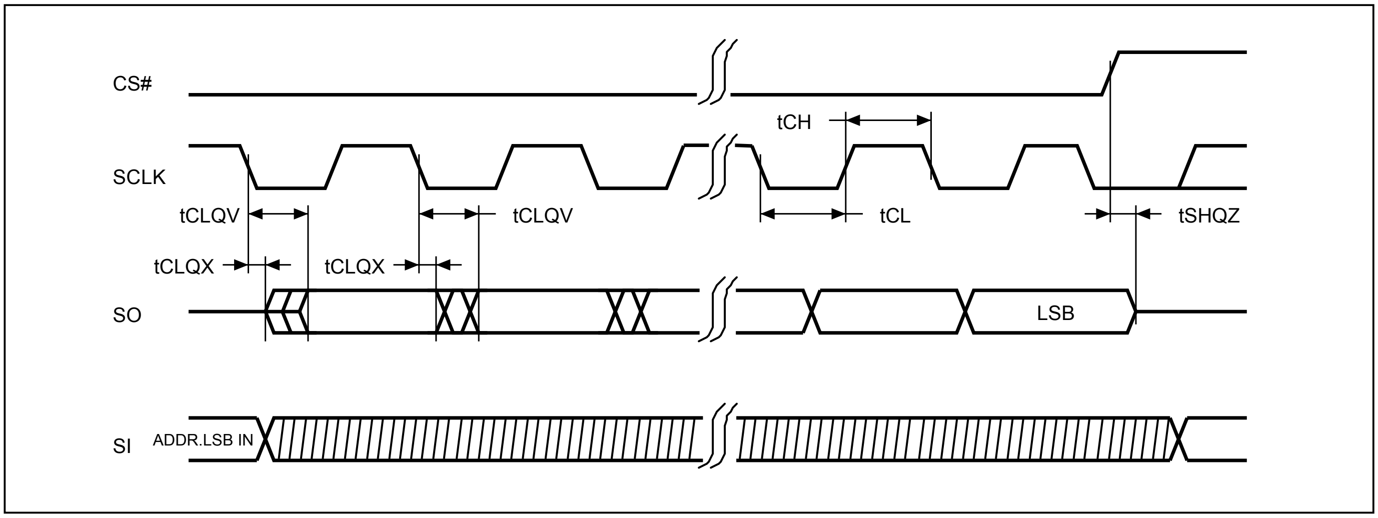


Figure 3. Output Timing



9. COMMAND DESCRIPTION

Table 4. Command Set

Read/Write Array Commands

Command (byte)	READ (normal read)	FAST READ (fast read data)	2READ (2 x I/O read command)	DREAD (1I 2O read)	4READ (4 I/O read)	QREAD (1I 4O read)
Address Bytes	3	3	3	3	3	3
1st byte	03 (hex)	0B (hex)	BB (hex)	3B (hex)	EB (hex)	6B (hex)
2nd byte	ADD1	ADD1	ADD1	ADD1	ADD1	ADD1
3rd byte	ADD2	ADD2	ADD2	ADD2	ADD2	ADD2
4th byte	ADD3	ADD3	ADD3	ADD3	ADD3	ADD3
5th byte		Dummy (8)	Dummy (4)	Dummy (8)	Dummy (6)	Dummy (8)
Data Cycles						
Action	n bytes read out until CS# goes high	n bytes read out until CS# goes high	n bytes read out by 2 x I/O until CS# goes high	n bytes read out by Dual output until CS# goes high	n bytes read out by 4 x I/O until CS# goes high	n bytes read out by Quad output until CS# goes high

Command (byte)	PP (page program)	4PP (quad page program)	SE (sector erase)	BE 32K (block erase 32KB)	BE (block erase 64KB)	CE (chip erase)
Address Bytes	3	3	3	3	3	0
1st byte	02 (hex)	38 (hex)	20 (hex)	52 (hex)	D8 (hex)	60 or C7 (hex)
2nd byte		ADD1	ADD1	ADD1	ADD1	
3rd byte		ADD2	ADD2	ADD2	ADD2	
4th byte		ADD3	ADD3	ADD3	ADD3	
5th byte						
Data Cycles	1-256	1-256				
Action	to program the selected page	quad input to program the selected page	to erase the selected sector	to erase the selected 32K block	to erase the selected block	to erase whole chip

Register/Setting Commands

Command (byte)	WREN (write enable)	WRDI (write disable)	RDSR (read status register)	RDCR (read configuration register)	WRSR (write status/ configuration register)	PGM/ERS Suspend (Suspends Program/ Erase)	PGM/ERS Resume (Resumes Program/ Erase)
1st byte	06 (hex)	04 (hex)	05 (hex)	15 (hex)	01 (hex)	B0 (hex)	30 (hex)
2nd byte					Values		
3rd byte					Values		
4th byte							
5th byte							
Data Cycles					1-2		
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	to read out the values of the status register	to read out the values of the configuration register	to write new values of the status/ configuration register		

Command (byte)	DP (Deep power down)	RDP (Release from deep power down)
1st byte	B9 (hex)	AB (hex)
2nd byte		
3rd byte		
4th byte		
5th byte		
Data Cycles		
Action	enters deep power down mode	release from deep power down mode

ID/Security Commands

Command (byte)	RDID (read identific-ation)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)	RDSFDP	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)
Address Bytes	0	0	0	3	0	0	0
1st byte	9F (hex)	AB (hex)	90 (hex)	5A (hex)	B1 (hex)	C1 (hex)	2B (hex)
2nd byte		x	x	ADD1			
3rd byte		x	x	ADD2			
4th byte		x	ADD1 (Note 1)	ADD3			
5th byte				Dummy (8)			
Action	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out 1-byte Device ID	output the Manufacturer ID & Device ID	Read SFDP mode	to enter the 4K-bit secured OTP mode	to exit the 4K-bit secured OTP mode	to read value of security register

Command (byte)	WRSCUR (write security register)
Address Bytes	0
1st byte	2F (hex)
2nd byte	
3rd byte	
4th byte	
5th byte	
Data Cycles	
Action	to set the lock-down bit as "1" (once lock-down, cannot be updated)

Reset Commands

Command (byte)	NOP (No Operation)	RSTEN (Reset Enable)	RST (Reset Memory)
1st byte	00 (hex)	66 (hex)	99 (hex)
2nd byte			
3rd byte			
4th byte			
5th byte			
Action			

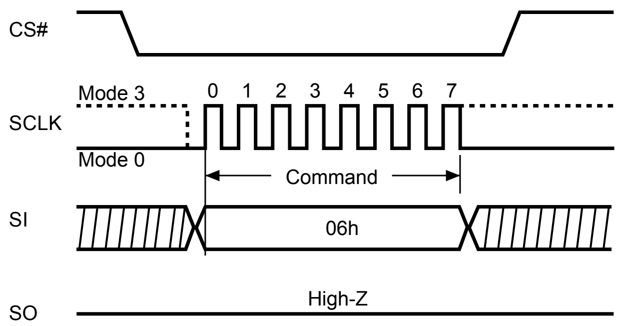
Note 1: The count base is 4-bit for ADD(2) and Dummy(2) because of 2 x I/O. And the MSB is on SO/SIO1 which is different from 1 x I/O condition.
Note 2: ADD=00H will output the manufacturer ID first and AD=01H will output device ID first.
Note 3: It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
Note 4: Before executing RST command, RSTEN command must be executed. If there is any other command to interfere, the reset operation will be disabled.
Note 5: The number in parentheses after "ADD" or "Data" stands for how many clock cycles it has. For example, "Data(8)" represents there are 8 clock cycles for the data in.

9-1. Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, SE, BE32K, BE, CE, WRSCUR and WRSR, which are intended to change the device content WEL bit should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→sending WREN instruction code→ CS# goes high.

Figure 4. Write Enable (WREN) Sequence



9-2. Write Disable (WRDI)

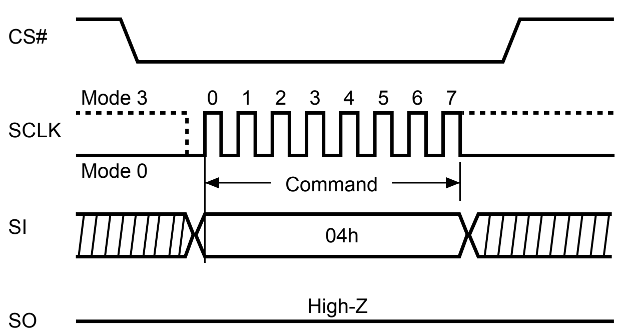
The Write Disable (WRDI) instruction is to reset Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→sending WRDI instruction code→CS# goes high.

The WEL bit is reset by following situations:

- Power-up
- WRDI command completion
- WRSR command completion
- PP command completion
- 4PP command completion
- SE command completion
- BE32K command completion
- BE command completion
- CE command completion
- PGM/ERS Suspend command completion
- Reset command completion
- WRSCUR command completion

Figure 5. Write Disable (WRDI) Sequence



9-3. Read Identification (RDID)

The RDID instruction is for reading the manufacturer ID of 1-byte and followed by Device ID of 2-byte. The Macronix Manufacturer ID and Device ID are listed as *"Table 5. ID Definitions"*.

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code→24-bits ID data out on SO→ to end RDID operation can drive CS# to high at any time during data out.

While Program/Erase operation is in progress, it will not decode the RDID instruction, therefore there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

Figure 6. Read Identification (RDID) Sequence

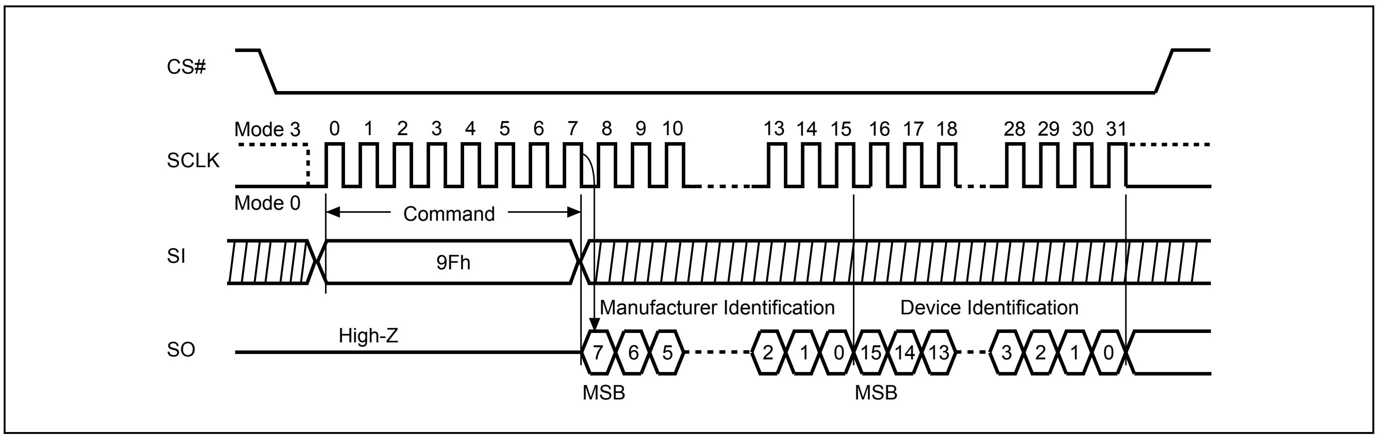


Table 5. ID Definitions

Command Type		MX25L12850F		
RDID	9Fh	Manufactory ID	Memory type	Memory density
		C2	20	18
RES	ABh	Electronic ID		
		17		
REMS	90h	Manufactory ID	Device ID	
		C2	17	

9-4. Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power-down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the Stand-by Power mode is delayed by tRES1, and Chip Select (CS#) must remain High for at least tRES1(max), as specified in *"Table 16. AC CHARACTERISTICS"*. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions. The RDP instruction is only for releasing from Deep Power Down Mode.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as *"Table 5. ID Definitions"*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction.

Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycle; there's no effect on the current program/erase/write cycle in progress.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

Figure 7. Read Electronic Signature (RES) Sequence

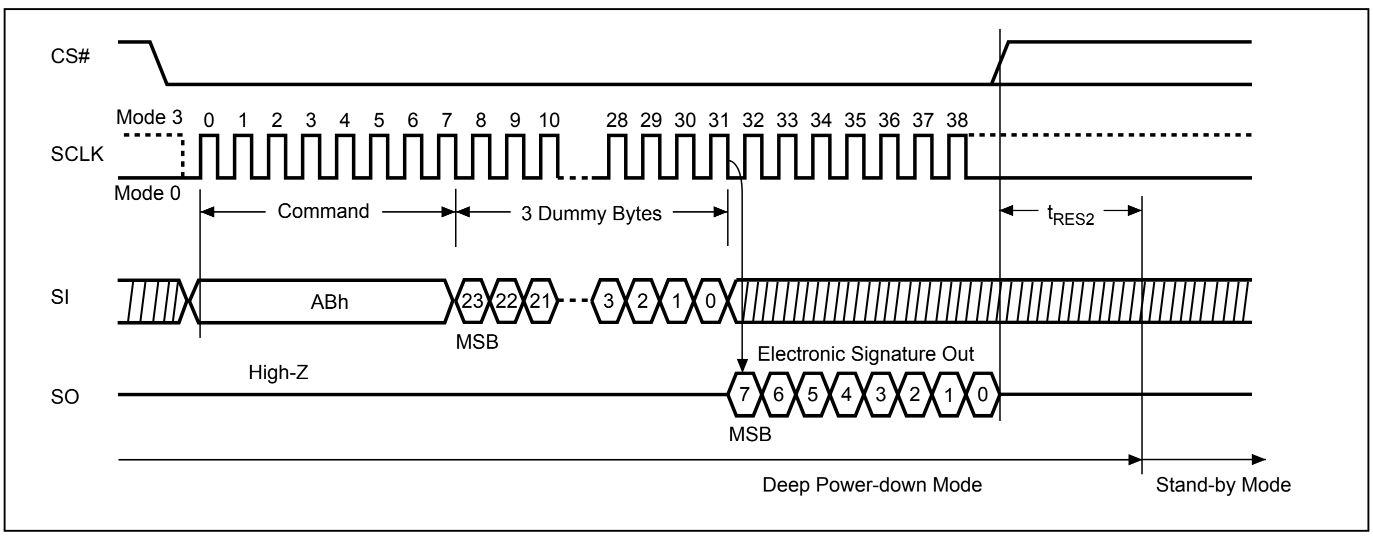
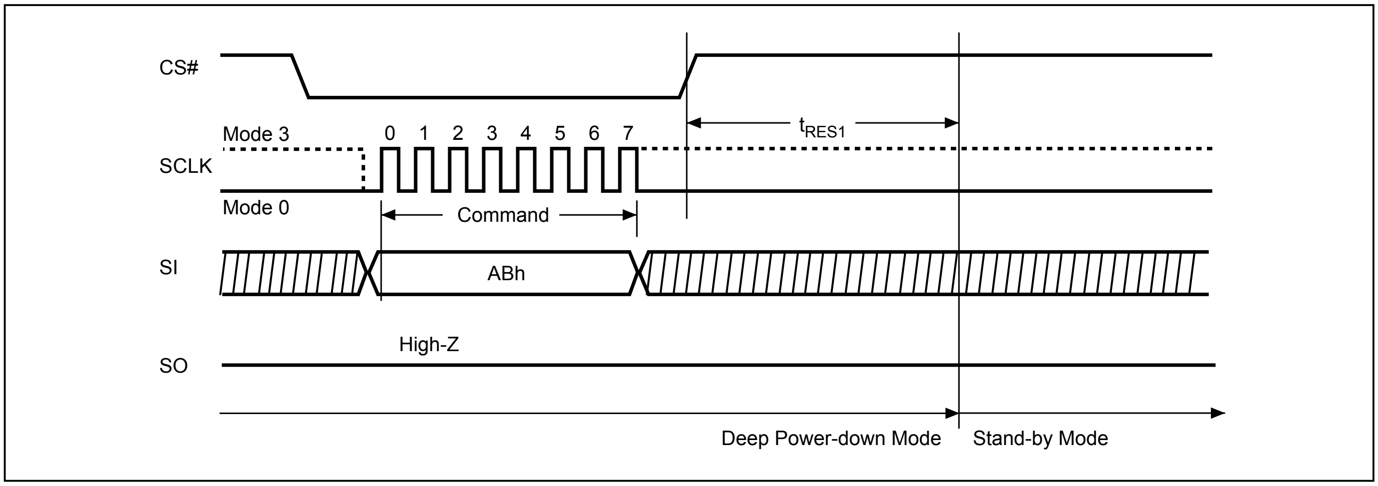


Figure 8. Release from Deep Power-down (RDP) Sequence

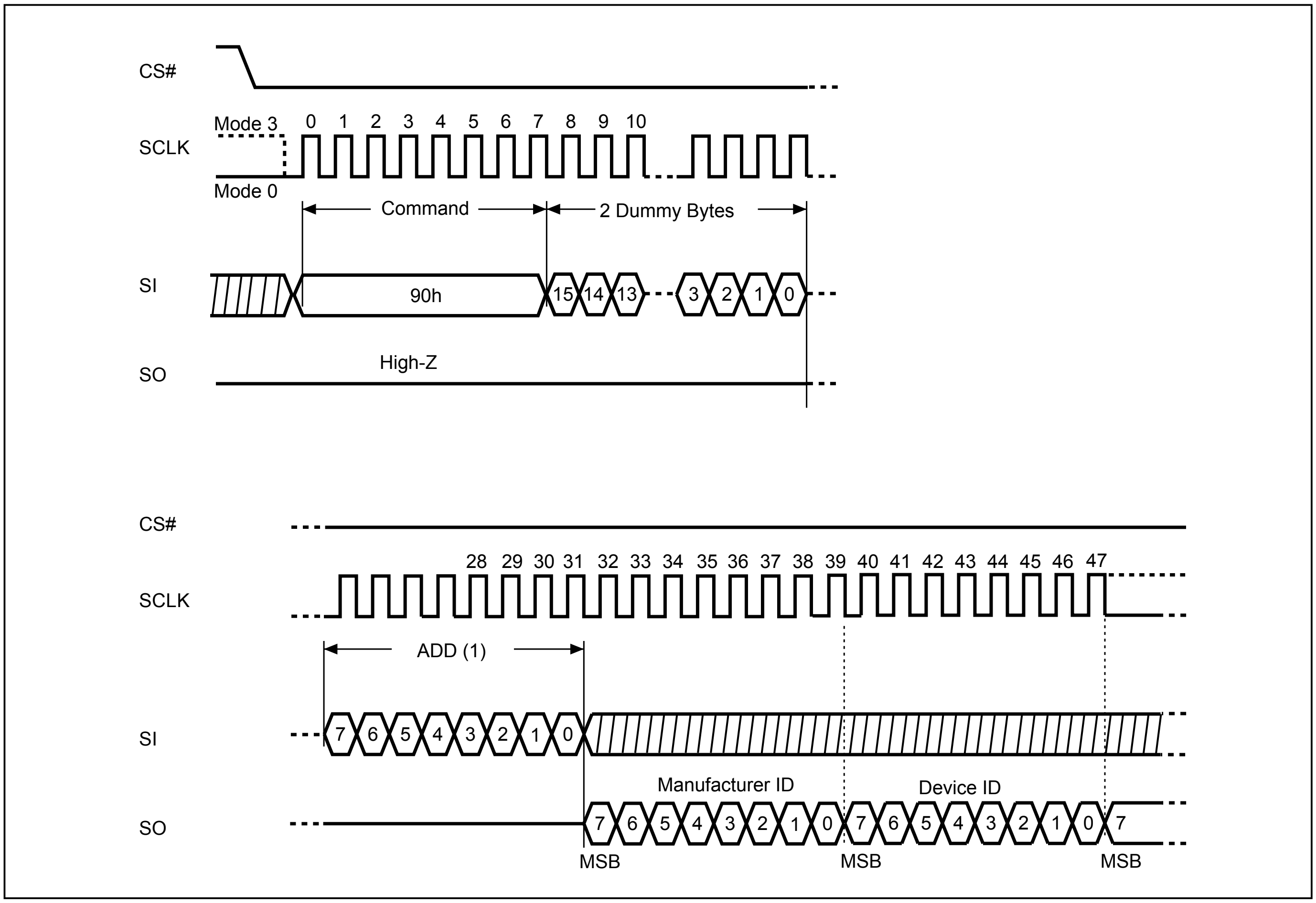


9-5. Read Electronic Manufacturer ID & Device ID (REMS)

The REMS instruction is an alternative to the Release from Power-down/Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The REMS instruction is very similar to the Release from Power-down/Device ID instruction. The instruction is initiated by driving the CS# pin low and shift the instruction code "90h" followed by two dummy bytes and one bytes address. After which, the Manufacturer ID for Macronix (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first. The Device ID values are listed in *"Table 5. ID Definitions"*. If the one-byte address is initially set to 01h, then the device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Figure 9. Read Electronic Manufacturer & Device ID (REMS) Sequence



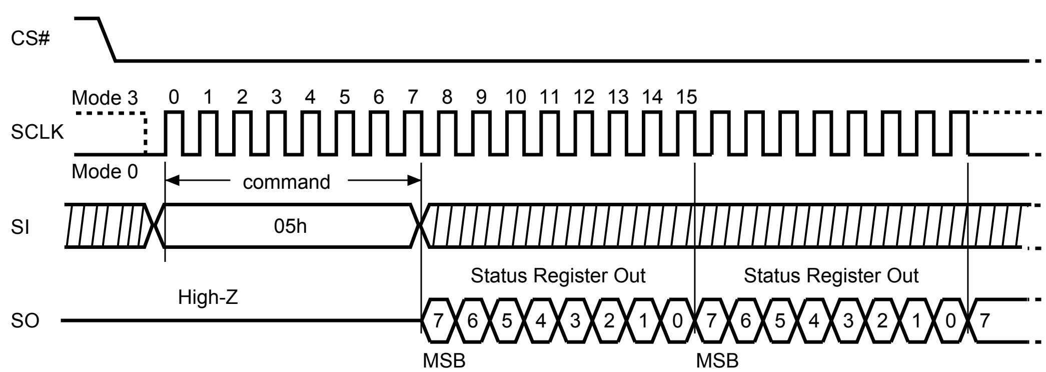
Notes:
(1) ADD=00H will output the manufacturer's ID first and ADD=01H will output device ID first.

9-6. Read Status Register (RDSR)

The RDSR instruction is for reading Status Register Bits. The Read Status Register can be read at any time (even in program/erase/write status register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO.

Figure 10. Read Status Register (RDSR) Sequence

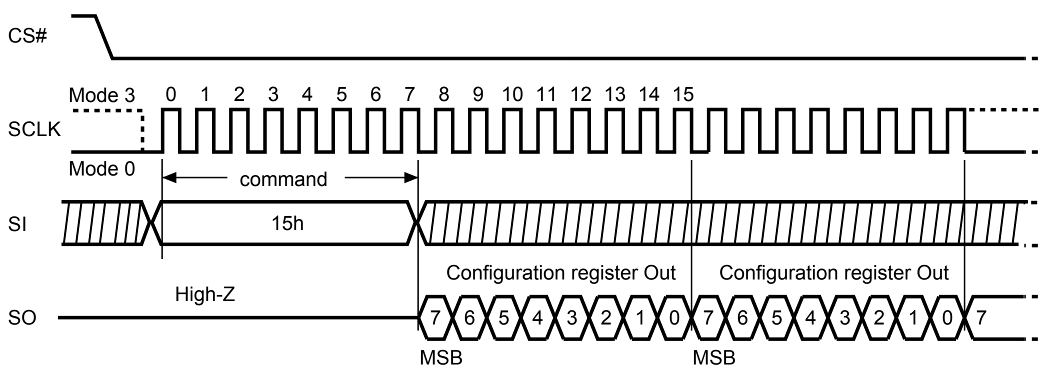


9-7. Read Configuration Register (RDCR)

The RDCR instruction is for reading Configuration Register Bits. The Read Configuration Register can be read at any time (even in program/erase/write configuration register condition). It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write configuration register operation is in progress.

The sequence of issuing RDCR instruction is: CS# goes low→ sending RDCR instruction code→ Configuration Register data out on SO.

Figure 11. Read Configuration Register (RDCR) Sequence



For user to check if Program/Erase operation is finished or not, RDSR instruction flow are shown as follows:

Figure 12. Program/Erase flow with read array data

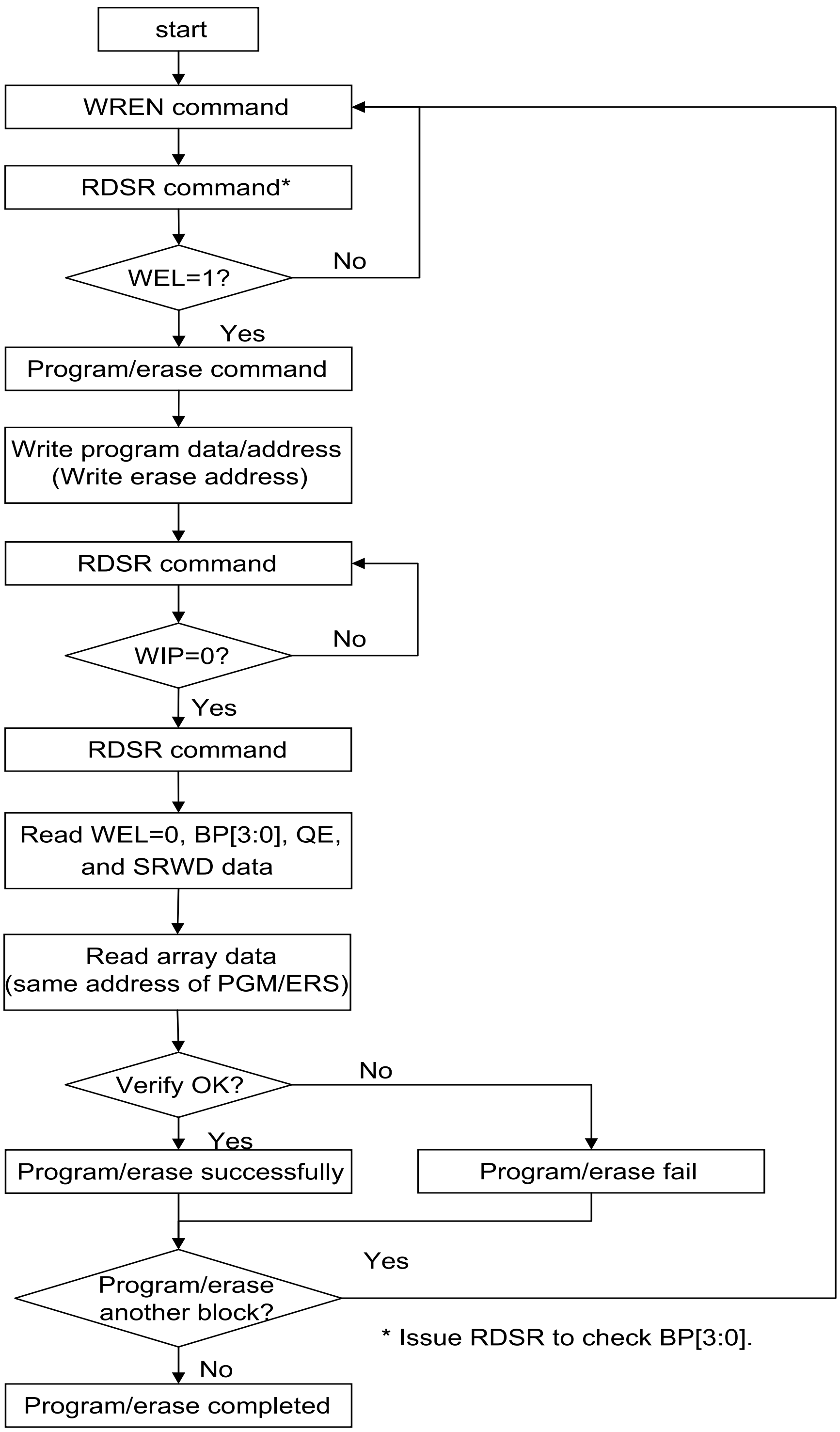
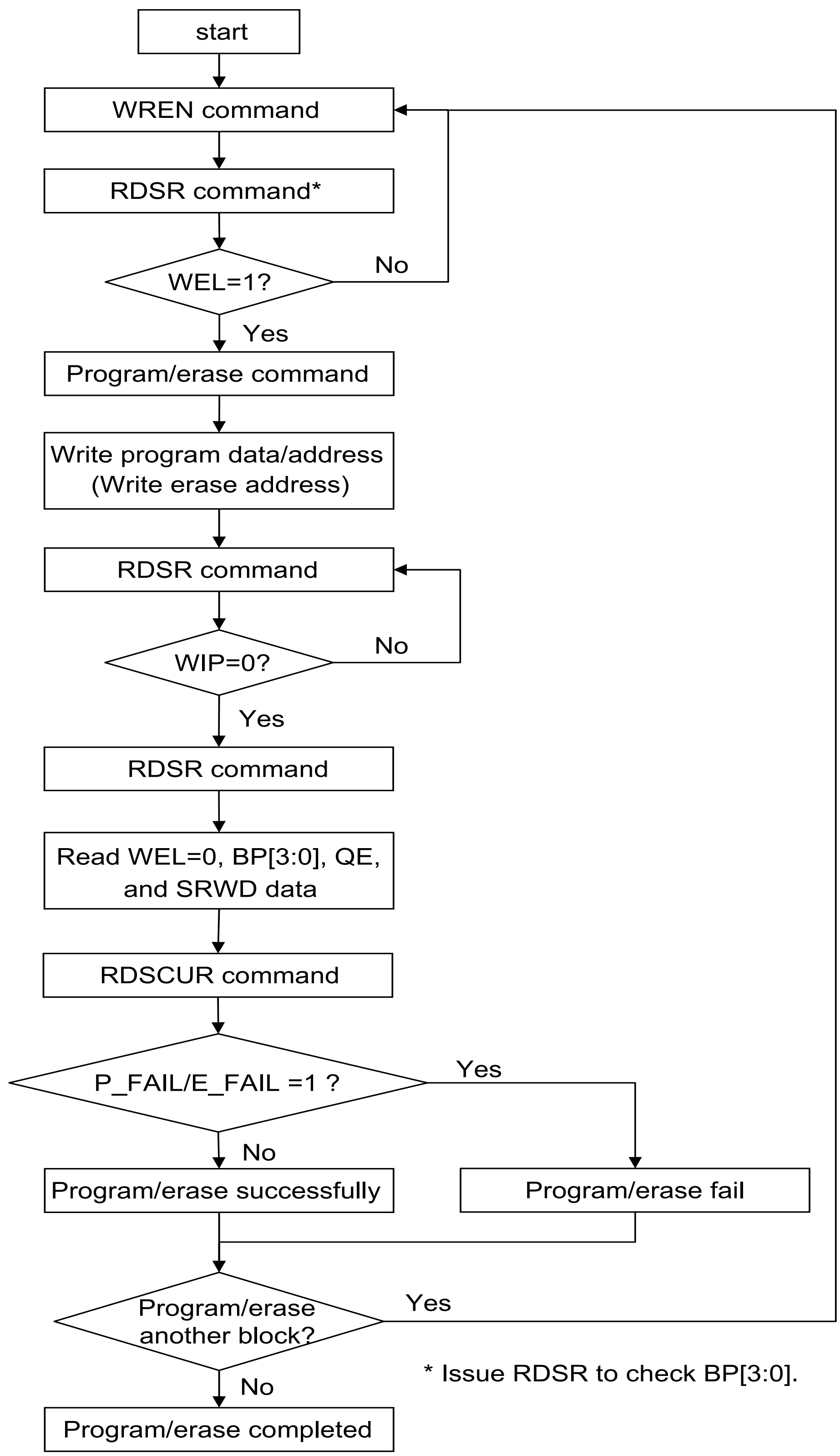


Figure 13. Program/Erase flow without read array data (read P_FAIL/E_FAIL flag)



Status Register

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to 1, which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored if it is applied to a protected memory area. To ensure both WIP bit & WEL bit are both set to 0 and available for next program/erase/operations, WIP bit needs to be confirm to be 0 before polling WEL bit. After WIP bit confirmed, WEL bit needs to be confirm to be 0.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in *"Table 1. Protected Area Sizes"*) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase 32KB (BE32K), Block Erase (BE) and Chip Erase (CE) instructions (only if Block Protect bits (BP3:BP0) set to 0, the CE instruction can be executed). The BP3, BP2, BP1, BP0 bits are "0" as default. Which is un-protected.

QE bit. The Quad Enable (QE) bit, a non-volatile OTP bit which is permanently set to "1". The flash always performs Quad I/O mode.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0".

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1=Quad Enable (note 2)	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	OTP	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Notes:
1. See the *"Table 1. Protected Area Sizes"*.
2. The QE bit is set by factory default, and can not be changed permanently.

Configuration Register

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

TB bit

The Top/Bottom (TB) bit is a non-volatile OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as "0", which means Top area protect. When it is set as "1", the protect area will change to Bottom area of the memory device. To write the TB bits requires the Write Status Register (WRSR) instruction to be executed.

Table 6. Configuration Register Table

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	Reserved	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	Reserved
x	x	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	x
x	x	x	x	OTP	x	x	x

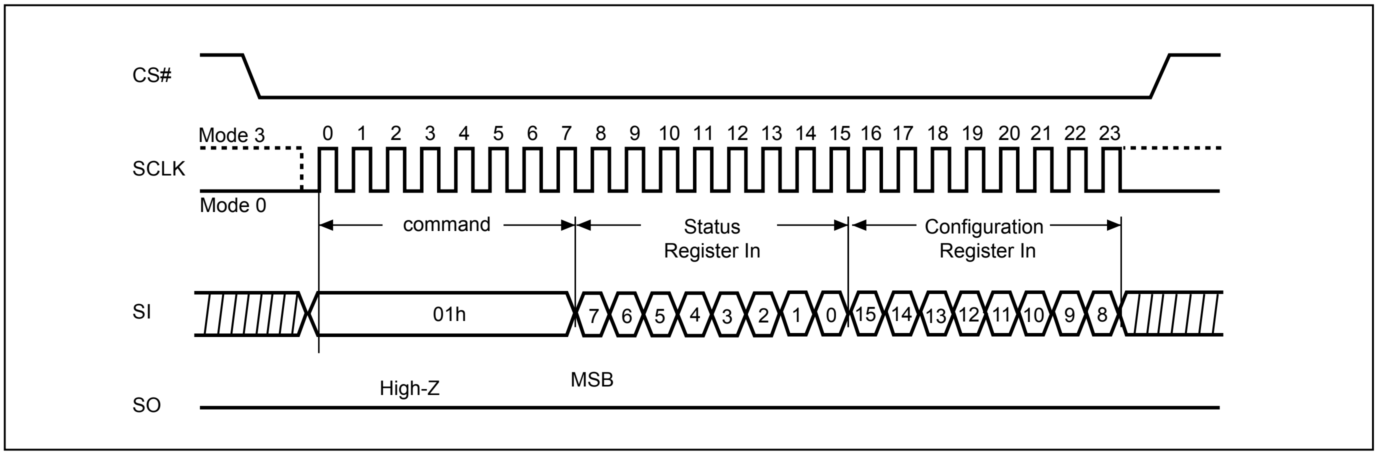
9-8. Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits and Configuration Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *"Table 1. Protected Area Sizes"*), but has no effect on bit1(WEL) and bit0 (WIP) of the status register.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→CS# goes high.

The CS# must go high exactly at the 8 bits or 16 bits data boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Figure 14. Write Status Register (WRSR) Sequence



Note : The CS# must go high exactly at 8 bits or 16 bits data boundary to completed the write register command.

Software Protected Mode (SPM):

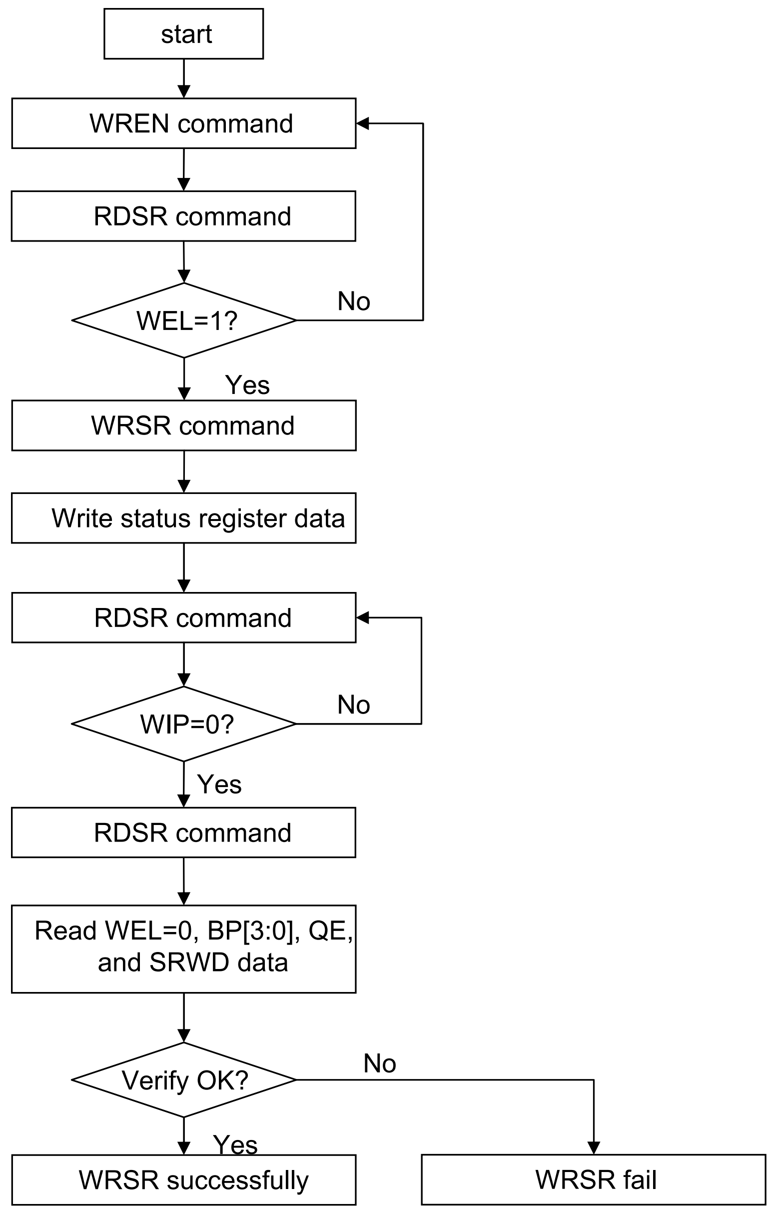
- When SRWD bit=0, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0 and T/B bit, is at software protected mode (SPM).

Table 7. Protection Modes

Mode	Status register condition	SRWD bit status	Memory
Software protection mode (SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	SRWD bit=0	The protected area cannot be program or erase.

Note:
1. As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *"Table 1. Protected Area Sizes"*.

Figure 15. WRSR flow

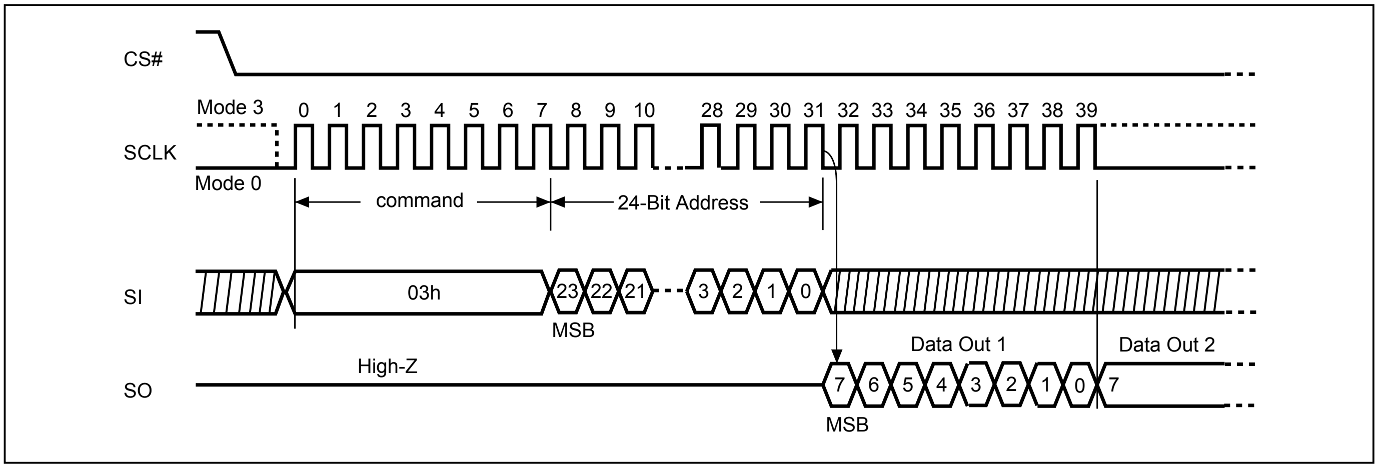


9-9. Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→sending READ instruction code→ 3-byte address on SI→ data out on SO→to end READ operation can use CS# to high at any time during data out.

Figure 16. Read Data Bytes (READ) Sequence



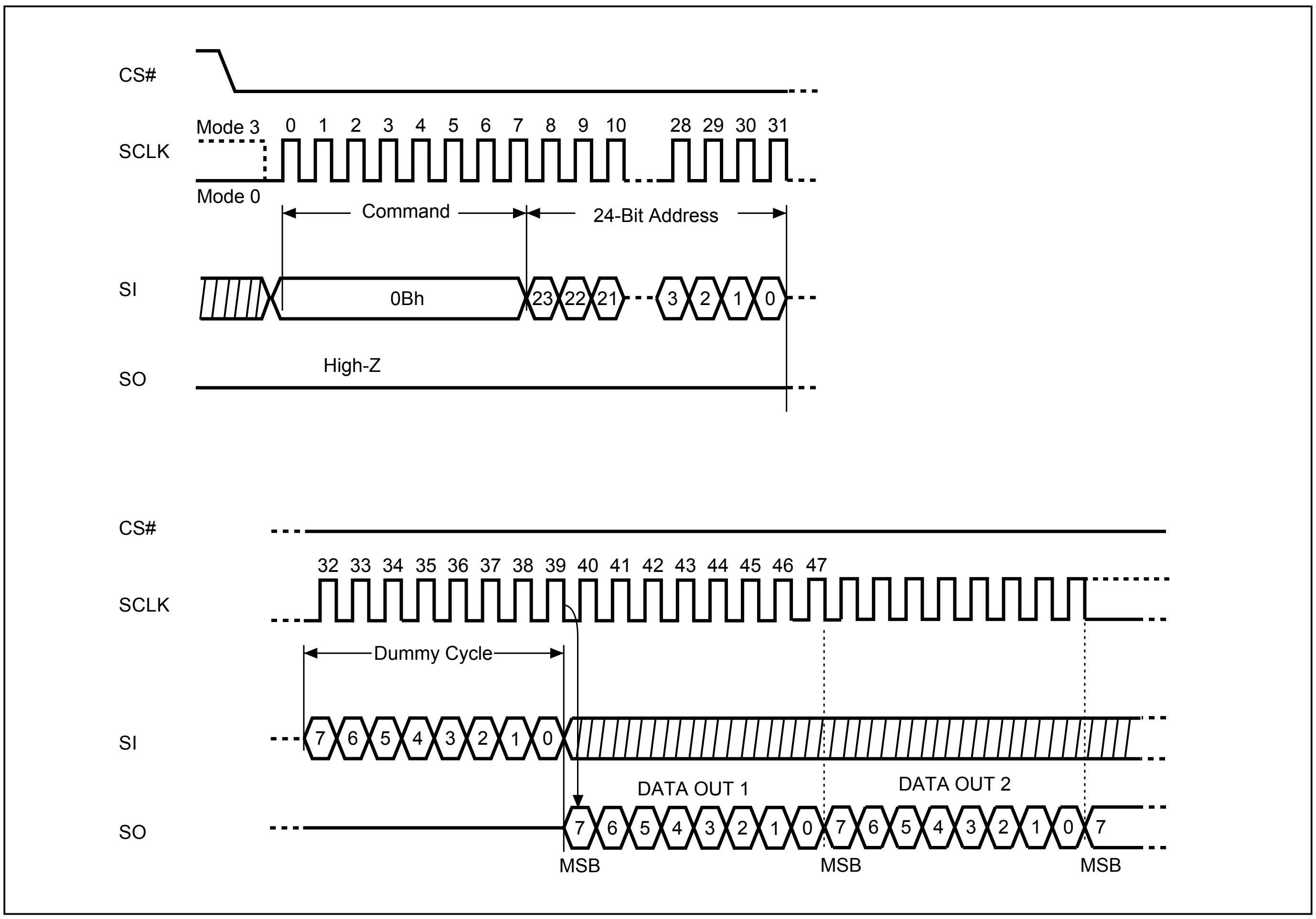
9-10. Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→ sending FAST_READ instruction code→ 3-byte address on SI→ 8 dummy cycles→ data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 17. Read at Higher Speed (FAST_READ) Sequence



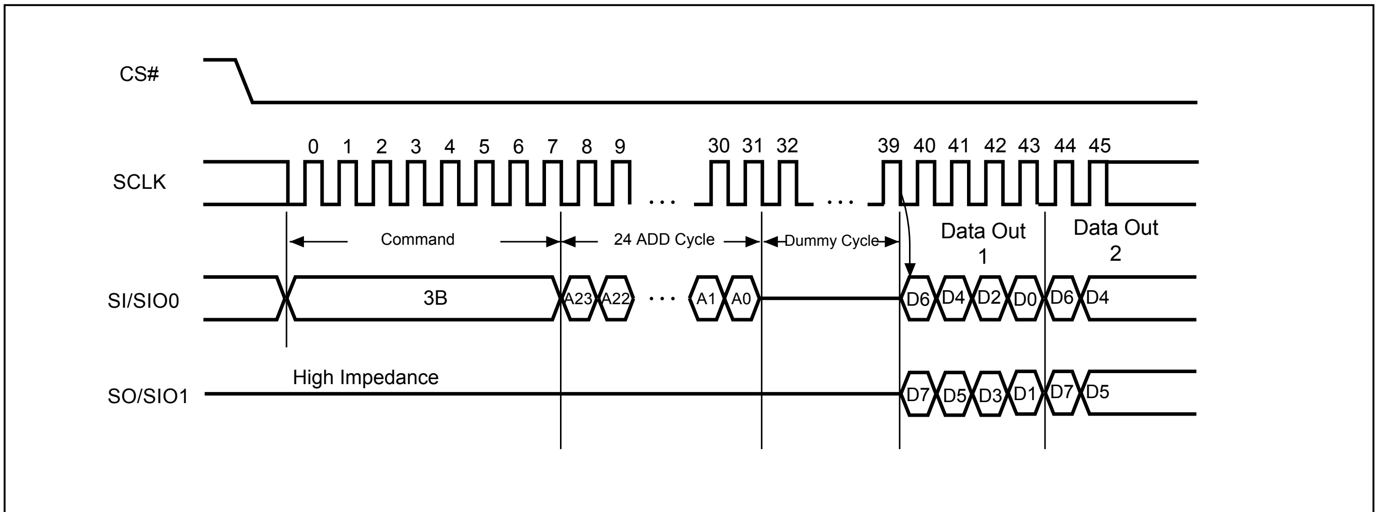
9-11. Dual Output Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low→ sending DREAD instruction→3-byte address on SIO0→ 8 dummy cycles on SIO0→ data out interleave on SIO1 & SIO0→ to end DREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 18. Dual Read Mode Sequence



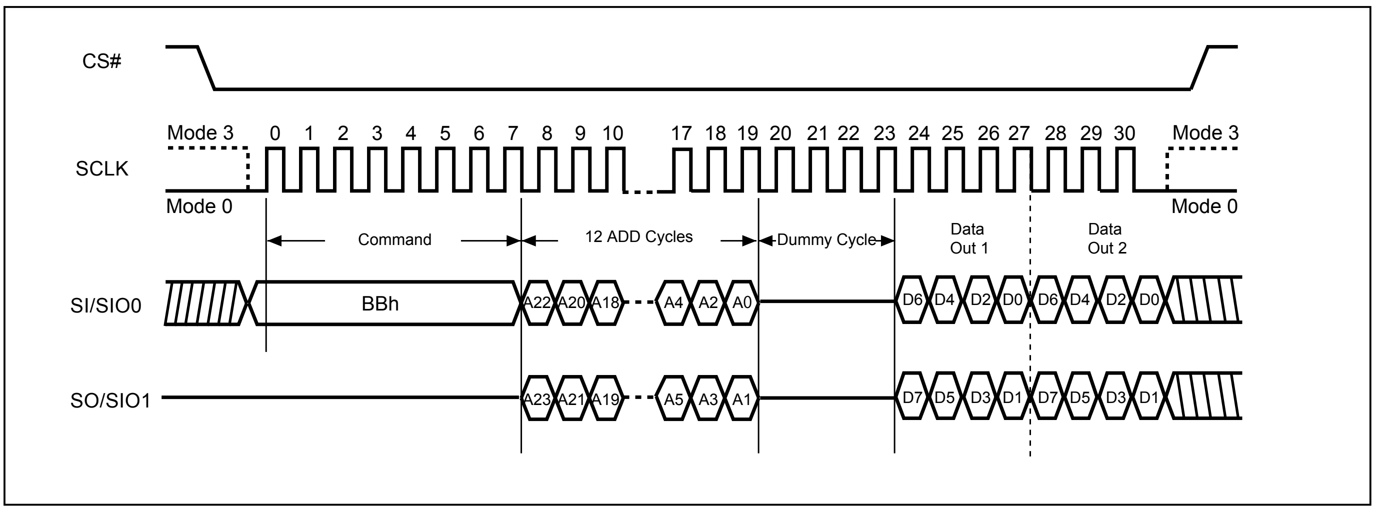
9-12. 2 x I/O Read Mode (2READ)

The 2READ instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 2READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 2READ instruction, the following address/dummy/data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing 2READ instruction is: CS# goes low→ sending 2READ instruction→ 3-byte address interleave on SIO1 & SIO0→ 4 dummy cycles on SIO1 & SIO0→ data out interleave on SIO1 & SIO0→ to end 2READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 2READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 19. 2 x I/O Read Mode Sequence



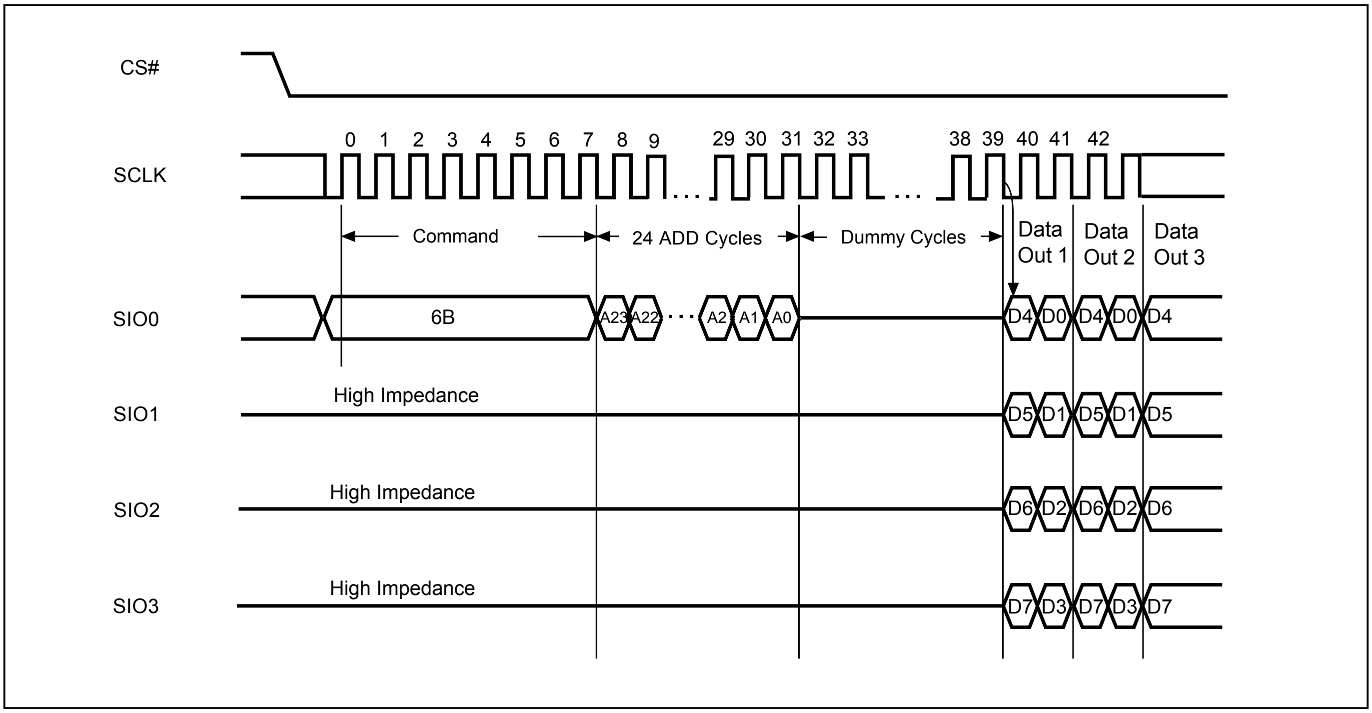
9-13. Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8 dummy cycle → data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end QREAD operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 20. Quad Read Mode Sequence



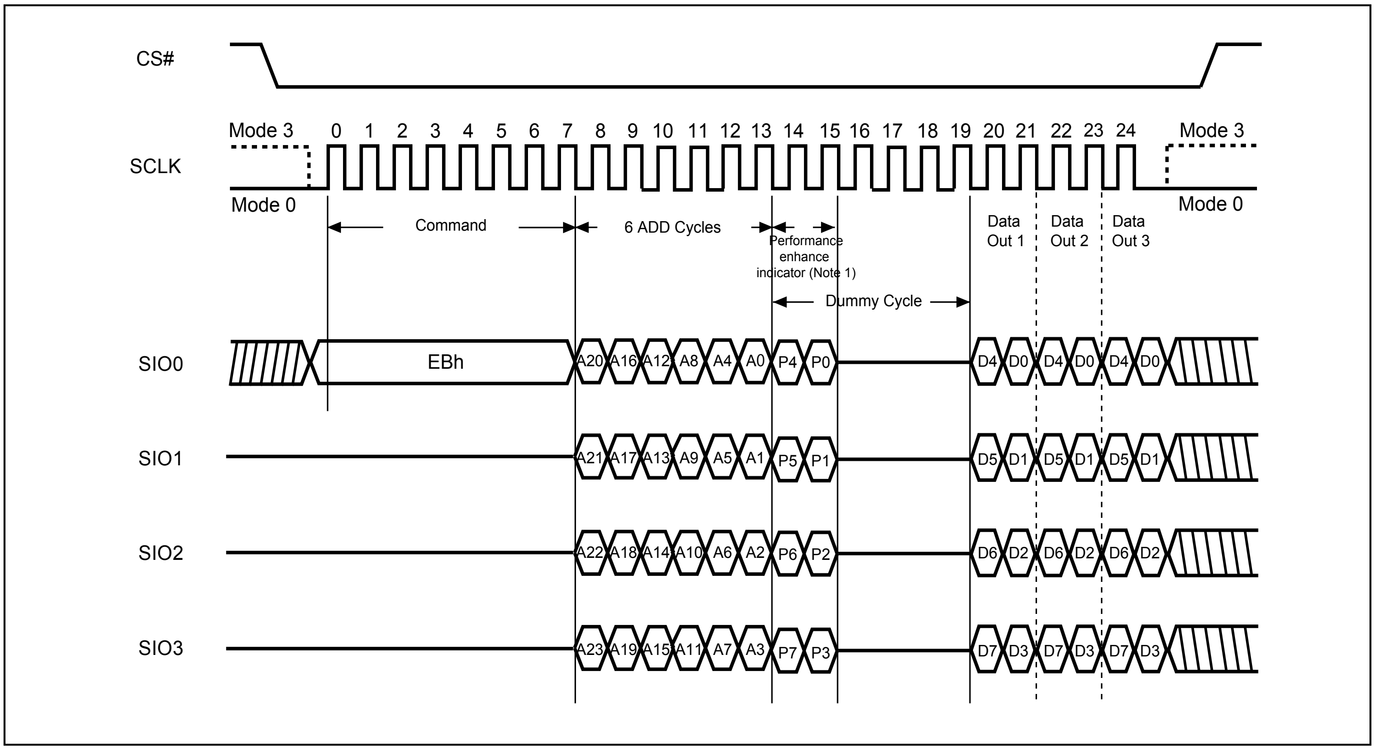
9-14. 4 x I/O Read Mode (4READ)

The 4READ instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single 4READ instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing 4READ instruction, the following address/dummy/data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing 4READ instruction is: CS# goes low→ sending 4READ instruction→ 3-byte address interleave on SIO3, SIO2, SIO1 & SIO0→ 6 dummy cycles →data out interleave on SIO3, SIO2, SIO1 & SIO0→ to end 4READ operation can use CS# to high at any time during data out.

While Program/Erase/Write Status Register cycle is in progress, 4READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

Figure 21. 4 x I/O Read Mode Sequence



Notes:
1. Hi-impedance is inhibited for the two clock cycles.
2. P7≠P3, P6≠P2, P5≠P1 & P4≠P0 (Toggling) is inhibited.

9-15. Performance Enhance Mode

The device could waive the command cycle bits if the two cycle bits after address cycle toggles.

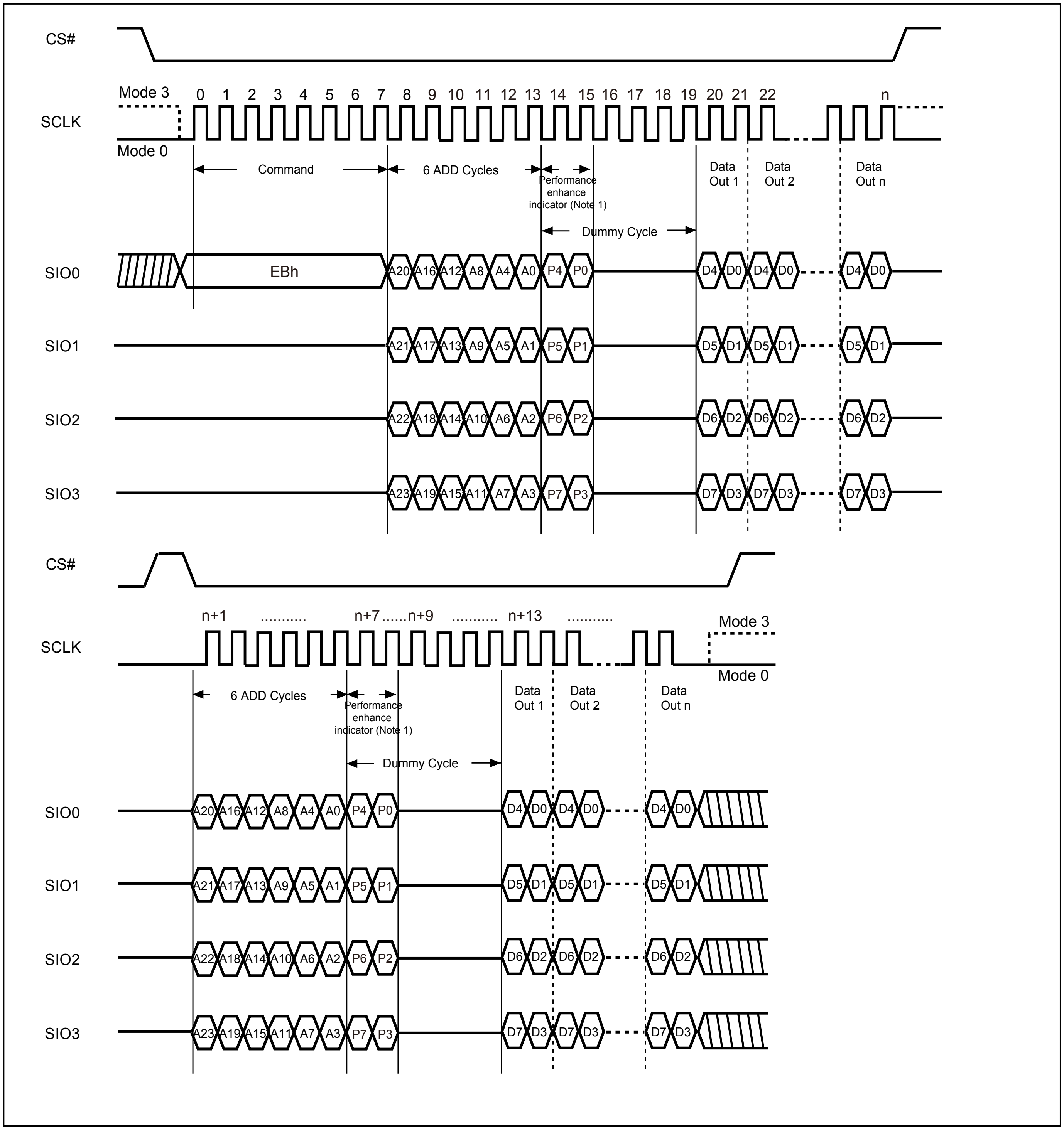
The "EBh" commands support enhance mode. The performance enhance mode is not supported in dual I/O mode.

To enter performance-enhancing mode, P[7:4] must be toggling with P[3:0]; likewise P[7:0]=A5h, 5Ah, F0h or 0Fh can make this mode continue and skip the next 4READ instruction. To leave enhance mode, P[7:4] is no longer toggling with P[3:0]; likewise P[7:0]=FFh, 00h, AAh or 55h along with CS# is afterwards raised and then lowered. Issuing "FFh" command can also exit enhance mode. The system then will leave performance enhance mode and return to normal operation.

After entering enhance mode, following CS# go high, the device will stay in the read mode and treat CS# go low of the first clock as address instead of command cycle.

Another sequence of issuing 4READ instruction especially useful in random access is : CS# goes low→sending 4 READ instruction→3-bytes address interleave on SIO3, SIO2, SIO1 & SIO0 →performance enhance toggling bit P[7:0]→ 4 dummy cycles →data out still CS# goes high → CS# goes low (reduce 4 Read instruction) → 3-bytes random access address.

Figure 22. 4 x I/O Read enhance performance Mode Sequence



Notes:

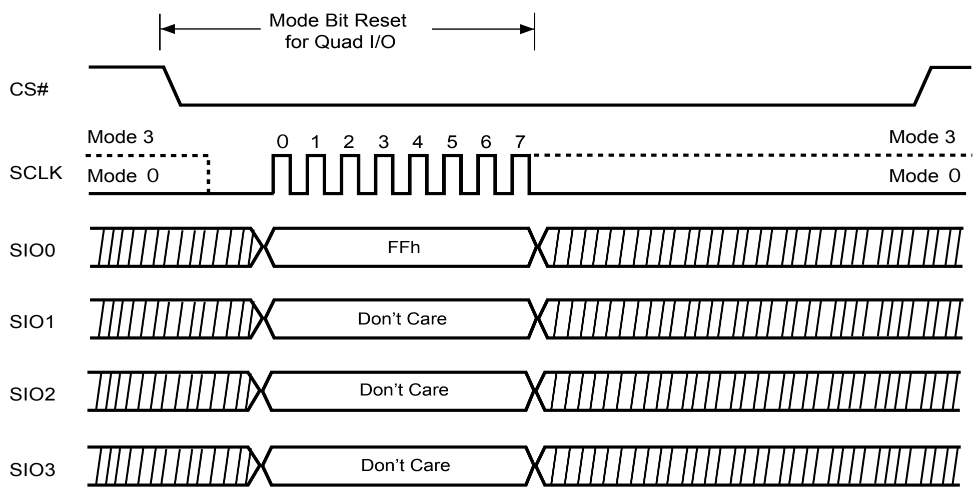
1. If not using performance enhance recommend to keep 1 or 0 in performance enhance indicator.

9-16. Performance Enhance Mode Reset

To conduct the Performance Enhance Mode Reset operation in SPI mode, FFh data cycle, 8 clocks, should be issued in 1I/O sequence.

If the system controller is being Reset during operation, the flash device will return to the standard SPI operation.

Figure 23. Performance Enhance Mode Reset for Fast Read Quad I/O



9-17. Sector Erase (SE)

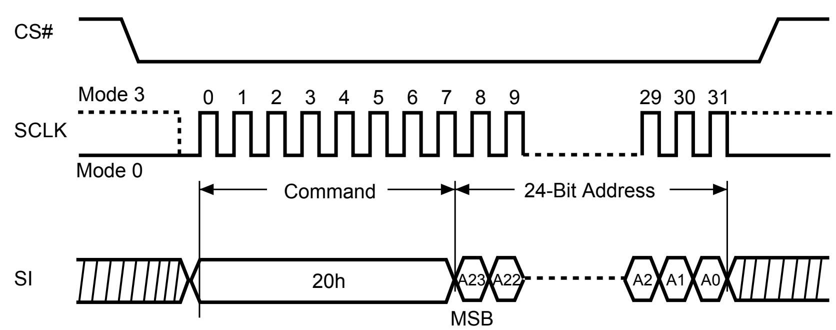
The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *"Table 3. Memory Organization"*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address byte been latched-in); otherwise, the instruction will be rejected and not executed.

Address bits [Am-A12] (Am is the most significant address) select the sector address.

The sequence of issuing SE instruction is: CS# goes low→ sending SE instruction code→ 3-byte address on SI→ CS# goes high.

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets 1 during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Sector Erase (SE) instruction will not be executed on the block.

Figure 24. Sector Erase (SE) Sequence



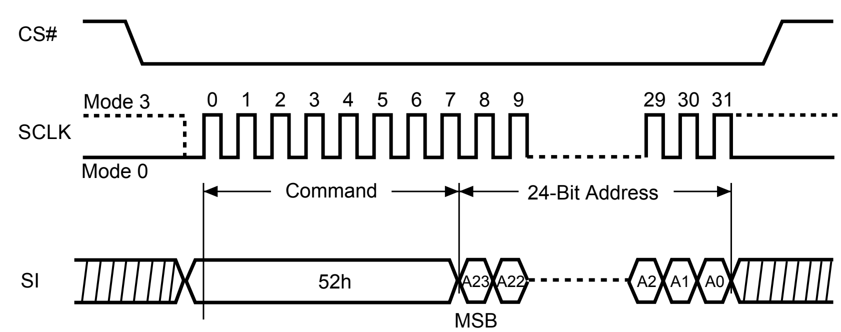
9-18. Block Erase (BE32K)

The Block Erase (BE32K) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE32K). Any address of the block (see *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE32K) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32K instruction is: CS# goes low→ sending BE32K instruction code→ 3-byte address on SI→CS# goes high.

The self-timed Block Erase Cycle time (tBE32K) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while during the Block Erase cycle is in progress. The WIP sets during the tBE32K timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Block Erase (BE32K) instruction will not be executed on the block.

Figure 25. Block Erase 32KB (BE32K) Sequence



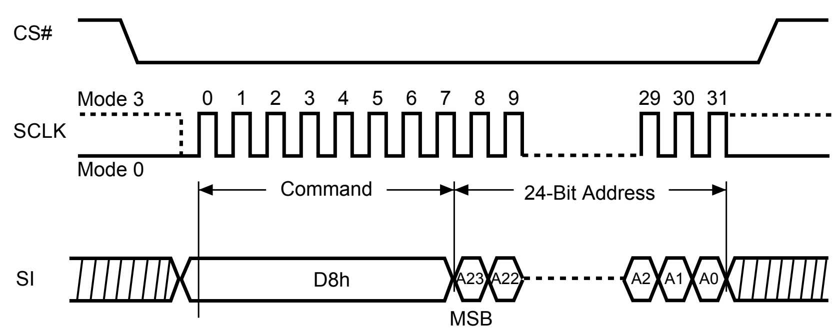
9-19. Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (Please refer to *"Table 3. Memory Organization"*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low→ sending BE instruction code→ 3-byte address on SI→ CS# goes high.

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is reset. If the Block is protected by BP bits (Block Protect Mode), the Block Erase (BE) instruction will not be executed on the block.

Figure 26. Block Erase (BE) Sequence



9-20. Chip Erase (CE)

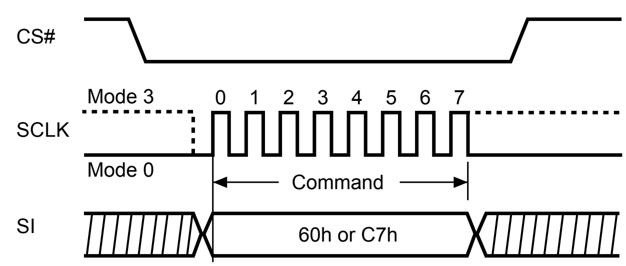
The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low→sending CE instruction code→CS# goes high.

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared.

When the chip is under "Block protect (BP) Mode". The Chip Erase(CE) instruction will not be executed, if one (or more) sector is protected by BP3-BP0 bits. It will be only executed when BP3-BP0 all set to "0".

Figure 27. Chip Erase (CE) Sequence



9-21. Page Program (PP)

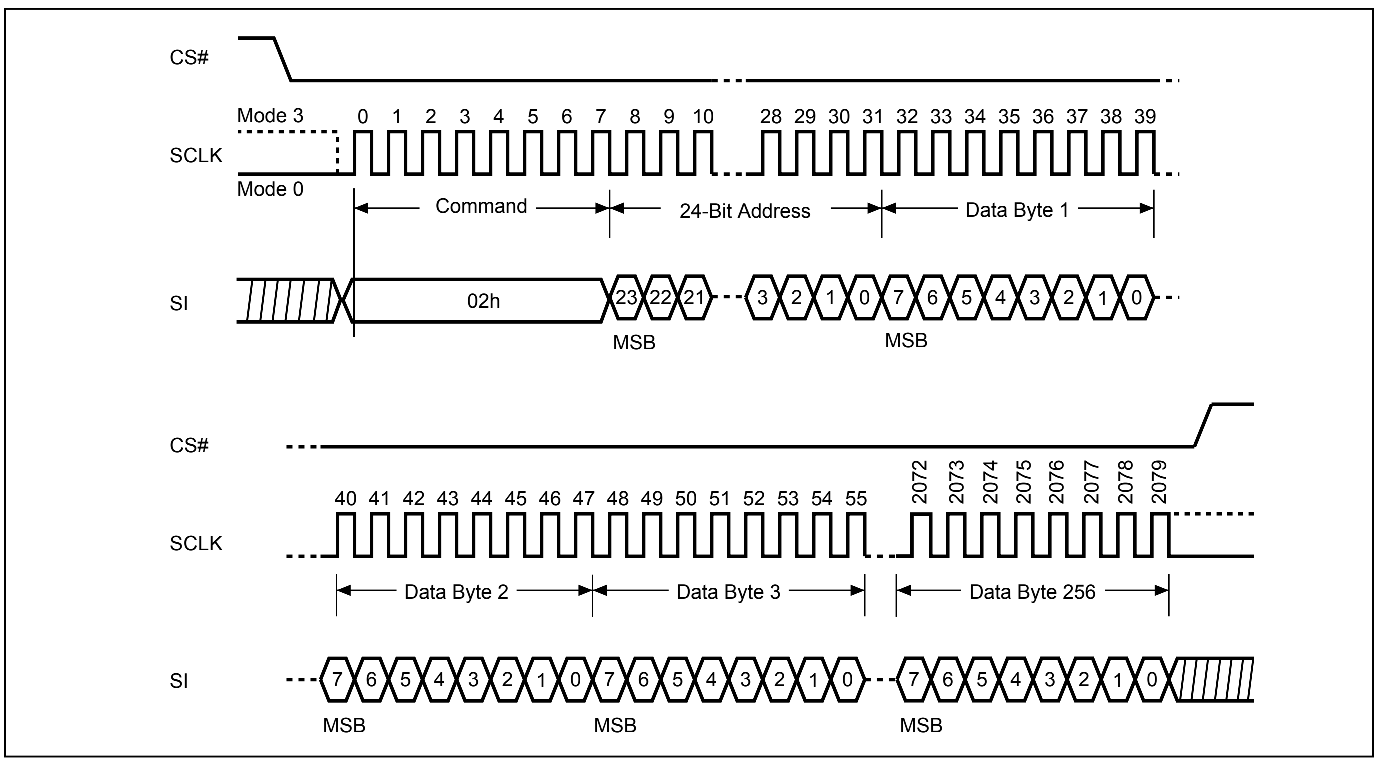
The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (The eight least significant address bits) should be set to 0. The last address byte (the 8 least significant address bits, A7-A0) should be set to 0 for 256 bytes page program. If A7-A0 are not all zero, transmitted data that exceed page length are programmed from the starting address (24-bit address that last 8 bit are all 0) of currently selected page. If the data bytes sent to the device exceeds 256, the last 256 data byte is programmed at the request page and previous data will be disregarded. If the data bytes sent to the device has not exceeded 256, the data will be programmed at the request address of the page. There will be no effort on the other data bytes of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high.

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the Block is protected by BP bits (Block Protect Mode), the Page Program (PP) instruction will not be executed.

Figure 28. Page Program (PP) Sequence



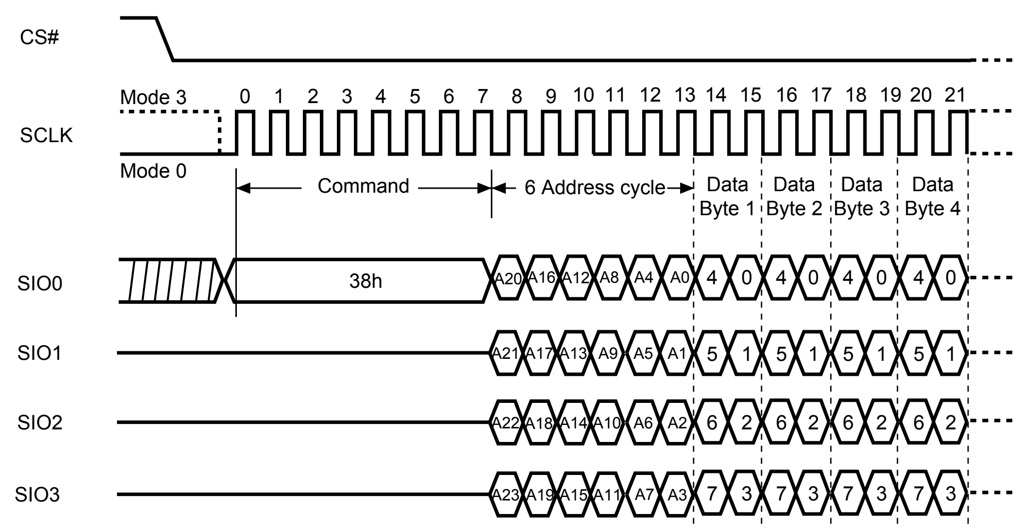
9-22. 4 x I/O Page Program (4PP)

The Quad Page Program (4PP) instruction is for programming the memory to be "0". The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3 as address and data input, which can improve programmer performance and the effectiveness of application. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→CS# goes high.

If the page is protected by BP bits (Block Protect Mode), the Quad Page Program (4PP) instruction will not be executed.

Figure 29. 4 x I/O Page Program (4PP) Sequence



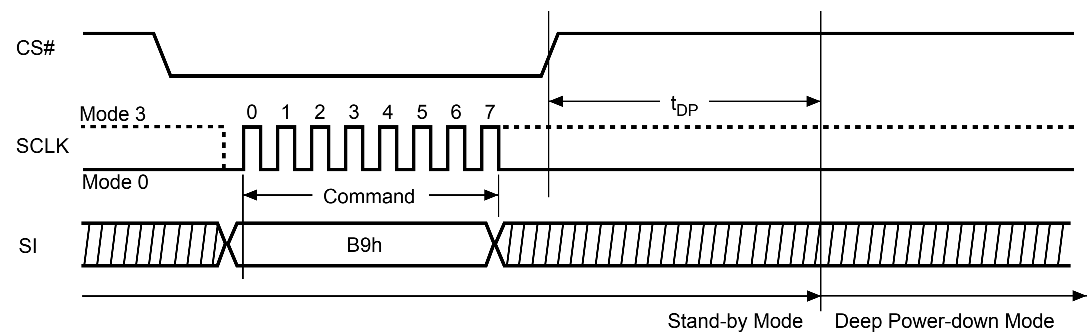
9-23. Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored. When CS# goes high, it's only in deep power-down mode not standby mode. It's different from Standby mode.

The sequence of issuing DP instruction is: CS# goes low→sending DP instruction code→CS# goes high.

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction and softreset command. (those instructions allow the ID being reading out). When Power-down, or software reset command the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For DP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode.

Figure 30. Deep Power-down (DP) Sequence



9-24. Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit secured OTP mode. While device is in 4K-bit secured OTPmode, main array access is not available. The additional 4K-bit secured OTP is independent from main array and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that after issuing ENSO command user can only access secure OTP region with standard read or program procedure. Furthermore, once security OTP is lock down, only read related commands are valid.

9-25. Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

9-26. Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→sending RDSCUR instruction→Security Register data out on SO→ CS# goes high.

9-27. Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. The WREN (Write Enable) instruction is required before issuing WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

Security Register

The definition of the Security Register bits is as below:

Erase Fail bit. The Erase Fail bit is a status flag, which shows the status of last Erase operation. It will be set to "1", if the erase operation fails. It will be set to "0", if the last operation is success. Please note that it will not interrupt or stop any operation in the flash memory.

Program Fail bit. The Program Fail bit is a status flag, which shows the status of last Program operation. It will be set to "1", if the program operation fails or the program region is protected. It will be set to "0", if the last operation is success. Please note that it will not interrupt or stop any operation in the flash memory.

Erase Suspend bit. Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

Program Suspend bit. Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit secured OTP mode, main array access is not allowed.

Table 8. Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	E_FAIL	P_FAIL	Reserved	ESB (Erase Suspend bit)	PSB (Program Suspend bit)	LDSO (indicate if lock-down)	Secured OTP indicator bit
-	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	-	0=Erase is not suspended 1= Erase suspended (default=0)	0=Program is not suspended 1= Program suspended (default=0)	0 = not lock-down 1 = lock-down (cannot program/ erase OTP)	0 = non-factory lock 1 = factory lock
Reserved	Volatile bit	Volatile bit	Reserved	Volatile bit	Volatile bit	Non-volatile bit (OTP)	Non-volatile bit (OTP)

9-28. Program/Erase Suspend/Resume

The device allow the interruption of Sector-Erase, Block-Erase or Page-Program operations and conduct other operations.

After issue suspend command, the system can determine if the device has entered the Erase-Suspended mode through Bit2 (PSB) and Bit3 (ESB) of security register. (please refer to *"Table 8. Security Register Definition"*)

For "Suspend to Read", "Resume to Read", "Resume to Suspend" timing specification please note *"Figure 31. Suspend to Read Latency", "Figure 32. Resume to Read Latency"* and *"Figure 33. Resume to Suspend Latency".*

9-29. Erase Suspend

Erase suspend allow the interruption of all erase operations. After the device has entered Erase-Suspended mode, the system can read any sector(s) or Block(s) except those being erased by the suspended erase operation. Reading the sector or Block being erase suspended is invalid.

After erase suspend, WEL bit will be clear, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 5Ah, 06h, 04h, 2Bh, 9Fh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 15h)

If the system issues an Erase Suspend command after the sector erase operation has already begun, the device will not enter Erase-Suspended mode until 20us time has elapsed.

Erase Suspend Bit (ESB) indicates the status of Erase Suspend operation. Users may use ESB to identify the state of flash memory. After the flash memory is suspended by Erase Suspend command, ESB is set to "1". ESB is cleared to "0" after erase operation resumes.

9-30. Program Suspend

Program suspend allows the interruption of all program operations. After the device has entered Program-Suspended mode, the system can read any sector(s) or Block(s) except those being programmed by the suspended program operation. Reading the sector or Block being program suspended is invalid.

After program suspend, WEL bit will be cleared, only read related, resume and reset command can be accepted. (including: 03h, 0Bh, 3Bh, 6Bh, BBh, EBh, 5Ah, 06h, 04h, 2Bh, 9Fh, 05h, ABh, 90h, B1h, C1h, B0h, 30h, 66h, 99h, 00h, 15h)

Program Suspend Bit (PSB) indicates the status of Program Suspend operation. Users may use PSB to identify the state of flash memory. After the flash memory is suspended by Program Suspend command, PSB is set to "1". PSB is cleared to "0" after program operation resumes.

Figure 31. Suspend to Read Latency

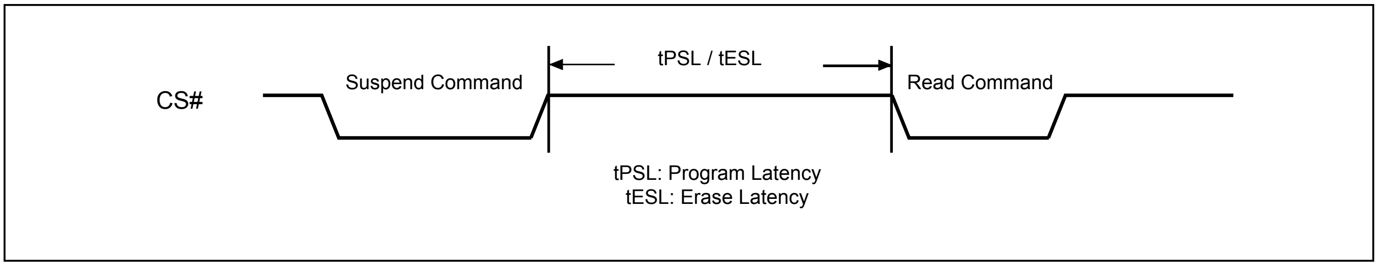


Figure 32. Resume to Read Latency

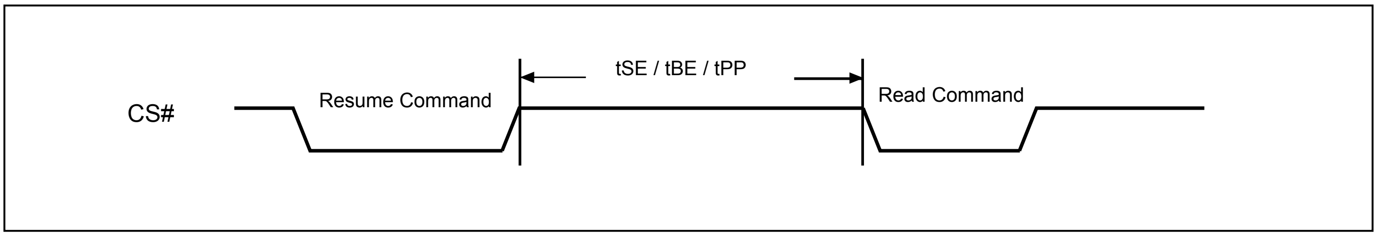
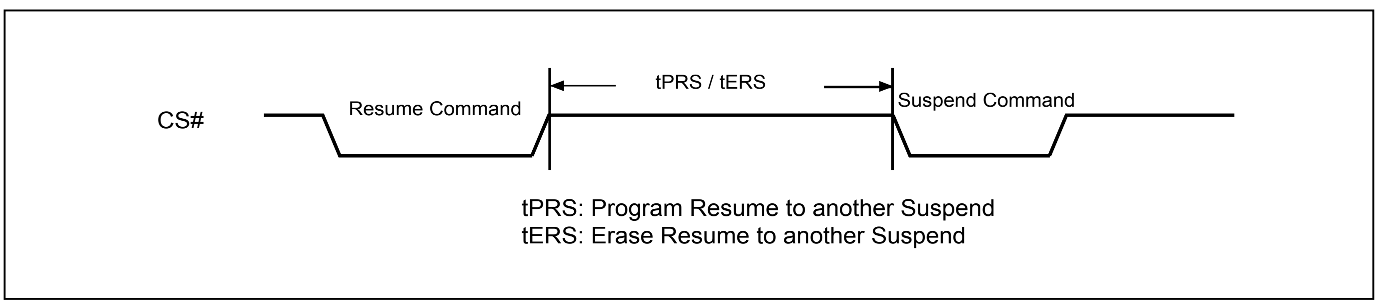


Figure 33. Resume to Suspend Latency



9-31. Write-Resume

The Write operation is being resumed when Write-Resume instruction issued. ESB or PSB (suspend status bit) in Status register will be changed back to “0”.

The operation of Write-Resume is as follows: CS# drives low → send write resume command cycle (30H) → drive CS# high. By polling Busy Bit in status register, the internal write operation status could be checked to be completed or not. The user may also wait the time lag of tSE, tBE, tPP for Sector-erase, Block-erase or Page-programming. WREN (command "06") is not required to issue before resume. Resume to another suspend operation requires latency time of 1ms.

Please note that, if "performance enhance mode" is executed during suspend operation, the device can not be resume. To restart the write command, disable the "performance enhance mode" is required. After the "performance enhance mode" is disable, the write-resume command is effective.

9-32. No Operation (NOP)

The “No Operation” command is only able to terminate the Reset Enable (RSTEN) command and will not affect any other command.

9-33. Software Reset (Reset-Enable (RSTEN) and Reset (RST))

The Software Reset operation combines two instructions: Reset-Enable (RSTEN) command following a Reset (RST) command. It returns the device to a standby mode. All the volatile bits and settings will be cleared then, which makes the device return to the default status as power on.

To execute Reset command (RST), the Reset-Enable (RSTEN) command must be executed first to perform the Reset operation. If there is any other command to interrupt after the Reset-Enable command, the Reset-Enable will be invalid.

If the Reset command is executed during program or erase operation, the operation will be disabled, the data under processing could be damaged or lost.

The reset time is different depending on the last operation. For details, please refer to *"Table 16. AC CHARACTERISTICS"* for tREADY.

Figure 34. Software Reset Recovery

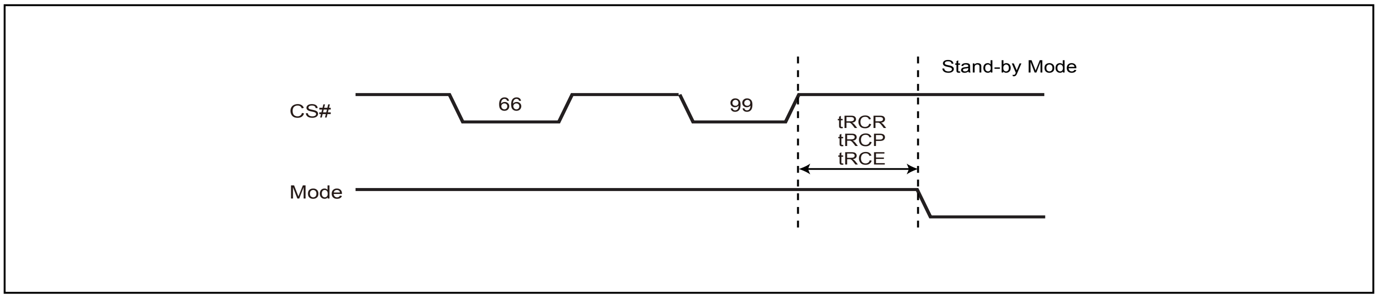
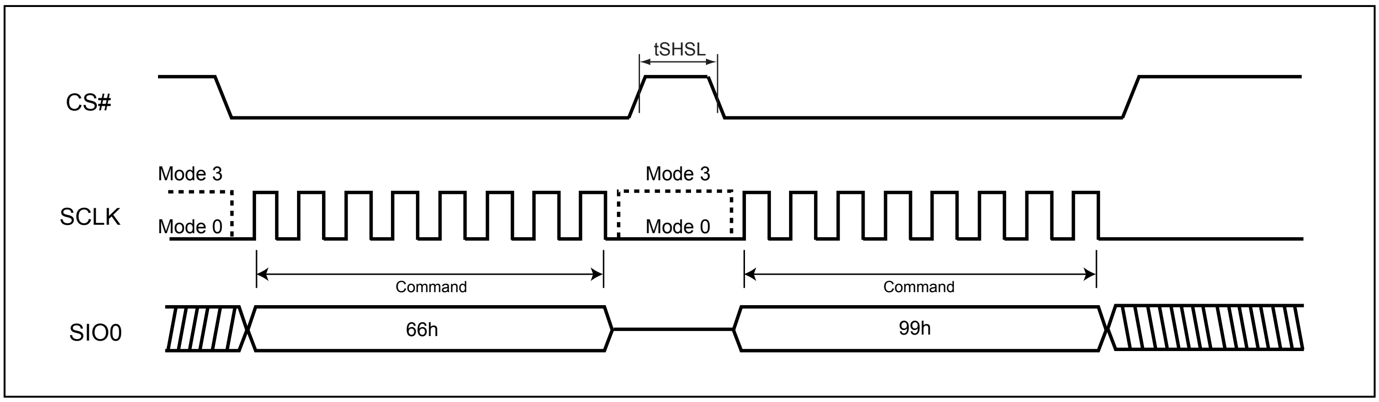


Figure 35. Reset Sequence



9-34. Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216A.

Figure 36. Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

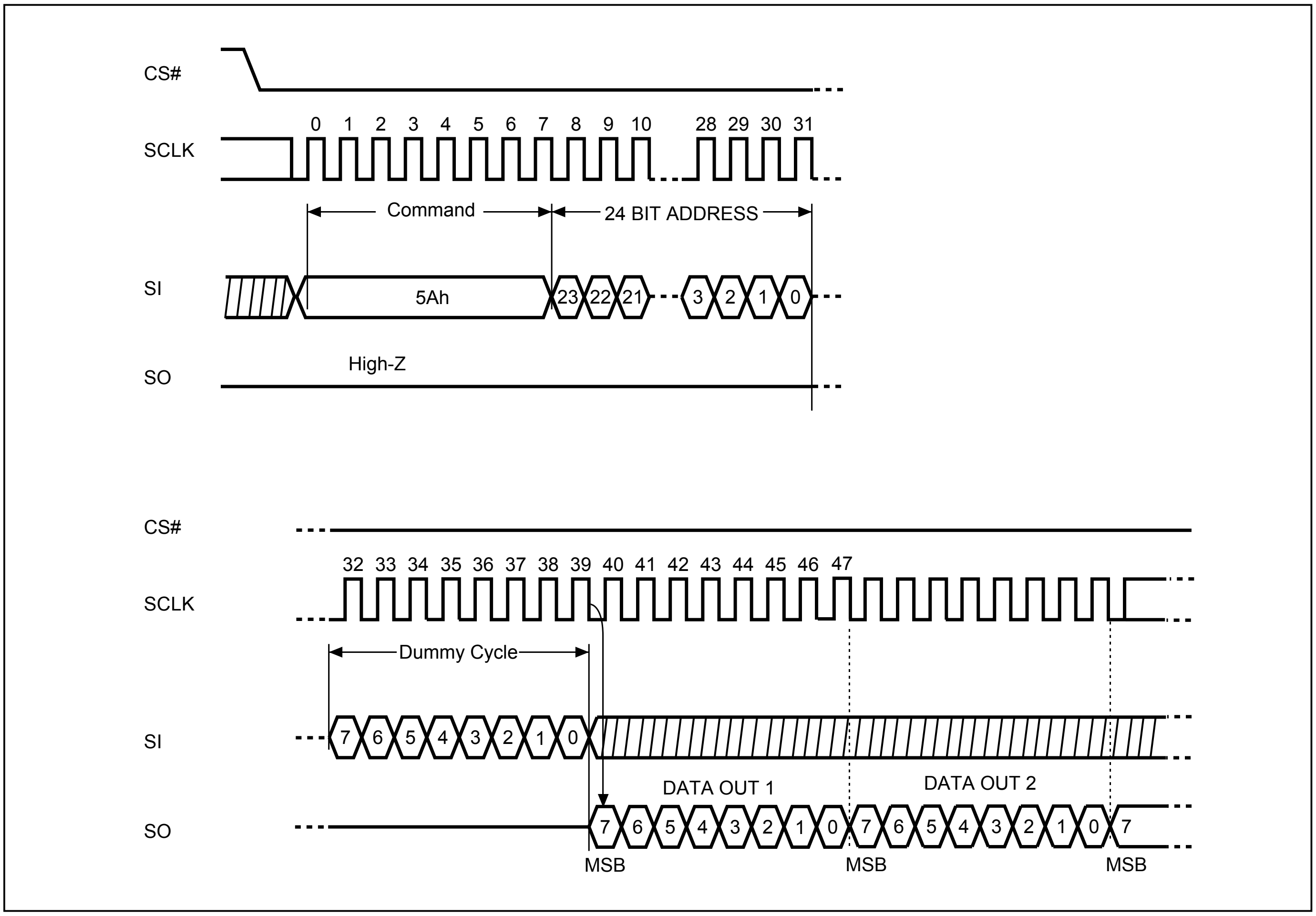


Table 9. Signature and Parameter Identification Data Values

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	05h	05h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	02h	02h
Reserved		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	05h	05h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	10h	10h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Reserved		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	10h	10h
		15h	15:08	01h	01h
		16h	23:16	00h	00h
Reserved		17h	31:24	FFh	FFh
ID number (RPMC)	RPMC parameter ID	18h	07:00	03h	03h
Parameter Table Minor Revision Number	Start from 00h	19h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	1Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	1Bh	31:24	02h	02h
Parameter Table Pointer (PTP)	First address of RPMC table	1Ch	07:00	00h	00h
		1Dh	15:08	01h	01h
		1Eh	23:16	00h	00h
Reserved		1Fh	31:24	FFh	FFh

Table 10. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not support 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Reserved	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	1b	F1h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	1b	
(1-4-4) Fast Read	0=not support 1=support		21	1b	
(1-1-4) Fast Read	0=not support 1=support		22	1b	
Reserved			23	1b	
Reserved		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	07FF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0110b: 6 dummy clocks	38h	04:00	0 0100b	44h
(1-4-4) Fast Read Number of Mode Bits (Note4)	010b: 2 mode bits		07:05	010b	
(1-4-4) Fast Read Opcode		39h	15:08	EBh	EBh
(1-1-4) Fast Read Number of Wait states	0 1000b: 8 dummy clocks	3Ah	20:16	0 1000b	08h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	6Bh	6Bh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 1000b: 8 dummy clocks	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0100b: 4 dummy clocks	3Eh	20:16	0 0100b	04h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	BBh	BBh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	EEh
Reserved			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Reserved			07:05	111b	
Reserved		43h:41h	31:08	FFh	FFh
Reserved		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not supported	46h	20:16	0 0000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not supported		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Reserved		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not supported	4Ah	20:16	0 0000b	00h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not supported		23:21	000b	
(4-4-4) Fast Read Opcode		4Bh	31:24	FFh	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes (Note5) 4KB	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 32KB	4Eh	23:16	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	31:24	52h	52h
Sector Type 3 Size	Sector/block size = 2^N bytes 64KB	50h	07:00	10h	10h
Sector Type 3 erase Opcode		51h	15:08	D8h	D8h
Sector Type 4 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Multiplier for Sector/Chip Erase Time (Maximum)	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) * Typical Time	55h:54h	03:00	0010b	7232h
Sector Type 1 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units		08:04	0 0011b	
	Units 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s		10:09	01b	
Sector Type 2 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units		15:11	0 1110b	
	Units 00: 1ms, 01: 16ms 10b: 128ms, 11b: 1s	57h:56h	17:16	01b	00F5h
Sector Type 3 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units		22:18	1 1101b	
	Units 00: 1 ms, 01: 16 ms 10b: 128ms, 11b: 1s		24:23	01b	
Sector Type 4 Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units		29:25	0 0000b	
	Units 00: 1ms, 01: 16ms 10b: 128 ms, 11b: 1 s		31:30	00b	
Multiplier for Page/Byte Program Time (Maximum)	Multiplier value: 0h~Fh (0~15) Max. time = 2 * (Multiplier + 1) *Typical Time	58h	03:00	0010b	82h
Page Program Size	Page size = 2^N bytes 2^8 = 256 bytes, 8h = 1000b		07:04	1000h	
Page Program Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	5Ah:59h	12:08	0 0101b	4225h
	Units 0: 8us, 1: 64us		13	1b	
Byte Program Time, First Byte (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units		17:14	1000b	
	Units 0: 1us, 1: 8us		18	0b	
Byte Program Time, Additional Byte (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * Units		22:19	1000b	
	Units 0: 1us, 1: 8us		23	0b	

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Chip Erase Time (Typical)	Count value: 00h~1Fh (0~31) Typical Time = (Count + 1) * Units	5Bh	28:24	1 0011b	D3h
	Units 00: 16ms, 01: 256ms 10: 4s, 11: 64s		30:29	10b	
Reserved	Reserved: 1b		31	1b	
Prohibited Operations During Program Suspend	◆ xxx0b: May not initiate a new erase anywhere ◆ xx0xb: May not initiate a new page program anywhere ◆ x1xxb: May not initiate a read in the program suspended page size ◆ 1xxxb: The erase and program restrictions in bits 1:0 are sufficient	5Ch	03:00	1100b	CCh
Prohibited Operations During Erase Suspend	◆ xxx0b: May not initiate a new erase anywhere ◆ xx1xb: May not initiate a page program in the erase suspended sector size ◆ x1xxb: May not initiate a read in the erase suspended sector size ◆ 1xxxb: The erase and program restrictions in bits 5:4 are sufficient		07:04	1100b	
Reserved	Reserved: 1b	5Eh:5Dh	08	1b	F67Fh
Program Resume to Suspend Interval (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us		12:09	1111b	
Program Suspend Latency (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units		17:13	1 0011b	
	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us		19:18	01b	
Erase Resume to Suspend Interval (Typical)	Count value: 0h~Fh (0~15) Typical Time = (Count + 1) * 64us		23:20	1111b	
Erase Suspend Latency (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units	5Fh	28:24	1 0011b	33h
	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us		30:29	01b	
Suspend / Resume supported	0= Support 1= Not supported		31	0b	
Program Resume Instruction	Instruction to Resume a Program	60h	07:00	30h	30h
Program Suspend Instruction	Instruction to Suspend a Program	61h	15:08	B0h	B0h
Erase Resume Instruction	Instruction to Resume Write/Erase	62h	23:16	30h	30h
Erase Suspend Instruction	Instruction to Suspend Write/Erase	63h	31:24	B0h	B0h

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Reserved	Reserved: 11b	64h	01:00	11b	F7h
Status Register Polling Device Busy	◆ Bit 2: Read WIP bit [0] by 05h Read instruction ◆ Bit 3: Read bit 7 of Status Register by 70h Read instruction (0=not support 1=support) ◆ Bit 07:04, Reserved: 1111b	64h	07:02	1111 01b	F7h
Release from Deep Power-down (RDP) Delay (Max.)	Count value: 00h~1Fh (0~31) Maximum Time = (Count + 1) * Units	67h:65h	12:08	0 0011b	5CD5C3h
	Units 00: 128ns, 01: 1us 10: 8us, 11: 64us		14:13	10b	
Release from Deep Power-down (RDP) Instruction	Instruction to Exit Deep Power Down		22:15	1010 1011b (ABh)	
Enter Deep Power Down Instruction	Instruction to Enter Deep Power Down		30:23	1011 1001 (B9h)	
Deep Power Down Supported	0: Supported 1: Not supported		31	0b	
4-4-4 Mode Disable Sequences	Supported Methods to Reset QPI Mode ◆ xx1xb: issue F5h instruction	69h:68h	03:00	0000b	FF00h
4-4-4 Mode Enable Sequences	Supported methods to enter QPI mode ◆ x_x1xxb: issue instruction 35h ◆ 1_xxxxb: Reserved		08:04	1 0000b	
0-4-4 mode Supported	Performance Enhance Mode, Continuous Read, Execute in Place 0: Not supported 1: Supported		09	1b	
0-4-4 Mode Exit Method	Exit Performance Enhance Mode ◆ xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read peration. ◆ xx_x1xxb: Reserved ◆ x1_xxxxb: Reserved ◆ 1x_xxxxb: Reserved		15:10	11 1111b	
0-4-4 Mode Entry Method	Enter Performance Enhance Mode ◆ xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode ◆ x1xxb: Reserved ◆ 1xxxb: Reserved	6Ah	19:16	1101h	2Dh
Quad Enable (QE) bit Requirements	◆ 010b: QE is bit 6 of Status Register. where 1=Quad Enable or 0=not Quad Enable		22:20	010b	
HOLD and WP Disable by bit 4 of Extended Configuration Register	0: Not supported		23	0b	
Reserved		6Bh	31:24	FFh	FFh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Volatile or Non-Volatile Register and Write Enable Instruction for Status Register 1	◆ xxx_xxx1b: Non-Volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write ◆ x1x_xxxxb: Reserved ◆ 1xx_xxxxb: Reserved	6Ch	06:00	110 0001b	E1h
Reserved			07	1b	
Soft Reset and Rescue Sequence Support	Return the device to its default power-on state ◆ x1_xxxxb: issue reset enable instruction 66h, then issue reset instruction 99h.	6Dh	13:08	11 0000b	30h
Exit 4-Byte Addressing	◆ xx_xxxx_xxx1b: issue instruction E9h to exit 4-Byte address mode (write enable instruction 06h is not required) ◆ xx_xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:A24] bits. Read with instruction C8h. Write instruction is C5h, data length is 1 byte. Return to lowest memory segment by setting A[31:24] to 00h and use 3-Byte addressing. ◆ xx_xx1x_xxxxb: Hardware reset ◆ xx_x1xx_xxxxb: Software reset (see bits 13:8 in this DWORD) ◆ xx_1xxx_xxxxb: Power cycle ◆ x1_xxxx_xxxxb: Reserved ◆ 1x_xxxx_xxxxb: Reserved		15:14	00b	
		6Eh	23:16	1100 0000b	C0h

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Enter 4-Byte Addressing	◆ xxxx_xxx1b: issue instruction B7h (preceding write enable not required) ◆ xxxx_x1xxb: 8-bit volatile extended address register used to define A[31:24] bits. Read with instruction C8h. Write instruction is C5h with 1 byte of data. Select the active 128 Mbit memory segment by setting the appropriate A[31:24] bits and use 3-Byte addressing. ◆ xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Consult vendor data sheet for the instruction set definition. ◆ 1xxx_xxxxb: Reserved	6Fh	31:24	1000 0000b	80h

Table 11. RPMC Parameter

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Flash_Hardening	0=Flash Hardening is supported. 1=Flash Hardening is not supported	100h	00	0b	3Ch
MC_Size	0= Monotonic counter size is 32 bit 1= Reserved		01	0b	
Busy_Polling_Method :	0= Poll for OP1 busy using OP2 Extended Status[0] 1= Poll for OP1 busy using Status		02	1b	
Reserved			03	1b	
Num_Counter-1:	Number of supported counters-1.		07:04	0011b	
OP1 Opcode		101h	15:08	9Bh	9Bh
OP2 Opcode		102h	23:16	96h	96h
Update_Rate	: Rate of Update = 5 * (2 ^ Update_Rate) seconds	103h	27:24	0000b	F0h
Reserved	: Must be 0FH		31:28	Fh	
Read Counter Polling Delay Typical case to calculate HMAC two times	0 : polling delay_read counter	104h	04:00	00101b	C5h
	units (00=1us, 01=16us, 10=128us, 11=1ms)		06:05	10b	
	reserved		07	1b	
Write Counter Polling Short Delay	0 : polling_short_delay_write_counter	105h	12:08	00100b	A4h
	units (00=1us, 01=16us, 10=128us, 11=1ms)		14:13	01b	
	reserved		15	1b	
Write Counter Polling Long Delay	Bits4:0 : polling_long_delay_write_counter	106h	20:16	00010b	C2h
	Bits 6:5 : units (00=1ms, 01=16ms,10=128ms, 11= 1s)		22:21	10b	
	Bit 7 : reserved		23	1b	
Reserved	: Must be FF	107h	31:24	FFh	FFh

Table 12. Parameter Table (1): Macronix Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	111h:110h	07:00 15:08	00h 36h	00h 36h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	113h: 112h	23:16 31:24	00h 27h	00h 27h
H/W Reset# pin	0=not support 1=support	115h: 114h	00	0b	799Ch
H/W Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
S/W Reset	0=not support 1=support		03	1b	
S/W Reset Opcode	Reset Enable (66h) should be issued before Reset Opcode		11:04	1001 1001b (99h)	
Program Suspend/Resume	0=not support 1=support		12	1b	
Erase Suspend/Resume	0=not support 1=support		13	1b	
Reserved			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		116h	23:16	FFh	FFh
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	117h	31:24	FFh	FFh
Individual block lock	0=not support 1=support	11Bh: 118h	00	0b	CBFCh
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	FFh	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Reserved			15:14	11b	
Reserved			31:16	FFh	FFh
Reserved		11Fh: 11Ch	31:00	FFh	FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh for SFDP Tables that are defined in Parameter Identification Header. All other areas beyond defined SFDP Table are reserved by Macronix.

10. POWER-ON STATE

The device is at below states when power-up:

- Standby mode (please note it is not deep power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage unless the VCC achieves below correct level:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal power-on reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state. When VCC is lower than VWI (POR threshold voltage value), the internal logic is reset and the flash device has no response to any command.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the below time delay:

- tVSL after VCC reached VCC minimum level

Please refer to the *"Figure 43. Power-up Timing"*.

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)
- At power-down stage, the VCC drops below VWI level, all operations are disable and device has no response to any command. The data corruption might occur during the stage while a write, program, erase cycle is in progress.

11. ELECTRICAL SPECIFICATIONS

Table 13. ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to VCC+0.5V
Applied Output Voltage		-0.5V to VCC+0.5V
VCC to Ground Potential		-0.5V to 4.0V

NOTICE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see *Figure 37*, and *Figure 38.*

Figure 37. Maximum Negative Overshoot Waveform

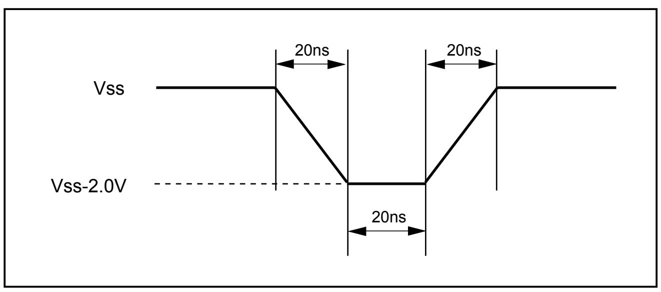


Figure 38. Maximum Positive Overshoot Waveform

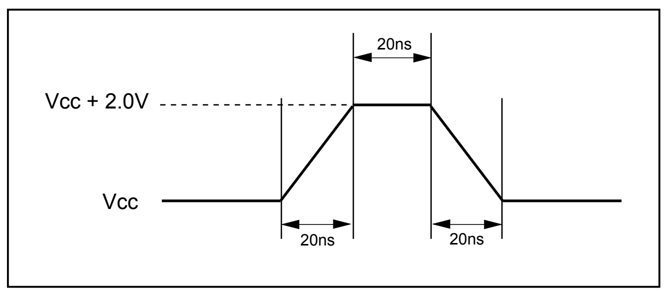


Table 14. CAPACITANCE TA = 25°C, f = 1.0 MHz

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 39. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL

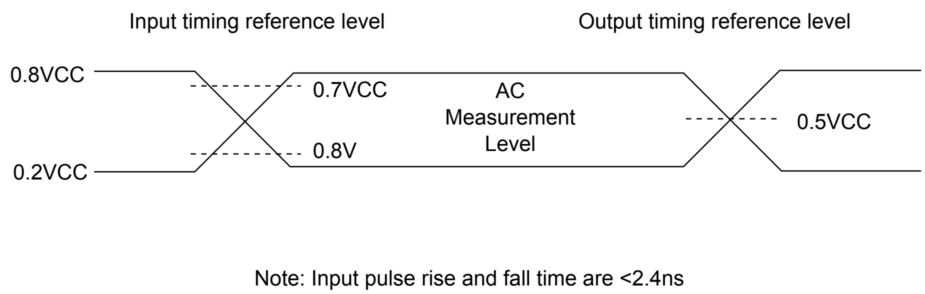


Figure 40. OUTPUT LOADING

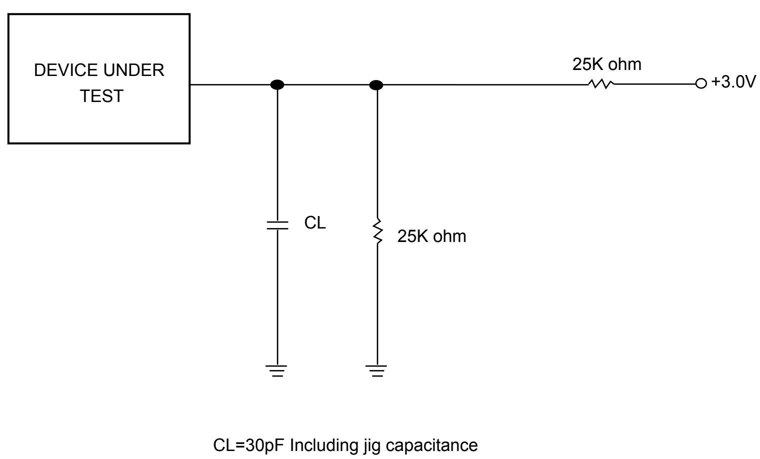


Table 15. DC CHARACTERISTICS

(Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Units	Test Conditions
ILI	Input Load Current	1			±2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			±2	uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		10	60	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			3	20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		10	17	mA	f=84MHz, (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		15	25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			15	20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector/Block (32K, 64K) Erase Current (SE/BE/BE32K)	1		15	25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		15	25	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8	V	
VIH	Input High Voltage		0.7VCC		VCC+0.4	V	
VOL	Output Low Voltage				0.2	V	IOL = 100uA
VOH	Output High Voltage		VCC-0.2			V	IOH = -100uA

Notes :
1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 16. AC CHARACTERISTICS

(Temperature = -40°C to 85°C, VCC = 2.7V ~ 3.6V)

Symbol	Alt.	Parameter		Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for all commands (FAST_READ, RDSFDP, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR)		D.C.		104	MHz
fRSCLK	fR	Clock Frequency for READ instructions				54	MHz
fTSCLK		Clock Frequency for DREAD, 2READ, QREAD, 4READ instructions				84	MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK)	3.3			ns
			Normal Read (fRSCLK)	9			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK)	3.3			ns
			Normal Read (fRSCLK)	9			ns
tCLCH(2)		Clock Rise Time (peak to peak)		0.1			V/ns
tCHCL(2)		Clock Fall Time (peak to peak)		0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)		5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)		7			ns
tDVCH	tDSU	Data In Setup Time		2			ns
tCHDX	tDH	Data In Hold Time		3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)		5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)		5			ns
tSHSL	tCSH	CS# Deselect Time	Read	7			ns
			Write/Erase/Program	30			ns
tSHQZ(2)	tDIS	Output Disable Time				8	ns
tCLQV	tV	Clock Low to Output Valid Loading: 30pF/15pF	Loading: 30pF			8	ns
			Loading: 15pF			6	ns
tCLQX	tHO	Output Hold Time		1			ns
tDP(2)		CS# High to Deep Power-down Mode				10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read				30	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read				30	us
tW		Write Status/Configuration Register Cycle Time				40	ms
tBP		Byte-Program			10	50	us
tPP		Page Program Cycle Time			0.33	1.2	ms
tPP(4)		Page Program Cycle Time (n bytes)			0.008+ (nx0.004) (5)	1.2	ms
tSE		Sector Erase Cycle Time			25	200	ms
tBE32		Block Erase (32KB) Cycle Time			140	600	ms
tBE		Block Erase (64KB) Cycle Time			250	1000	ms
tCE		Chip Erase Cycle Time			40	120	s
tWRK		Write Root Key Time			180	510	us
tUHK		Update HMAC Key Time			315	445	us
tIMC		Increment Monotonic Counter Time			0.045	300	ms
tRQMC		Request Monotonic Counter Time			65	105	us
tRSL		Suspend during OP1 command to suspend ready time			20		us
tRSP		Resume to suspend timing for OP1 command			1		ms
tESL(6)		Erase Suspend Latency				20	us
tPSL(6)		Program Suspend Latency				20	us
tPRS(7)		Latency between Program Resume and next Suspend		0.3	1000		us
tERS(8)		Latency between Erase Resume and next Suspend		0.3	1000		us

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tRCR		Recovery Time from Read	20			us
tRCP		Recovery Time from Program	20			us
tRCE		Recovery Time from Erase	12			ms

Notes:
1. tCH + tCL must be greater than or equal to 1/ Frequency.
2. Typical values given for TA=25°C. Not 100% tested.
3. Test condition is shown as *Figure 39* and *Figure 40*.
4. While programming consecutive bytes, Page Program instruction provides optimized timings by selecting to program the whole 256 bytes or only a few bytes between 1~256 bytes.
5. “n”=how many bytes to program. In the formula, while n=1, byte program time=12us.
6. Latency time required to complete Erase/Program Suspend operation until WIP bit is "0".
7. For tPRS, Min. timing is needed to issue next program suspend command. However, a period of time equal to/or longer than typ. timing is also required to complete the program progress.
8. For tERS, Min. timing is needed to issue next erase suspend command. However, a period of time equal to/or longer than typ. timing is also required to complete the erase progress.

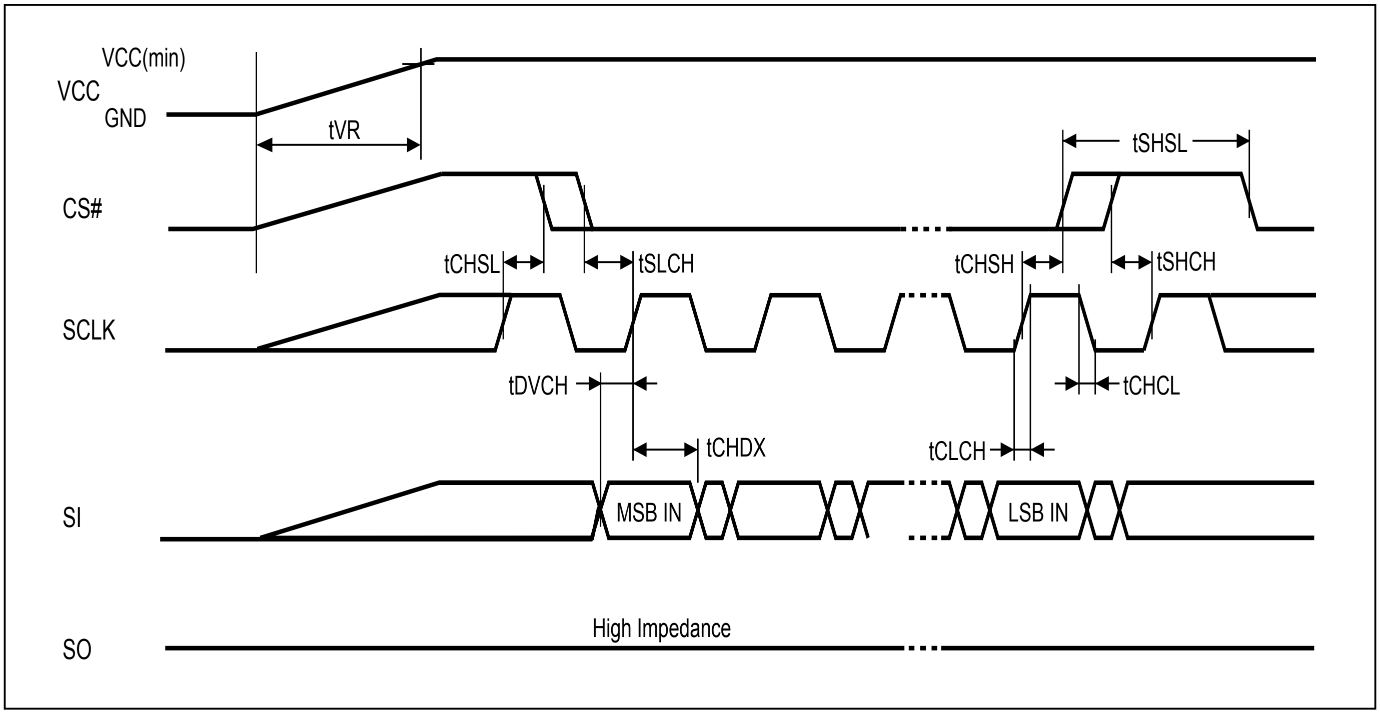
12. OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *"Figure 41. AC Timing at Device Power-Up"* and *"Figure 42. Power-Down Sequence"* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 41. AC Timing at Device Power-Up



Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 16. AC CHARACTERISTICS"*.

Figure 42. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.

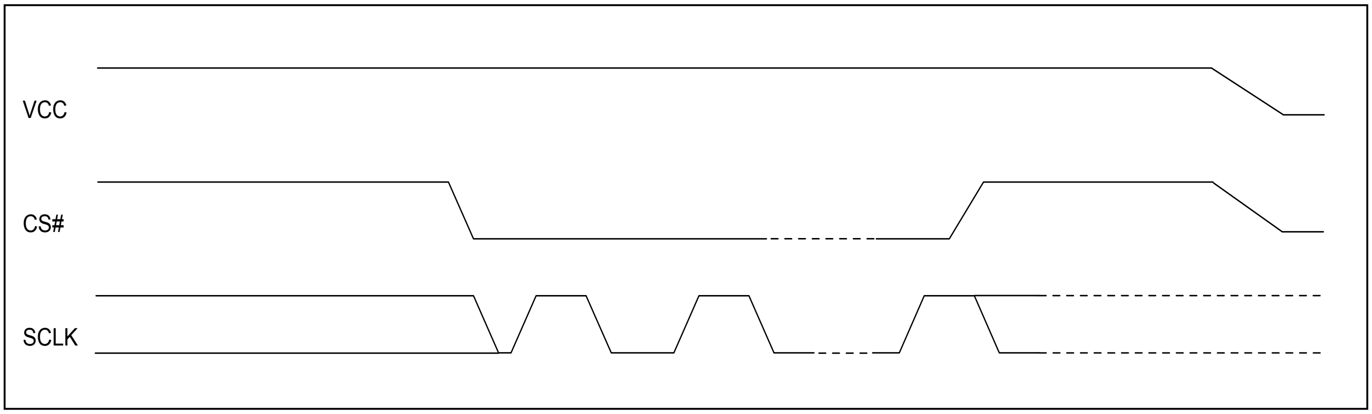


Figure 43. Power-up Timing

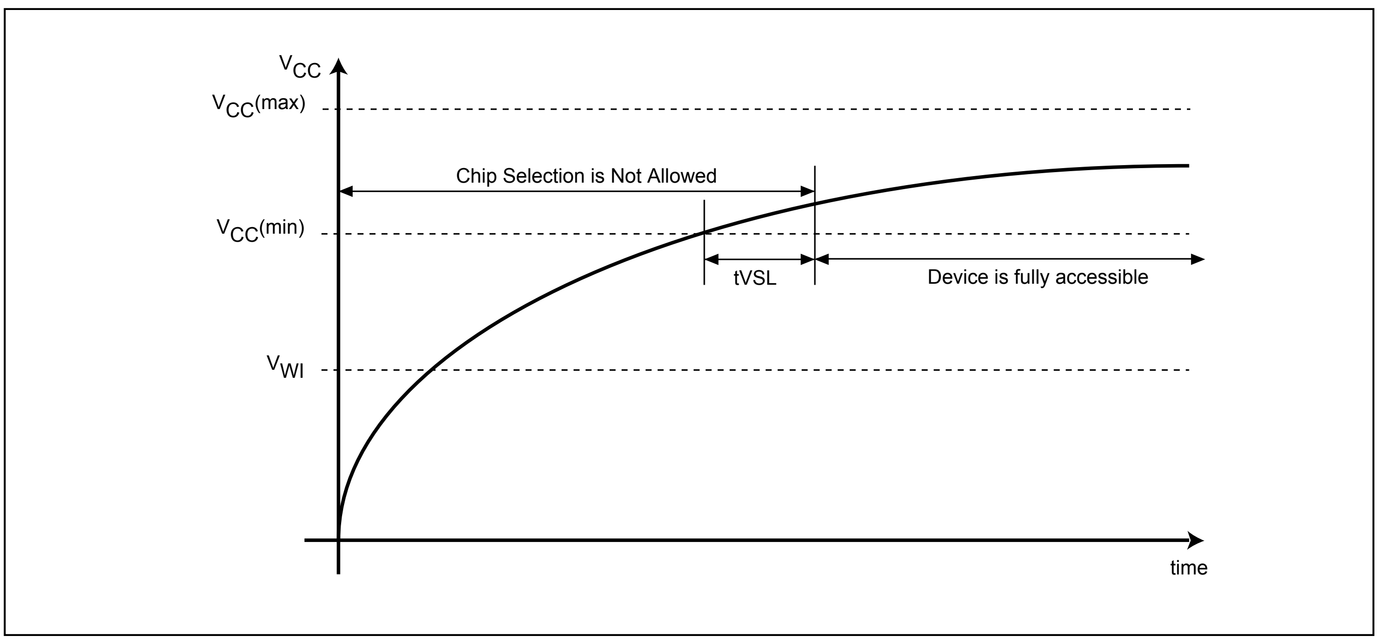


Figure 44. Power Up/Down and Voltage Drop

For Power-down to Power-up operation, the VCC of flash device must below V_{PWD} for at least tPWD timing. Please check the table below for more detail.

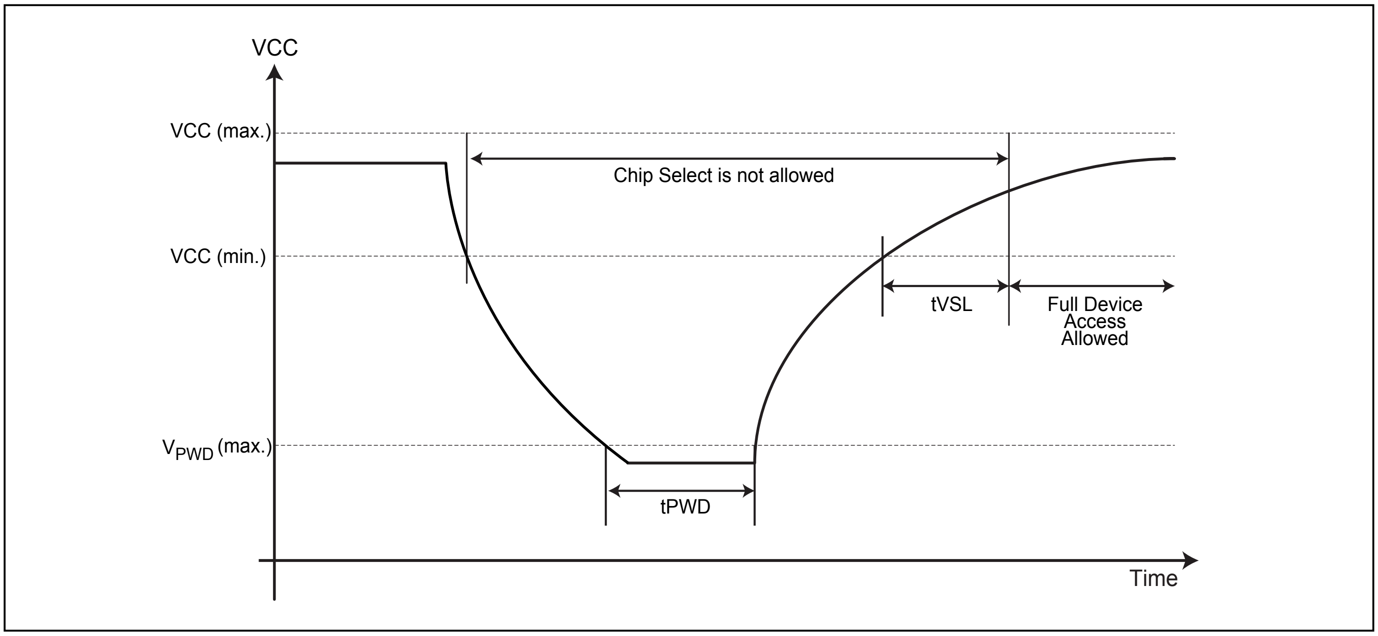


Table 17. Power-Up/Down Voltage and Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC(min.) to device operation	800		us
VWI	Write Inhibit Voltage	1.5	2.5	V
V_{PWD}	VCC voltage needed to below V_{PWD} for ensuring initialization will occur		0.9	V
tPWD	The minimum duration for ensuring initialization will occur	300		us
tVR	VCC Rise Time	20	500000	us/V
VCC	VCC Power Supply	2.7	3.6	V

Note: These parameters are characterized only.

12-1. INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 40h (all Status Register bits are 0, , except QE bit: QE=1).

13. ERASE AND PROGRAMMING PERFORMANCE

Parameter	Min.	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time			40	ms
Sector Erase Cycle Time (4KB)		25	200	ms
Block Erase Cycle Time (32KB)		0.14	0.6	s
Block Erase Cycle Time (64KB)		0.25	1	s
Chip Erase Cycle Time		40	120	s
Byte Program Time (via page program command)		10	50	us
Page Program Time		0.33	1.2	ms
Erase/Program Cycle		100,000		cycles

Note:
1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and all zero pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.
4. The maximum chip programming time is evaluated under the worst conditions of 0°C, VCC=3.3V, and 100K cycle with 90% confidence level.

14. DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

15. LATCH-UP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

16. ORDERING INFORMATION

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25L12850FM2I-10G	104	-40°C~85°C	8-SOP (200mil)	
MX25L12850FZNI-10G	104	-40°C~85°C	8-WSON (6x5mm)	
MX25L12850FPI-10G	104	-40°C~85°C	8-PDIP (300mil)	

17. PART NAME DESCRIPTION

MX 25 L 12850F M2 I - 10 G

OPTION:
G: RoHS Compliant & Halogen-free

SPEED:
10: 104MHz

TEMPERATURE RANGE:
I: Industrial (-40°C to 85°C)

PACKAGE:
M2: 8-SOP (200mil)
ZN: 8-WSON (6x5mm)
P: 8-PDIP (300mil)

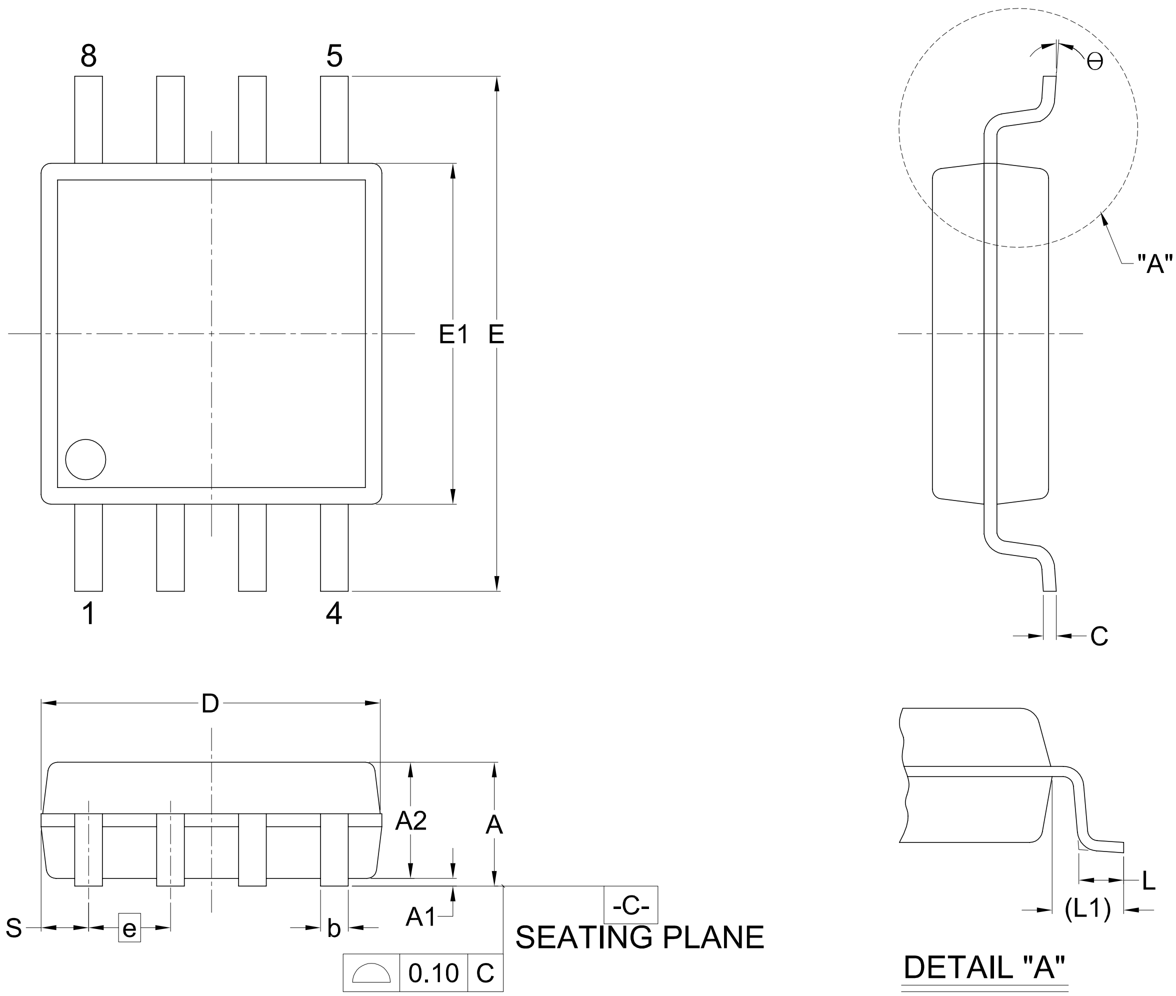
DENSITY & MODE:
12850F: 128Mb

TYPE:
L: 3V

DEVICE:
25: Serial Flash

18. PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)

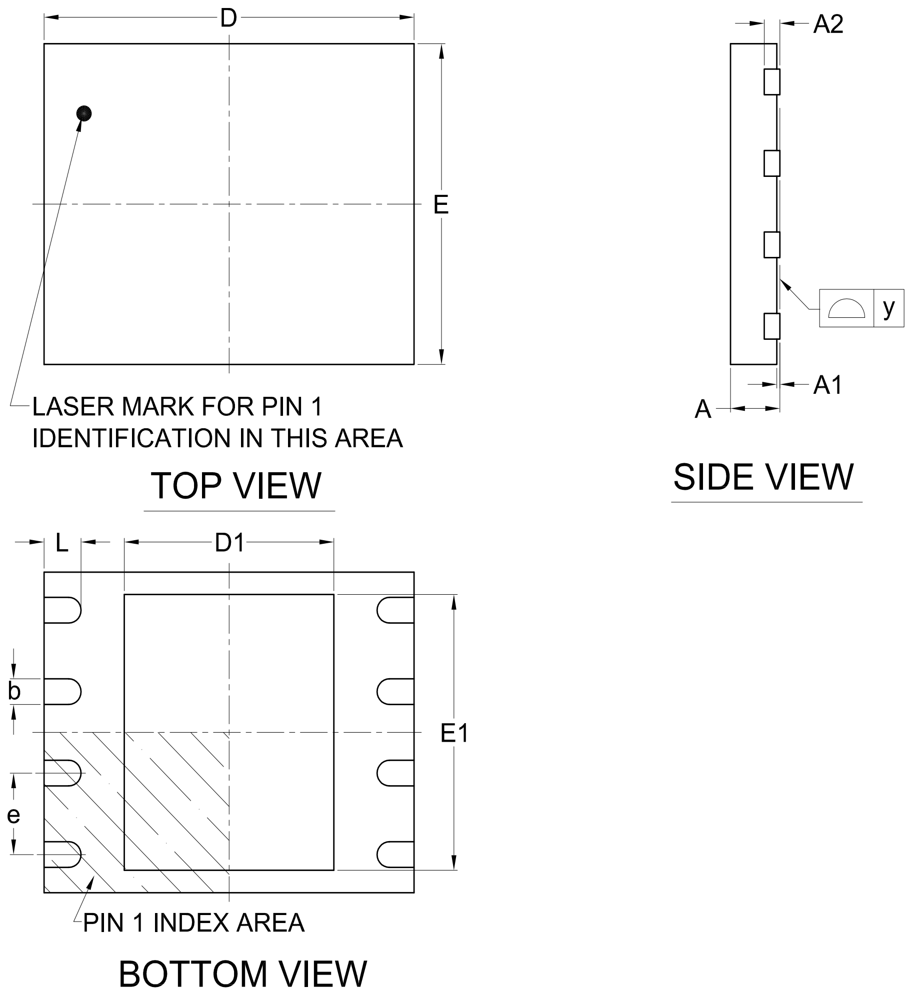


Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8°

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	5				

Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



Note:

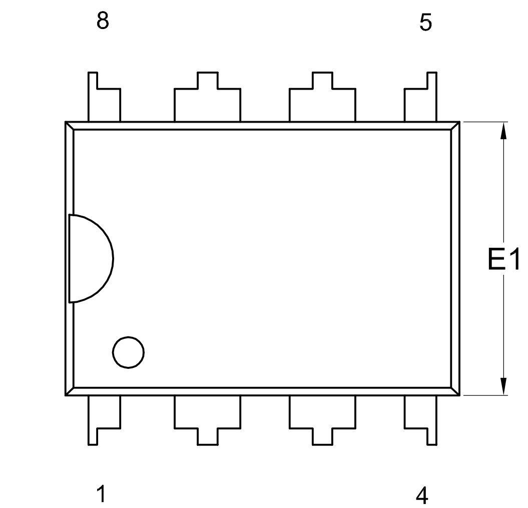
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

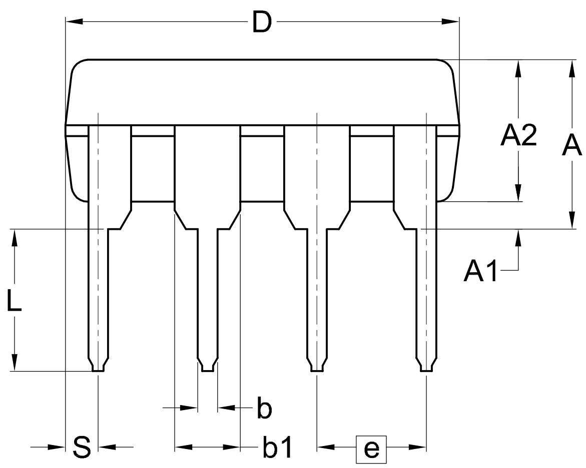
Dimensions (inch dimensions are derived from the original mm dimensions)

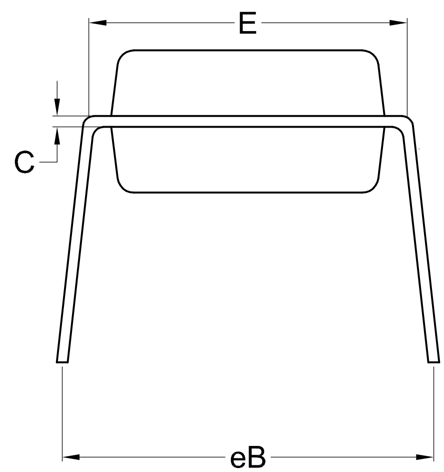
UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.30	4.90	3.90	0.50	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.50	5.10	4.10	0.75	---	0.08
Inch	Min.	0.028	---	---	0.014	0.232	0.129	0.193	0.154	0.020	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.138	0.201	0.161	0.030	---	0.003

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3401	6	MO-220			

Doc. Title: Package Outline for PDIP 8L (300MIL)







Dimensions (inch dimensions are derived from the original mm dimensions)

UNIT \ SYMBOL		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.38	3.18	0.36	1.14	0.20	9.02	7.62	6.22	---	7.87	2.92	0.76
	Nom.	---	---	3.30	0.46	1.52	0.25	9.27	7.87	6.35	2.54	8.89	3.30	1.14
	Max.	5.33	---	3.43	0.56	1.78	0.36	10.16	8.13	6.48	---	9.53	3.81	1.52
Inch	Min.	---	0.015	0.125	0.014	0.045	0.008	0.355	0.300	0.245	---	0.310	0.115	0.030
	Nom.	---	---	0.130	0.018	0.060	0.010	0.365	0.310	0.250	0.100	0.350	0.130	0.045
	Max.	0.210	---	0.135	0.022	0.070	0.014	0.400	0.320	0.255	---	0.375	0.150	0.060

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-0201	7	MS-001			

19. REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Advanced Information"	All	DEC/08/2014
	2. Modified Support fast clock frequency for read operation	P4,72	
	3. Added parameters name for Suspend/Resume	P52,53,72,73	
	4. Updated AC/DC and VWI values (Removed tWREAW) and updated Sector Erase Cycle Time	P71,72,76,77	
	5. Content correction	P13,55,70,76	

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