MX25L6433F- J/K Grade

3V, 64M-BIT [x 1/x 2/x 4]
CMOS MXSMIO® (SERIAL MULTI I/O)
FLASH MEMORY

Key Features

- *J Grade (Temperature = -40°C to 105°C)*
- *K Grade (Temperature = -40°C to 125°C)*
- *Hold Feature*
- *Multi I/O Support - Single I/O, Dual I/O and Quad I/O*
- *Auto Erase and Auto Program Algorithms*
- *Program Suspend/Resume & Erase Suspend/Resume*

64M-BIT [x 1 / x 2 / x 4] CMOS MXSMIO® (SERIAL MULTI I/O) FLASH MEMORY

1. FEATURES

GENERAL

- Supports Serial Peripheral Interface -- Mode 0 and Mode 3
- 67,108,864 x 1 bit structure
  or 33,554,432 x 2 bits (two I/O read mode) structure
  or 16,777,216 x 4 bits (four I/O mode) structure
- 2048 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 256 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 128 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.65-3.6 volts for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V
- Supports Performance Enhance Mode - XIP (execute-in-place)
- Fast read for SPI mode
  - Supports Fast Read, 2READ, DREAD, 4READ, QREAD instructions
  - Configurable dummy cycle number for fast read operation
- Programming: 256byte page buffer
- Minimum 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - Block lock protection
    The BP0-BP3 and T/B status bits define the size of the area to be protected against program and erase instructions
- Additional 8K-bit bit secured OTP
  - Features unique identifier
  - Factory locked identifiable, and customer lockable
- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programmed should have page in the erased state first.)
- Status Register Feature
- Command Reset
- Program/Erase Suspend
- Program/Erase Resume
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
- Supports Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O mode or Serial Data Input/Output for 4 x I/O mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O mode or Serial Data Input/Output for 4 x I/O mode
- WP#/SIO2
  - Hardware Write Protection or Serial Data Input/Output for 4 x I/O mode
- HOLD#/SIO3
  - To pause the device without deselecting the device or Serial Data Input/Output for 4 x I/O mode
- PACKAGE
  - 8-pin SOP (200mil)
  - 16-pin SOP (300mil)
  - 8-WSON (6x5mm)
  - 8-WSON (8x6mm)
  - 24 ball TFBGA (6x8mm)
  - **All devices are RoHS Compliant and Halogen-free**

2. GENERAL DESCRIPTION

MX25L6433F is 64Mb bits Serial NOR Flash memory, which is configured as 8,388,608 x 8 internally. When it is in four I/O mode, the structure becomes 16,777,216 bits x 4. When it is in two I/O mode, the structure becomes 33,554,432 bits x 2.

MX25L6433F features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus while it is in single I/O mode. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L6433F, MXSMIO® (Serial Multi I/O) flash memory, provides sequential read operation on the whole chip and multi-I/O features.

When it is in quad I/O mode, the SI pin, SO pin, WP# pin and HOLD# pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis. Erase command is executed on 4K-byte sector, 32K-byte/64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit.

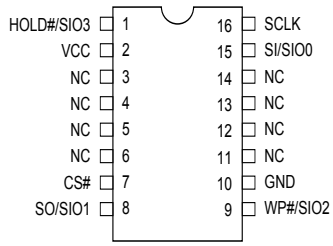
When the device is not in operation and CS# is high, it will remain in standby mode.

The MX25L6433F utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

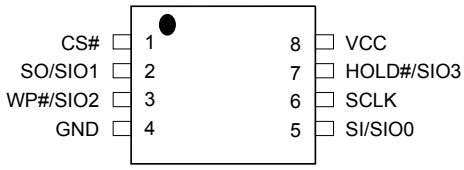
For detailed electrical specifications, please refer to MX25L6433F datasheet.

3. PIN CONFIGURATION

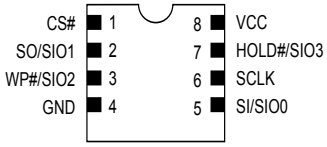
16-PIN SOP (300mil)



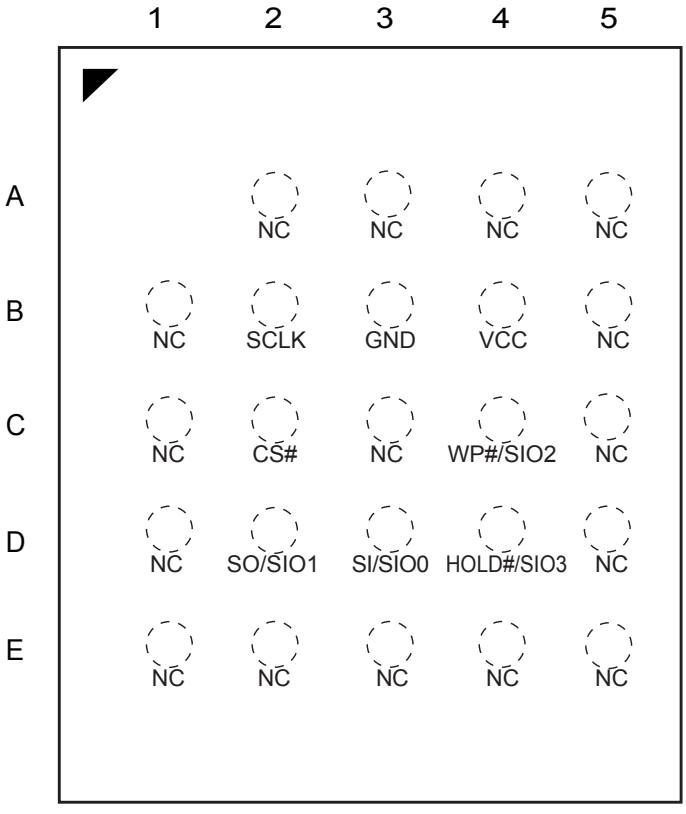
8-PIN SOP (200mil)



8-WSON (6x5mm, 8x6mm)



24-Ball TFBGA (6x8 mm with 5x5 Ball Array)



4. PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O mode and 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection Active Low or Serial Data Input & Output (for 4xI/O mode)
HOLD#/ SIO3	To pause the device without deselecting the device or Serial data Input/Output for 4 x I/O mode
VCC	+ 3.0V Power Supply
GND	Ground
NC	No Connection

Note: The pin of HOLD#/SIO3 or WP#/SIO2 will remain internal pull up function while this pin is not physically connected in system configuration.
However, the internal pull up function will be disabled if the system has physical connection to HOLD#/SIO3 or WP#/SIO2 pin.

5. CONFIGURATION REGISTER

The Configuration Register is able to change the default status of Flash memory. Flash memory will be configured after the CR bit is set.

ODS bit
The output driver strength ODS bit are volatile bits, which indicate the output driver level of the device. The Output Driver Strength is defaulted=1 when delivered from factory. To write the ODS bit requires the Write Status Register (WRSR) instruction to be executed.

TB bit
The Top/Bottom (TB) bit is a OTP bit. The Top/Bottom (TB) bit is used to configure the Block Protect area by BP bit (BP3, BP2, BP1, BP0), starting from TOP or Bottom of the memory array. The TB bit is defaulted as “0”, which means Top area protect. When it is set as “1”, the protect area will change to Bottom area of the memory device. To write the TB bit requires the Write Status Register (WRSR) instruction to be executed.

Table 1. Configuration Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Reserved	DC (Dummy Cycle)	Reserved	Reserved	TB (top/bottom selected)	Reserved	Reserved	ODS
x	2READ/ 4READ Dummy Cycle	x	x	0=Top area protect 1=Bottom area protect (Default=0)	x	x	0,Output driver strength=1 1,Output driver strength=1/4 (Default=0)
x	volatile	x	x	OTP	x	x	volatile

Note: Please refer to *"Table 2. Dummy Cycle Table"*, with "Don't Care" on other Reserved Configuration Registers.

Table 2. Dummy Cycle Table

	DC	Numbers of Dummy Cycles	Freq. (MHz)	
			105°C	125°C
2READ	0 (default)	4	80	80
	1	8	133	120
4READ	0 (default)	6	80	80
	1	10	133	120

6. ELECTRICAL SPECIFICATIONS

Table 3. DC Characteristics

Temperature = -40°C to 105°C/125°C ; VCC = 2.65V - 3.6V

Symbol	Parameters	Notes	Min.	Typ.	Max.(4)		Units	Test Conditions
					105°C	125°C		
ILI	Input Load Current	1			± 2		uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1			± 2		uA	VCC = VCC Max, VOUT = VCC or GND
ISB1	VCC Standby Current	1		10	85	100	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			3	25	30	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		2.5	7	10	mA	Normal Read (50MHz), SCLK=0.1VCC/0.9VCC, SO=Open
		1,5		10	22	25	mA	4 IxO Read, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		10	15		mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			10	15		mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		10	15		mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		10	15		mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5		0.8		V	
VIH	Input High Voltage		0.7VCC		VCC+0.4		V	
VOL	Output Low Voltage				0.4		V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2				V	IOH = -100uA

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.
3. The values are guaranteed by characterization, not 100% tested in production.
4. Under worst conditions from -40°C to 105°C/125°C and 2.65V.
5. For ICC1 4I/O Read frequency, please refer to the values of fTSCLK in *"Table 4. AC Characteristics"*.

Table 4. AC Characteristics

Temperature = -40°C to 105°C/125°C ; VCC = 2.65V - 3.6V

Symbol	Alt.	Parameters			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, PP, SE, BE32K, BE, CE, RES, WREN, WRDI, RDID, RDSR, WRSR			D.C.		133 (105°C) 120 (125°C)	MHz
fTSCLK	fT	Clock Frequency for 2READ/DREAD instructions						MHz
	fQ	Clock Frequency for 4READ/QREAD instructions						MHz
f4PP		Clock Frequency for 4PP (Quad page program)						MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
tCH(1)	tCLH	Clock High Time	Others (fSCLK/fTSCLK)	> 50MHz	45% x (1/fSCLK)			ns
					45% x (1/fTSCLK)			ns
				≤ 50MHz	9			ns
			Normal Read (fRSCLK)		9			ns
tCL(1)	tCLL	Clock Low Time	Others (fSCLK/fTSCLK)	> 50MHz	45% x (1/fSCLK)			ns
					45% x (1/fTSCLK)			ns
				≤ 50MHz	9			ns
			Normal Read (fRSCLK)		9			ns
tCLCH(2)		Clock Rise Time (peak to peak)			0.1			ns
tCHCL(2)		Clock Fall Time (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			4			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			4			ns
tDVCH	tDSU	Data In Setup Time			2			ns
tCHDX	tDH	Data In Hold Time			3			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			4			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			4			ns
tSHSL	tCSH	CS# Deselect Time	From Read to next Read		15			ns
			From Write/Erase/Program to Read Status Register		50			ns
tSHQZ(2)	tDIS	Output Disable Time	2.65V-3.6V				10	ns
			3.0V-3.6V				8	ns
tHLCH		HOLD# Setup Time (relative to SCLK)			5			ns
tCHHH		HOLD# Hold Time (relative to SCLK)			5			ns
tHHCH		HOLD Setup Time (relative to SCLK)			5			ns
tCHHL		HOLD Hold Time (relative to SCLK)			5			ns
tHHQX	tLZ	HOLD to Output Low-Z Loading=30pF	2.65V-3.6V				10	ns
			3.0V-3.6V				8	ns
tHLQZ	tHZ	HOLD# to Output High-Z Loading=30pF	2.65V-3.6V				10	ns
			3.0V-3.6V				8	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.65V-3.6V	Loading: 15pF				6	ns
			Loading: 30pF				8	ns
tCLQX	tHO	Output Hold Time			1			ns
tWHSL(3)		Write Protect Setup Time			20			ns
tSHWL(3)		Write Protect Hold Time			100			ns
tESL(4)		Erase Suspend Latency					20	us
tPSL(4)		Program Suspend Latency					20	us
tPRS(5)		Latency between Program Resume and next Suspend			0.3	100		us
tERS(6)		Latency between Erase Resume and next Suspend			0.3	200		us

Symbol	Alt.	Parameters	Min.	Typ.	Max.(7)		Unit
					105°C	125°C	
tRCR		Recovery Time from Read	20				us
tRCP		Recovery Time from Program	20				us
tRCE		Recovery Time from Erase	12				ms
tDP		CS# High to Deep Power-down Mode			10		us
tRES1		CS# High to Standby Mode without Electronic Signature Read			100		us
tRES2		CS# High to Standby Mode with Electronic Signature Read			100		us
tW		Write Status Register Cycle Time			40		ms
tBP		Byte-Program		10	60	70	us
tPP		Page Program Cycle Time		0.33	1.6	2.0	ms
tSE		Sector Erase Cycle Time (4KB)		25	240	260	ms
tBE32K		Block Erase Cycle Time (32KB)		0.14	0.7	0.8	s
tBE		Block Erase Cycle Time (64KB)		0.25	1.1	1.2	s
tCE		Chip Erase Cycle Time		20	65	70	s
tWSR		Write Security Register Time			1		ms
Erase/Program cycles			100,000				cycles

Notes:

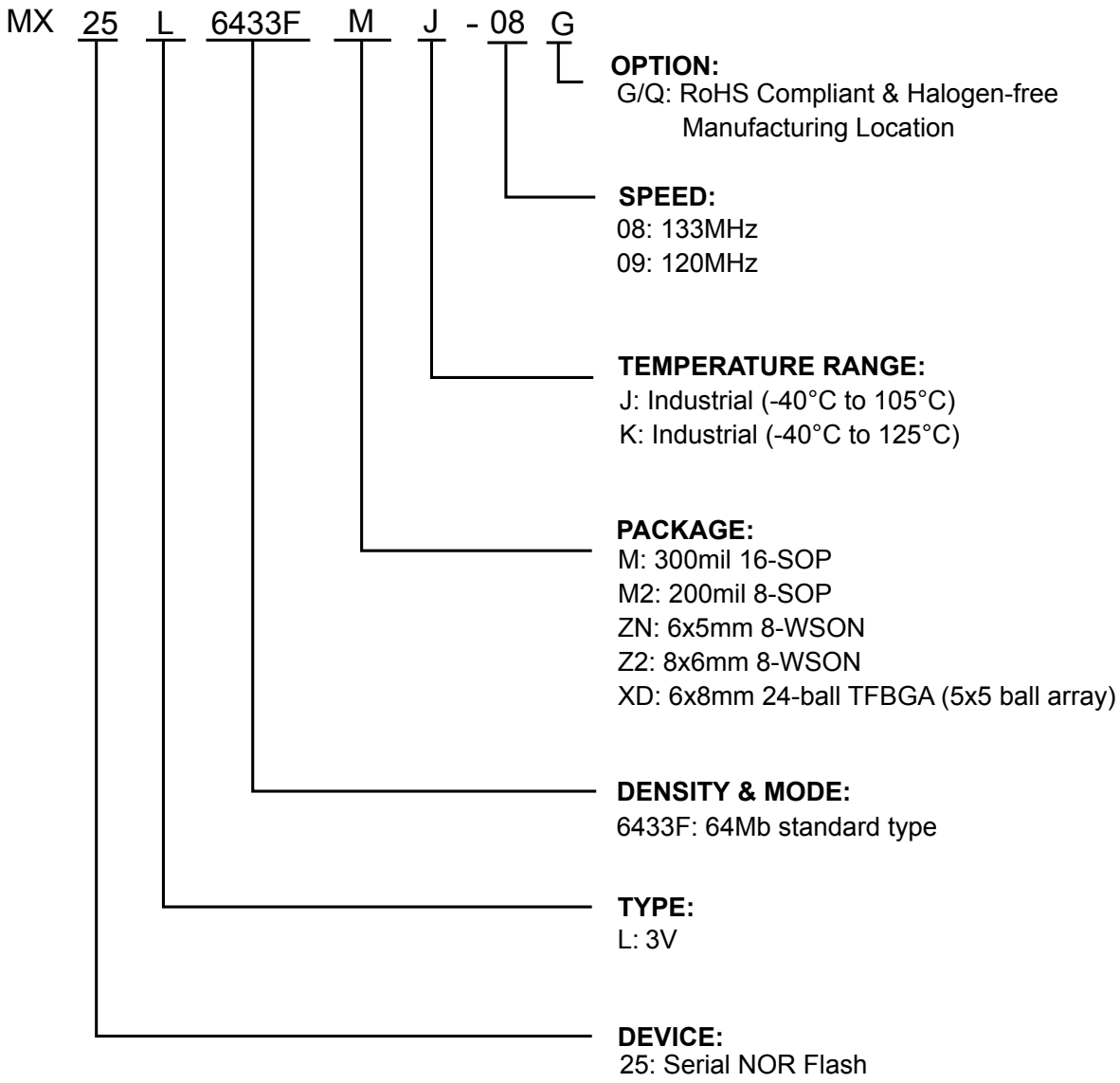
1. tCH + tCL must be greater than or equal to 1/ fC.
2. The value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.
4. Latency time is required to complete Erase/Program Suspend operation until WIP bit is "0".
5. For tPRS, minimum timing must be observed before issuing the next program suspend command. However, a period equal to or longer than the typical timing is required in order for the program operation to make progress.
6. For tERS, minimum timing must be observed before issuing the next erase suspend command. However, a period equal to or longer than the typical timing is required in order for the erase operation to make progress.
7. Under worst conditions from -40°C to 105°C/125°C and 2.65V.

7. ORDERING INFORMATION

Please contact Macronix regional sales for the latest product selection and available form factors.

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25L6433FMJ-08G	133	-40°C to 105°C	300mil 16-SOP	
MX25L6433FM2J-08G	133	-40°C to 105°C	200mil 8-SOP	
MX25L6433FM2J-08Q	133	-40°C to 105°C	200mil 8-SOP	
MX25L6433FXDJ-08Q	133	-40°C to 105°C	24-ball TFBGA	5x5 ball array
MX25L6433FZNJ-08Q	133	-40°C to 105°C	8-WSON (6x5mm)	

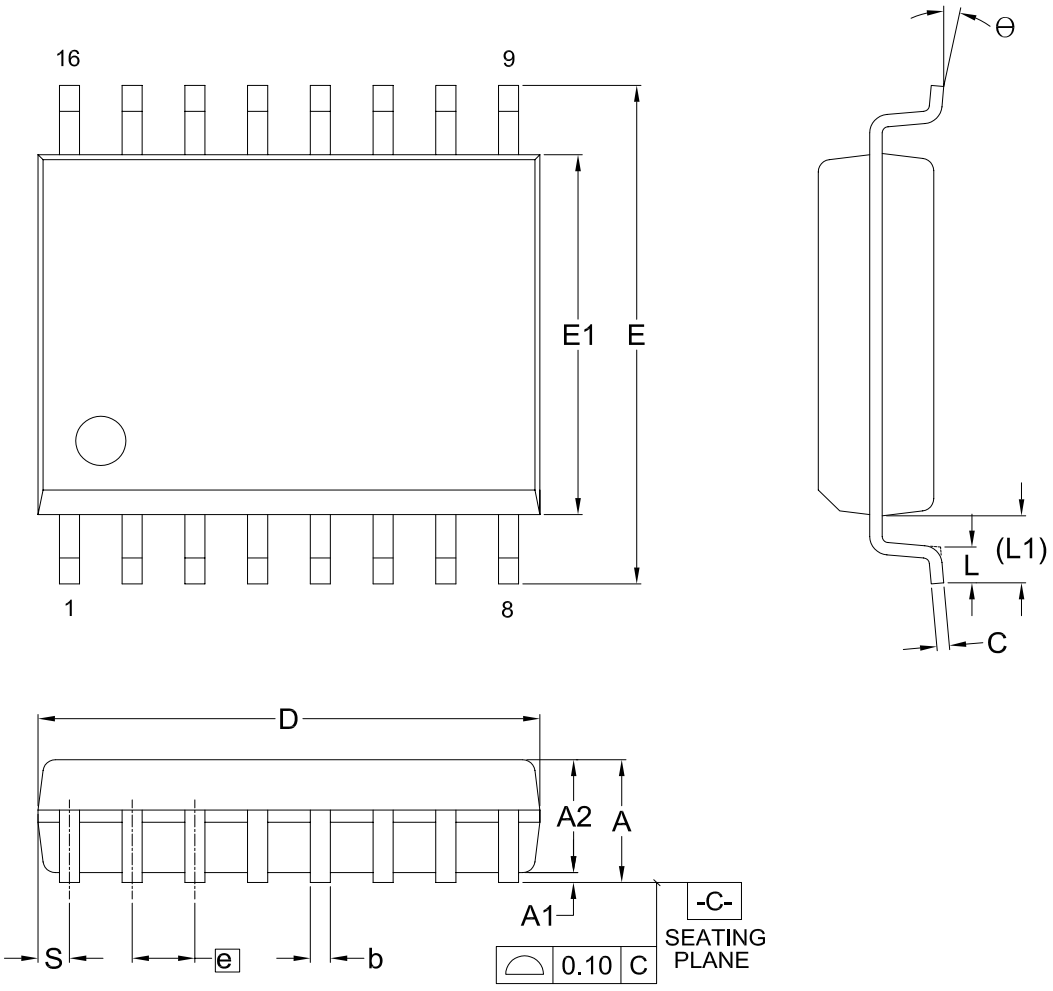
8. PART NAME DESCRIPTION



9. PACKAGE INFORMATION

9-1. 16-SOP (300mil)

Doc. Title: Package Outline for SOP 16L (300MIL)

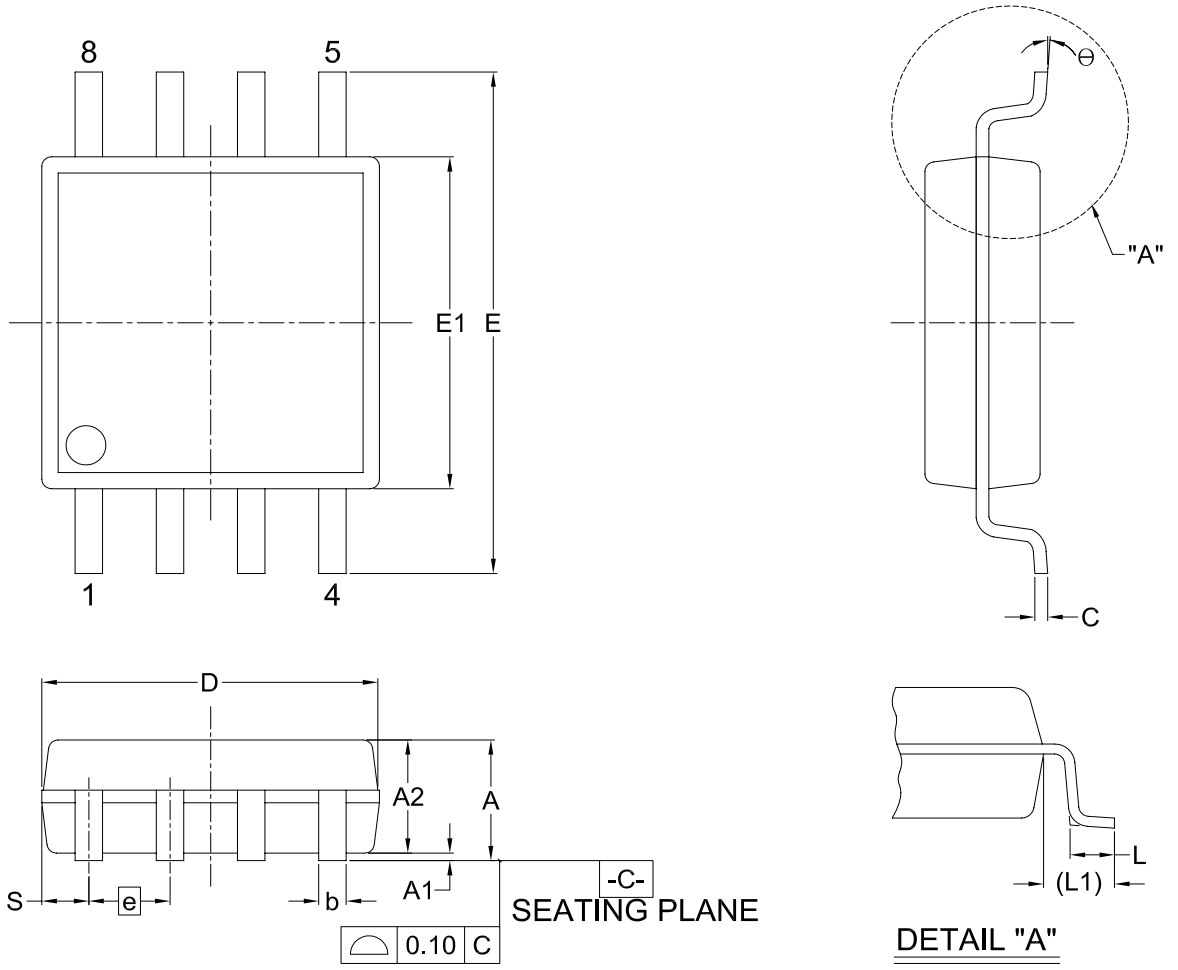


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.25	0.31	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0°
	Nom.	---	0.20	2.35	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5°
	Max.	2.65	0.30	2.45	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8°
Inch	Min.	---	0.004	0.089	0.012	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0°
	Nom.	---	0.008	0.093	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5°
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8°

9-2. 8-SOP (200mil)

Doc. Title: Package Outline for SOP 8L 200MIL

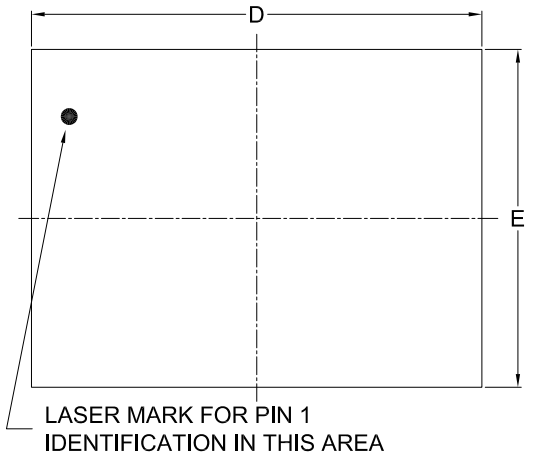


Dimensions (inch dimensions are derived from the original mm dimensions)

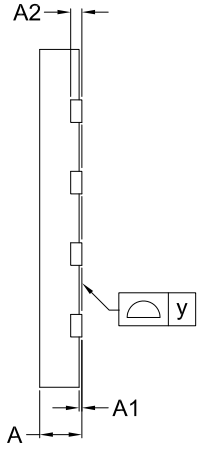
SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	1.75	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0°
	Nom.	1.95	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5°
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8°
Inch	Min.	0.069	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0°
	Nom.	0.077	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5°
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8°

9-3. 8-WSON (8x6mm)

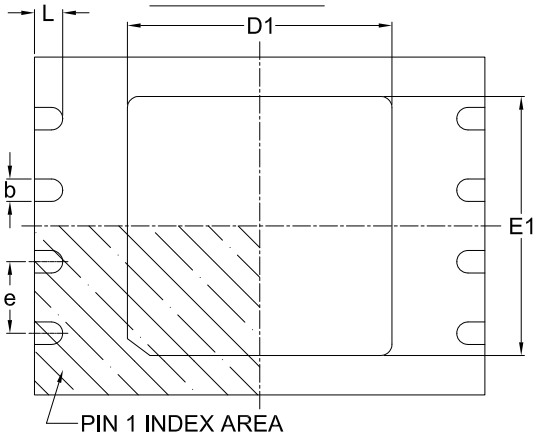
Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM)



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note:

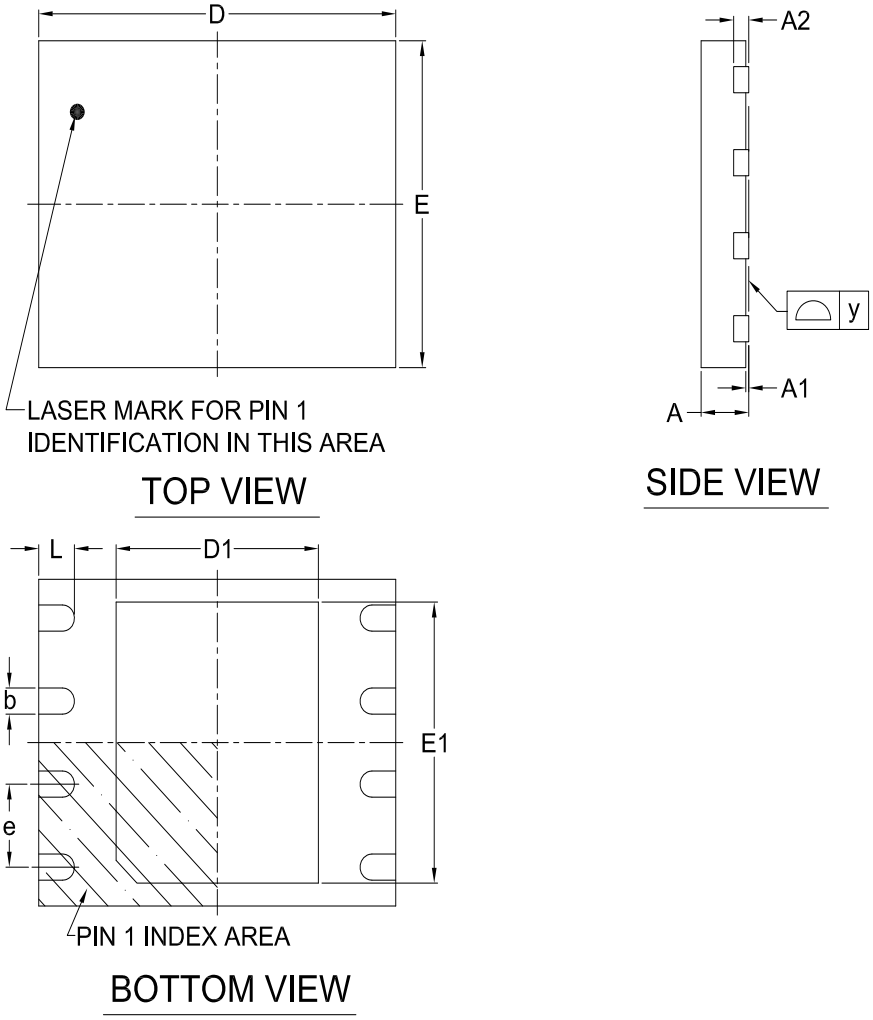
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	4.65	5.90	4.55	0.45	---	0.00
	Nom.	---	---	0.20	0.40	8.00	4.70	6.00	4.60	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	4.75	6.10	4.65	0.55	---	0.05
Inch	Min.	0.028	---	---	0.014	0.311	0.183	0.232	0.179	0.018	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.185	0.236	0.181	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.187	0.240	0.183	0.022	---	0.002

9-4. 8-WSON (6x5mm)

Doc. Title: Package Outline for WSON 8L (6x5x0.8MM, LEAD PITCH 1.27MM)



Note:

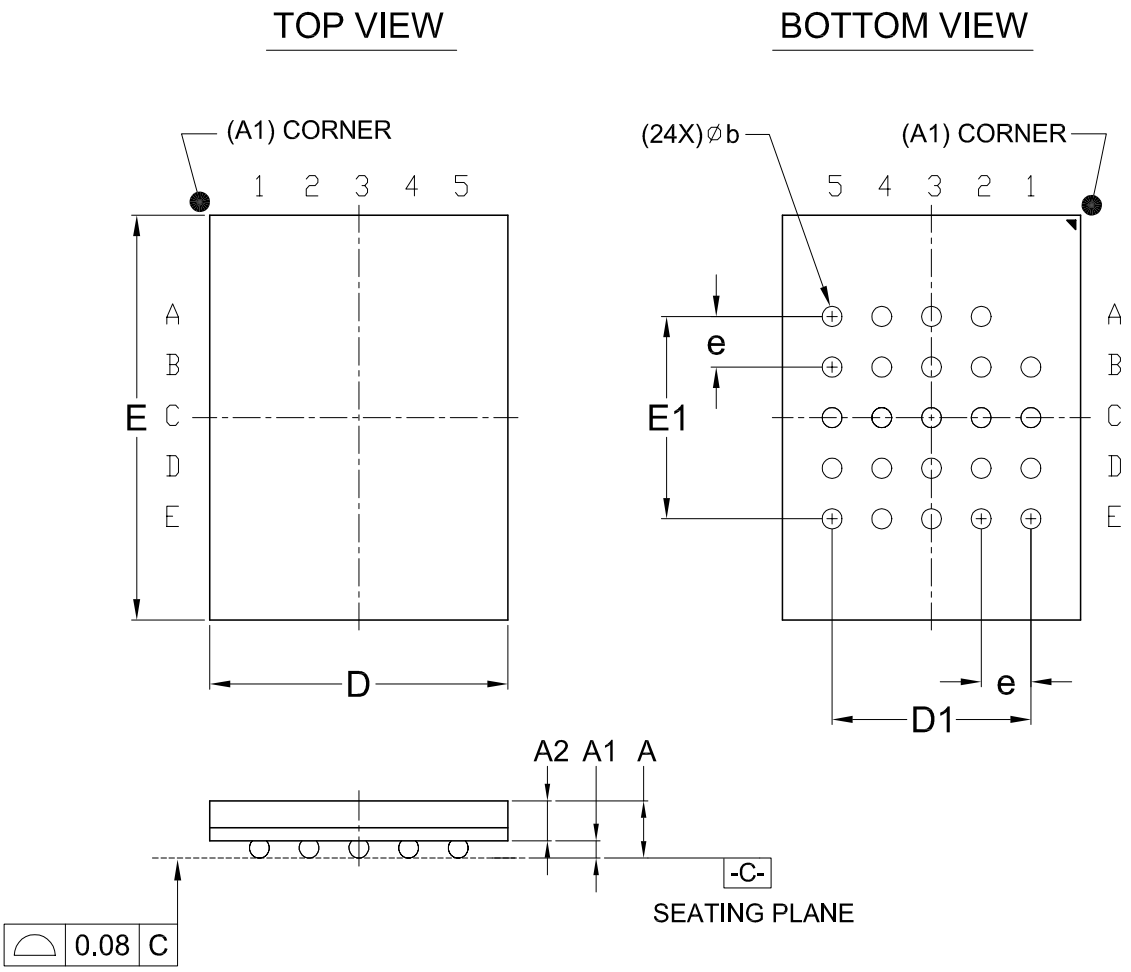
This package has an exposed metal pad underneath the package. It is recommended to leave the metal pad floating or to connect it to the same ground as the GND pin of the package. Do not connect the metal pad to any other voltage or signal line on the PCB. Avoid placing vias or traces underneath the metal pad. Connection of this metal pad to any other voltage or signal line can result in shorts and/or electrical malfunction of the device.

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	5.90	3.35	4.90	3.95	0.55	---	0.00
	Nom.	---	---	0.20	0.40	6.00	3.40	5.00	4.00	0.60	1.27	---
	Max.	0.80	0.05	---	0.48	6.10	3.45	5.10	4.05	0.65	---	0.05
Inch	Min.	0.028	---	---	0.014	0.232	0.132	0.193	0.156	0.022	---	0.00
	Nom.	---	---	0.008	0.016	0.236	0.134	0.197	0.157	0.024	0.05	---
	Max.	0.032	0.002	---	0.019	0.240	0.136	0.201	0.159	0.026	---	0.002

9-5. 24-Ball TFBGA (5x5 Ball Array)

Doc. Title: Package Outline for CSP 24BALL (6x8x1.2MM, BALL PITCH 1.0MM, BALL DIAMETER 0.4MM, 5x5 BALL ARRAY)



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	D	D1	E	E1	e
mm	Min.	---	0.25	0.65	0.35	5.90	---	7.90	---	---
	Nom.	---	0.30	---	0.40	6.00	4.00	8.00	4.00	1.00
	Max.	1.20	0.35	---	0.45	6.10	---	8.10	---	---
Inch	Min.	---	0.010	0.026	0.014	0.232	---	0.311	---	---
	Nom.	---	0.012	---	0.016	0.236	0.157	0.315	0.157	0.039
	Max.	0.047	0.014	---	0.018	0.240	---	0.319	---	---

10. REVISION HISTORY

Revision	Descriptions	Page
April 01, 2016		
1.0	1. Initial Release.	All
July 30, 2019		
1.1	1. Added "Macronix Proprietary" footnote.	All
	2. Added 08Q part names of 8-SOP.	P10-11
	3. Updated the note for the internal pull up status of HOLD#/SIO3 and WP#/SIO2.	P5
	4. Format modification.	P12-15
	5. Updated *"9-3. 8-WSON (8x6mm)"* in Max. "y" values and Min./Max. D1, E1 and L values.	P14
	6. Updated *"9-4. 8-WSON (6x5mm)"* in Min./Max. D1, E1 and L values.	P15
May 23, 2022		
1.2	1. Revised Doc. Title of package outline.	P13
	2. Added part name: MX25L6433FXDJ-08Q.	P3, 5, 10-11, 16
	3. Added "Support Performance Enhance Mode - XIP (execute-in-place)".	P3
	4. Corrected tCH / tCL descriptions.	P8
December 14, 2022		
1.3	1. Added part name: MX25L6433FZNJ-08Q.	P10

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