MX25L6436E

HIGH PERFORMANCE
SERIAL FLASH SPECIFICATION

Contents

64M-BIT [x 1/x 2/x 4] CMOS MXSMIO™ (SERIAL MULTI I/O) FLASH MEMORY

FEATURES

GENERAL

- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 64Mb: 67,108,864 x 1 bit structure or 33,554,432 x 2 bits (two I/O mode) structure or 16,777,216 x 4 bits (four I/O mode) structure
- 2048 Equal Sectors with 4K bytes each
  - Any Sector can be erased individually
- 256 Equal Blocks with 32K bytes each
  - Any Block can be erased individually
- 128 Equal Blocks with 64K bytes each
  - Any Block can be erased individually
- Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Latch-up protected to 100mA from -1V to Vcc +1V

PERFORMANCE

- High Performance
  VCC = 2.7~3.6V
  - Normal read
    - 50MHz
  - Fast read (Normal Serial Mode)
    - 1 I/O: 104MHz with 8 dummy cycles
    - 2 I/O: 70MHz with 8 dummy cycles
    - 4 I/O: 75MHz with 8 dummy cycles
  - Fast program time: 1.4ms(typ.) and 5ms(max.)/page (256-byte per page)
  - Byte program time: 9us (typical)
  - Continuously Program mode (automatically increase address under word program mode)
  - Fast erase time: 60ms (typ.)/sector (4K-byte per sector) ; 0.7s(typ.) /block (64K-byte per block); 50s(typ.) /chip
- Low Power Consumption
  - Low active read current: 19mA(max.) at 104MHz, 15mA(max.) at 66MHz and 10mA(max.) at 33MHz
  - Low active programming current: 25mA (max.)
  - Low active erase current: 25mA (max.)
  - Low standby current: 50uA (max.)
  - Deep power down current: 20uA (max.)
- Typical 100,000 erase/program cycles
- 20 years data retention

SOFTWARE FEATURES

- Input Data Format
  - 1-byte Command code
- Advanced Security Features
  - BP0-BP3 block group protect
  - Flexible individual block protect when OTP WPSEL=1
  - Additional 4K bits secured OTP for unique identifier

- Auto Erase and Auto Program Algorithms
  - Automatically erases and verifies data at selected sector
  - Automatically programs and verifies data at selected page by an internal algorithm that automatically times the program pulse width (Any page to be programed should have page in the erased state first.)
- Status Register Feature
- Electronic Identification
  - JEDEC 1-byte Manufacturer ID and 2-byte Device ID
  - RES command for 1-byte Device ID
  - REMS, REMS2 and REMS4 commands for 1-byte Manufacturer ID and 1-byte Device ID
- Support Serial Flash Discoverable Parameters (SFDP) mode

HARDWARE FEATURES

- SCLK Input
  - Serial clock input
- SI/SIO0
  - Serial Data Input or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- SO/SIO1
  - Serial Data Output or Serial Data Input/Output for 2 x I/O mode and 4 x I/O mode
- WP#/SIO2
  - Hardware write protection or serial data Input/Output for 4 x I/O mode
- NC/SIO3
  - NC pin or serial data Input/Output for 4 x I/O mode
- PACKAGE
  - 16-pin SOP (300mil)
  - 8-WSON (8x6mm)
  - 8-pin SOP (200mil)
  - **All devices are RoHS Compliant**

GENERAL DESCRIPTION

MX25L6436E is 67,108,864 bits serial Flash memory, which is configured as 8,388,608 x 8 internally. When it is in two or four I/O mode, the structure becomes 33,554,432 bits x 2 or 16,777,216 bits x 4. The MX25L6436E features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input.

MX25L6436E provides high performance read mode, which may latch address and data on both rising and falling edge of clock. By using this high performance read mode, the data throughput may be doubling. Moreover, the performance may reach direct code execution, the RAM size of the system may be reduced and further saving system cost.

MX25L6436E, MXSMIO^{TM} (Serial Multi I/O) flash memory, provides sequential read operation on the whole chip and multi-I/O features.

When it is in dual I/O mode, the SI pin and SO pin become SIO0 pin and SIO1 pin for address/dummy bits input and data output. When it is in quad I/O mode, the SI pin, SO pin, WP# pin and NC pin become SIO0 pin, SIO1 pin, SIO2 pin and SIO3 pin for address/dummy bits input and data Input/Output.

After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page (256 bytes) basis, or word basis. Continuously Program mode and erase command are executed on 4K-byte sector, 32K-byte/64K-byte block, or whole chip basis.

To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via the WIP bit.

When the device is not in operation and CS# is high, it is put in standby mode and draws less than 100uA DC current.

The MX25L6436E utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after 100,000 program and erase cycles.

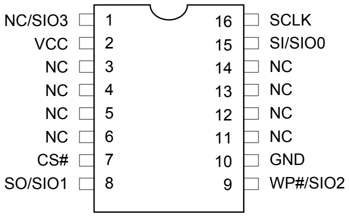
Table 1. Additional Features

Additional Features / Part Name	Protection and Security		Read Performance		
	Flexible or Individual block (or sector) protection	4K-bit secured OTP	1 I/O Read (104 MHz)	2 I/O Read (70 MHz)	4 I/O Read (75 MHz)
MX25L6436E	V	V	V	V	V

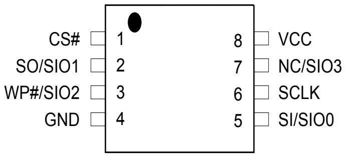
Additional Features / Part Name	Identifier				
	RES (command: AB hex)	REMS (command: 90 hex)	REMS2 (command: EF hex)	REMS4 (command: DF hex)	RDID (command: 9F hex)
MX25L6436E	16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 16 (hex)	C2 20 17 (hex)

PIN CONFIGURATION

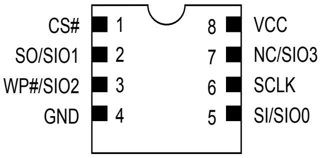
16-PIN SOP (300mil) *



8-PIN SOP (200mil)



8-WSON (8x6mm) *

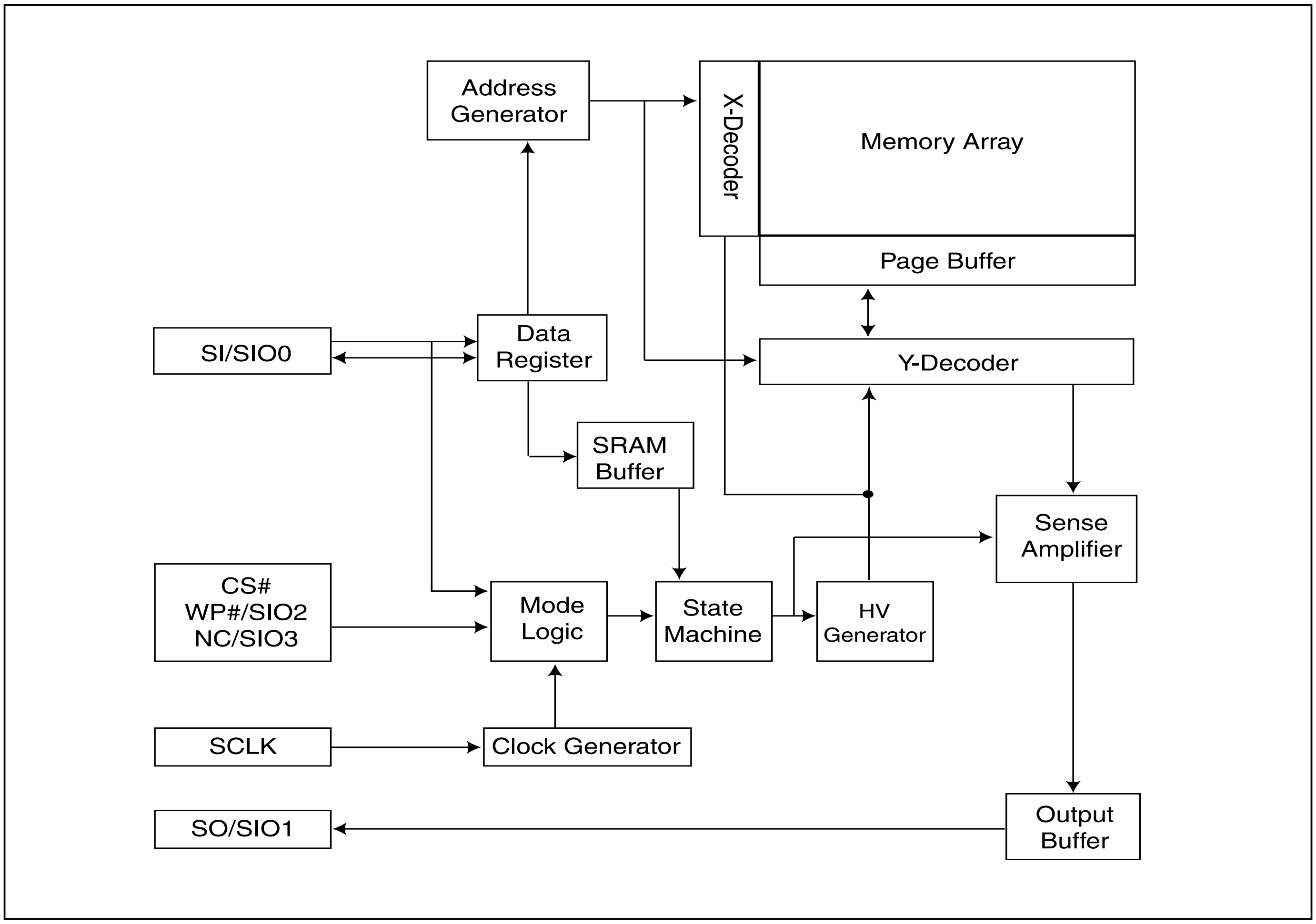


* Advanced Information

PIN DESCRIPTION

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1xI/O)/ Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SO/SIO1	Serial Data Output (for 1xI/O)/Serial Data Input & Output (for 2xI/O or 4xI/O mode)
SCLK	Clock Input
WP#/SIO2	Write protection: connect to GND or Serial Data Input & Output (for 4xI/O mode)
NC/SIO3	NC pin (Not connect) or Serial Data Input & Output (for 4xI/O mode)
VCC	+ 3.3V Power Supply
GND	Ground
NC	No Connection

BLOCK DIAGRAM



DATA PROTECTION

During power transition, there may be some false system level signals which result in inadvertent erasure or programming. The device is designed to protect itself from these accidental write cycles.

The state machine will be reset as standby mode automatically during power up. In addition, the control register architecture of the device constrains that the memory contents can only be changed after specific command sequences have completed successfully.

In the following, there are several features to protect the system from the accidental write cycles during VCC power-up and power-down or from system noise.

- Valid command length checking: The command length will be checked whether it is at byte base and completed on byte boundary.

- Write Enable (WREN) command: WREN command is required to set the Write Enable Latch bit (WEL) before issuing other commands to change data. The WEL bit will return to reset stage under following situations:
  - Power-up
  - Write Disable (WRDI) command completion
  - Write Status Register (WRSR) command completion
  - Page Program (PP, 4PP) command completion
  - Continuously Program mode (CP) instruction completion
  - Sector Erase (SE) command completion
  - Block Erase (BE, BE32K) command completion
  - Chip Erase (CE) command completion
  - Single Block Lock/Unlock (SBLK/SBULK) instruction completion
  - Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

- Deep Power Down Mode: By entering deep power down mode, the flash device also is under protected from writing all commands except Release from Deep Power Down mode command (RDP) and Read Electronic Signature command (RES).

I. Block lock protection

- The Software Protected Mode (SPM) uses (BP3, BP2, BP1, BP0) bits to allow part of memory to be protected as read only. The protected area definition is shown as table of "*Protected Area Sizes*", the protected areas are more flexible which may protect various area by setting value of BP0-BP3 bits. Please refer to table of "*Protected Area Sizes*".

- The Hardware Protected Mode (HPM) uses WP#/SIO2 to protect the (BP3, BP2, BP1, BP0) bits and SRWD bit. If the system goes into four I/O mode, the feature of HPM will be disabled.

- MX25L6436E provides individual block (or sector) write protect & unprotect. User may enter the mode with WPSEL command and conduct individual block (or sector) write protect with SBLK instruction, or SBULK for individual block (or sector) unprotect. Under the mode, user may conduct whole chip (all blocks) protect with GBLK instruction and unlock the whole chip with GBULK instruction.

Table 2. Protected Area Sizes

Status bit				Protection Area
BP3	**BP2**	**BP1**	**BP0**	**64Mb**
0	0	0	0	0 (none)
0	0	0	1	1 (2 blocks, block 126th-127th)
0	0	1	0	2 (4 blocks, block 124th-127th)
0	0	1	1	3 (8 blocks, block 120th-127th)
0	1	0	0	4 (16 blocks, block 112nd-127th)
0	1	0	1	5 (32 blocks, block 96th-127th)
0	1	1	0	6 (64 blocks, block 64th-127th)
0	1	1	1	7 (128 blocks, all)
1	0	0	0	8 (128 blocks, all)
1	0	0	1	9 (128 blocks, all)
1	0	1	0	10 (128 blocks, all)
1	0	1	1	11 (128 blocks, all)
1	1	0	0	12 (128 blocks, all)
1	1	0	1	13 (128 blocks, all)
1	1	1	0	14 (128 blocks, all)
1	1	1	1	15 (128 blocks, all)

Note: The device is ready to accept a Chip Erase instruction if, and only if, all Block Protect (BP3, BP2, BP1, BP0) are 0.

II. Additional 4K-bit secured OTP for unique identifier: to provide 4K-bit One-Time Program area for setting device unique serial number - Which may be set by factory or system maker. Please refer to *Table 3. 4K-bit Secured OTP Definition*.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command), and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command.
- Customer may lock-down the customer lockable secured OTP by writing WRSCUR(write security register) command to set customer lock-down bit1 as "1". Please refer to table of "*Security Register Definition*" for security register bit definition and table of "*4K-bit Secured OTP Definition*" for address range definition.
- **Note:** Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit Secured OTP mode, array access is not allowed.

Table 3. 4K-bit Secured OTP Definition

Address range	Size	Standard Factory Lock	Customer Lock
xxx000~xxx00F	128-bit	ESN (electrical serial number)	Determined by customer
xxx010~xxx1FF	3968-bit	N/A	

Memory Organization

Table 4. Memory Organization

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
127	255	2047	7FF000h	7FFFFFh
		⋮		
		2040	7F8000h	7F8FFFh
	254	2039	7F7000h	7F7FFFh
		⋮		
		2032	7F0000h	7F0FFFh
126	253	2031	7EF000h	7EFFFFh
		⋮		
		2024	7E8000h	7E8FFFh
	252	2023	7E7000h	7E7FFFh
		⋮		
		2016	7E0000h	7E0FFFh
125	251	2015	7DF000h	7DFFFFh
		⋮		
		2008	7D8000h	7D8FFFh
	250	2007	7D7000h	7D7FFFh
		⋮		
		2000	7D0000h	7D0FFFh

individual 16 sectors
lock/unlock unit:4K-byte

individual block
lock/unlock unit:64K-byte

individual block
lock/unlock unit:64K-byte

Block(64K-byte)	Block(32K-byte)	Sector (4K-byte)	Address Range	
2	5	47	02F000h	02FFFFh
		⋮		
		40	028000h	028FFFh
	4	39	027000h	027FFFh
		⋮		
		32	020000h	020FFFh
1	3	31	01F000h	01FFFFh
		⋮		
		24	018000h	018FFFh
	2	23	017000h	017FFFh
		⋮		
		16	010000h	010FFFh
0	1	15	00F000h	00FFFFh
		⋮		
		8	008000h	008FFFh
	0	7	007000h	007FFFh
		⋮		
		0	000000h	000FFFh

individual block
lock/unlock unit:64K-byte

individual 16 sectors
lock/unlock unit:4K-byte

DEVICE OPERATION

1. Before a command is issued, status register should be checked to ensure device is ready for the intended operation.

2. When incorrect command is inputted to this device, it enters standby mode and remains in standby mode until next CS# falling edge. In standby mode, SO pin of the device is High-Z.

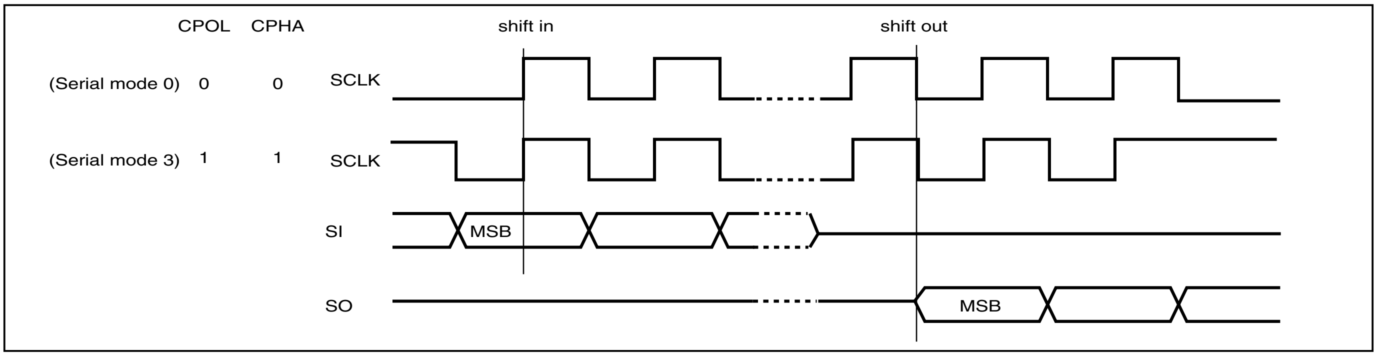
3. When correct command is inputted to this device, it enters active mode and remains in active mode until next CS# rising edge.

4. For standard single data rate serial mode, input data is latched on the rising edge of Serial Clock (SCLK) and data is shifted out on the falling edge of SCLK. The difference of Serial mode 0 and mode 3 is shown as *Figure 1*.

5. For the following instructions: RDID, RDSR, RDSCUR, READ, FAST_READ, RDSFDP, DREAD, QREAD, RDBLOCK, RES, REMS, REMS2, and REMS4 the shifted-in instruction sequence is followed by a data-out sequence. After any bit of data being shifted out, the CS# can be high. For the following instructions: WREN, WRDI, WRSR, SE, BE, BE32K, CE, PP, CP, 4PP, RDP, DP, WPSEL, SBLK, SBULK, GBLK, GBULK, ENSO, EXSO, WRSCUR, ESRY, DSRY and CLSR the CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

6. While a Write Status Register, Program or Erase operation is in progress, access to the memory array is neglected and will not affect the current operation of Write Status Register, Program, Erase.

Figure 1. Serial Modes Supported (for Normal Serial mode)



Note:
CPOL indicates clock polarity of Serial master, CPOL=1 for SCLK high while idle, CPOL=0 for SCLK low while not transmitting. CPHA indicates clock phase. The combination of CPOL bit and CPHA bit decides which Serial mode is supported.

COMMAND DESCRIPTION

Table 5. Command Sets

COMMAND (byte)	WREN (write enable)	WRDI (write disable)	RDID (read identification)	RDSR (read status register)	WRSR (write status register)	READ (read data)	FAST READ (fast read data)
Command (hex)	06	04	9F	05	01	03	0B
Input Cycles					Data(8)	ADD(24)	ADD(24)
Dummy Cycles							8
Action	sets the (WEL) write enable latch bit	resets the (WEL) write enable latch bit	outputs JEDEC ID: 1-byte Manufacturer ID & 2-byte Device ID	to read out the values of the status register	to write new values to the status register	n bytes read out until CS# goes high	n bytes read out until CS# goes high

COMMAND (byte)	RDSFDP (Read SFDP)	DREAD (1I 2O read)	QREAD (1I 4O read)	4PP (quad page program)	SE (sector erase)	BE (block erase 64KB)	BE 32K (block erase 32KB)
Command (hex)	5A	3B	6B	38	20	D8	52
Input Cycles	ADD(24)	ADD(24)	ADD(24)	ADD(6)+ Data(512)	ADD(24)	ADD(24)	ADD(24)
Dummy Cycles	8	8	8				
Action	Read SFDP mode	n bytes read out by Dual output until CS# goes high	n bytes read out by Quad output until CS# goes high	quad input to program the selected page	to erase the selected sector	to erase the selected 64KB block	to erase the selected 32KB block

COMMAND (byte)	CE (chip erase)	PP (Page program)	CP (Continuously program mode)	DP (Deep power down)	RDP (Release from deep power down)	RES (read electronic ID)	REMS (read electronic manufacturer & device ID)
Command (hex)	60 or C7	02	AD	B9	AB	AB	90
Input Cycles		ADD(24)+ Data(2048)	ADD(24)+ Data(16)				ADD(24)
Dummy Cycles						24	
Action	to erase whole chip	to program the selected page	continously program whole chip, the address is automatically increase	enters deep power down mode	release from deep power down mode	to read out 1-byte Device ID	output the Manufacturer ID & Device ID

COMMAND (byte)	REMS2 (read ID for 2x I/O mode)	REMS4 (read ID for 4x I/O mode)	ENSO (enter secured OTP)	EXSO (exit secured OTP)	RDSCUR (read security register)	WRSCUR (write security register)	ESRY (enable SO to output RY/BY#)	DSRY (disable SO to output RY/BY#)
Command (hex)	EF	DF	B1	C1	2B	2F	70	80
Input Cycles	ADD(24)	ADD(24)						
Dummy Cycles								
Action	output the Manufacturer ID & Device ID	output the Manufact-urer ID & device ID	to enter the 4K-bit Secured OTP mode	to exit the 4K-bit Secured OTP mode	to read value of security register	to set the lock-down bit as "1" (once lock-down, cannot be updated)	to enable SO to output RY/BY# during CP mode	to disable SO to output RY/BY# during CP mode

COMMAND (byte)	CLSR (Clear SR Fail Flags)	WPSEL (write protection selection)	SBLK (single block lock) *Note 2	SBULK (single block unlock)	RDBLOCK (block protect read)	GBLK (gang block lock)	GBULK (gang block unlock)
Command (hex)	30	68	36	39	3C	7E	98
Input Cycles			ADD(24)	ADD(24)	ADD(24)		
Dummy Cycles							
Action	clear security register bit 6 and bit 5	to enter and enable individal block protect mode	individual block (64K-byte) or sector (4K-byte) write protect	individual block (64K-byte) or sector (4K-byte) unprotect	read individual block or sector write protect status	whole chip write protect	whole chip unprotect

Notes:
1. It is not recommended to adopt any other code not in the command definition table, which will potentially enter the hidden mode.
2: In individual block write protection mode, all blocks/sectors are locked as defualt.

(1) Write Enable (WREN)

The Write Enable (WREN) instruction is for setting Write Enable Latch (WEL) bit. For those instructions like PP, 4PP, CP, SE, BE, BE32K, CE, WRSR, SBLK, SBULK, GBLK and GBULK, which are intended to change the device content, should be set every time after the WREN instruction setting the WEL bit.

The sequence of issuing WREN instruction is: CS# goes low→ sending WREN instruction code→ CS# goes high. (Please refer to *Figure 10*)

(2) Write Disable (WRDI)

The Write Disable (WRDI) instruction is for resetting Write Enable Latch (WEL) bit.

The sequence of issuing WRDI instruction is: CS# goes low→ sending WRDI instruction code→ CS# goes high. (Please refer to *Figure 11*)

The WEL bit is reset by following situations:
- Power-up
- Write Disable (WRDI) instruction completion
- Write Status Register (WRSR) instruction completion
- Page Program (PP, 4PP) instruction completion
- Sector Erase (SE) instruction completion
- Block Erase (BE, BE32K) instruction completion
- Chip Erase (CE) instruction completion
- Continuously Program mode (CP) instruction completion
- Single Block Lock/Unlock (SBLK/SBULK) instruction completion
- Gang Block Lock/Unlock (GBLK/GBULK) instruction completion

(3) Read Identification (RDID)

The RDID instruction is for reading the Manufacturer ID of 1-byte and followed by Device ID of 2-byte. The MXIC Manufacturer ID is C2(hex), the memory type ID is 20(hex) as the first-byte Device ID, and the individual Device ID of second-byte ID are listed as table of "*ID Definitions*". (Please refer to *Table 6*)

The sequence of issuing RDID instruction is: CS# goes low→ sending RDID instruction code → 24-bits ID data out on SO→ to end RDID operation can use CS# to high at any time during data out. (Please refer to *Figure 12*)

While Program/Erase operation is in progress, it will not decode the RDID instruction, so there's no effect on the cycle of program/erase operation which is currently in progress. When CS# goes high, the device is at standby stage.

(4) Read Status Register (RDSR)

The RDSR instruction is for reading Status Register. The Read Status Register can be read at any time (even in program/erase/write status register condition) and continuously. It is recommended to check the Write in Progress (WIP) bit before sending a new instruction when a program, erase, or write status register operation is in progress.

The sequence of issuing RDSR instruction is: CS# goes low→ sending RDSR instruction code→ Status Register data out on SO (Please refer to *Figure 13*).

The definition of the status register bits is as below:

WIP bit. The Write in Progress (WIP) bit, a volatile bit, indicates whether the device is busy in program/erase/write status register progress. When WIP bit sets to 1, which means the device is busy in program/erase/write status register progress. When WIP bit sets to 0, which means the device is not in progress of program/erase/write status register cycle.

WEL bit. The Write Enable Latch (WEL) bit, a volatile bit, indicates whether the device is set to internal write enable latch. When WEL bit sets to "1", which means the internal write enable latch is set, the device can accept program/erase/write status register instruction. When WEL bit sets to 0, which means no internal write enable latch; the device will not accept program/erase/write status register instruction. The program/erase command will be ignored and will reset WEL bit if it is applied to a protected memory area.

BP3, BP2, BP1, BP0 bits. The Block Protect (BP3, BP2, BP1, BP0) bits, non-volatile bits, indicate the protected area (as defined in Table 2) of the device to against the program/erase instruction without hardware protection mode being set. To write the Block Protect (BP3, BP2, BP1, BP0) bits requires the Write Status Register (WRSR) instruction to be executed. Those bits define the protected area of the memory to against Page Program (PP), Sector Erase (SE), Block Erase (BE) and Chip Erase (CE) instructions (only if all Block Protect bits set to 0, the CE instruction can be executed).

QE bit. The Quad Enable (QE) bit, non-volatile bit, while it is "0" (factory default), it performs non-Quad and WP# is enable. While QE is "1", it performs Quad I/O mode and WP# is disabled. In the other word, if the system goes into four I/O mode (QE=1), the feature of HPM will be disabled.

SRWD bit. The Status Register Write Disable (SRWD) bit, non-volatile bit, default value is "0". SRWD bit is operated together with Write Protection (WP#/SIO2) pin for providing hardware protection mode. The hardware protection mode requires SRWD sets to 1 and WP#/SIO2 pin signal is low stage. In the hardware protection mode, the Write Status Register (WRSR) instruction is no longer accepted for execution and the SRWD bit and Block Protect bits (BP3, BP2, BP1, BP0) are read only.

Status Register

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
SRWD (status register write protect)	QE (Quad Enable)	BP3 (level of protected block)	BP2 (level of protected block)	BP1 (level of protected block)	BP0 (level of protected block)	WEL (write enable latch)	WIP (write in progress bit)
1=status register write disable	1= Quad Enable 0=not Quad Enable	(note 1)	(note 1)	(note 1)	(note 1)	1=write enable 0=not write enable	1=write operation 0=not in write operation
Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	Non-volatile bit	volatile bit	volatile bit

Note: see the *"Table 2. Protected Area Sizes"*.

(5) Write Status Register (WRSR)

The WRSR instruction is for changing the values of Status Register Bits. Before sending WRSR instruction, the Write Enable (WREN) instruction must be decoded and executed to set the Write Enable Latch (WEL) bit in advance. The WRSR instruction can change the value of Block Protect (BP3, BP2, BP1, BP0) bits to define the protected area of memory (as shown in *Table 2*). The WRSR also can set or reset the Quad enable (QE) bit and set or reset the Status Register Write Disable (SRWD) bit in accordance with Write Protection (WP#/SIO2) pin signal, but has no effect on bit1(WEL) and bit0 (WIP) of the status register. The WRSR instruction cannot be executed once the Hardware Protected Mode (HPM) is entered.

The sequence of issuing WRSR instruction is: CS# goes low→ sending WRSR instruction code→ Status Register data on SI→ CS# goes high. (Please refer to *Figure 14*)

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed. The self-timed Write Status Register cycle time (tW) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be check out during the Write Status Register cycle is in progress. The WIP sets 1 during the tW timing, and sets 0 when Write Status Register Cycle is completed, and the Write Enable Latch (WEL) bit is reset.

Protection Modes

Mode	Status register condition	WP# and SRWD bit status	Memory
Software protection mode(SPM)	Status register can be written in (WEL bit is set to "1") and the SRWD, BP0-BP3 bits can be changed	WP#=1 and SRWD bit=0, or WP#=0 and SRWD bit=0, or WP#=1 and SRWD=1	The protected area cannot be program or erase.
Hardware protection mode (HPM)	The SRWD, BP0-BP3 of status register bits cannot be changed	WP#=0, SRWD bit=1	The protected area cannot be program or erase.

Note: As defined by the values in the Block Protect (BP3, BP2, BP1, BP0) bits of the Status Register, as shown in *Table 2*.

As the table above showing, the summary of the Software Protected Mode (SPM) and Hardware Protected Mode (HPM):

Software Protected Mode (SPM):

- When SRWD bit=0, no matter WP#/SIO2 is low or high, the WREN instruction may set the WEL bit and can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM).
- When SRWD bit=1 and WP#/SIO2 is high, the WREN instruction may set the WEL bit can change the values of SRWD, BP3, BP2, BP1, BP0. The protected area, which is defined by BP3, BP2, BP1, BP0, is at software protected mode (SPM)

Hardware Protected Mode (HPM):

- When SRWD bit=1, and then WP#/SIO2 is low (or WP#/SIO2 is low before SRWD bit=1), it enters the hardware protected mode (HPM). The data of the protected area is protected by software protected mode by BP3, BP2, BP1, BP0 and hardware protected mode by the WP#/SIO2 to against data modification.

Note:
To exit the hardware protected mode requires WP#/SIO2 driving high once the hardware protected mode is entered.
If the WP#/SIO2 pin is permanently connected to high, the hardware protected mode can never be entered; only can use software protected mode via BP3, BP2, BP1, BP0.
If the system goes into four I/O mode, the feature of HPM will be disabled.

(6) Read Data Bytes (READ)

The read instruction is for reading data out. The address is latched on rising edge of SCLK, and data shifts out on the falling edge of SCLK at a maximum frequency fR. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing READ instruction is: CS# goes low→ sending READ instruction code→3-byte address on SI →data out on SO→ to end READ operation can use CS# to high at any time during data out. (Please refer to *Figure 15*)

(7) Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction is for quickly reading data out. The address is latched on rising edge of SCLK, and data of each bit shifts out on the falling edge of SCLK at a maximum frequency fC. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single FAST_READ instruction. The address counter rolls over to 0 when the highest address has been reached.

The sequence of issuing FAST_READ instruction is: CS# goes low→sending FAST_READ instruction code→3-byte address on SI→ 1-dummy byte (default) address on SI→data out on SO→ to end FAST_READ operation can use CS# to high at any time during data out. (Please refer to *Figure 16*)

While Program/Erase/Write Status Register cycle is in progress, FAST_READ instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(8) Dual Read Mode (DREAD)

The DREAD instruction enable double throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every two bits (interleave on 2 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fT. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single DREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing DREAD instruction, the following data out will perform as 2-bit instead of previous 1-bit.

The sequence of issuing DREAD instruction is: CS# goes low → sending DREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO1 & SO0 → to end DREAD operation can use CS# to high at any time during data out (Please refer to *Figure 17*).

While Program/Erase/Write Status Register cycle is in progress, DREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(9) Quad Read Mode (QREAD)

The QREAD instruction enable quad throughput of Serial Flash in read mode. The address is latched on rising edge of SCLK, and data of every four bits (interleave on 4 I/O pins) shift out on the falling edge of SCLK at a maximum frequency fQ. The first address byte can be at any location. The address is automatically increased to the next higher address after each byte data is shifted out, so the whole memory can be read out at a single QREAD instruction. The address counter rolls over to 0 when the highest address has been reached. Once writing QREAD instruction, the following data out will perform as 4-bit instead of previous 1-bit.

The sequence of issuing QREAD instruction is: CS# goes low→ sending QREAD instruction → 3-byte address on SI → 8-bit dummy cycle → data out interleave on SO3, SO2, SO1 & SO0→ to end QREAD operation can use CS# to high at any time during data out (Please refer to *Figure 18*).

While Program/Erase/Write Status Register cycle is in progress, QREAD instruction is rejected without any impact on the Program/Erase/Write Status Register current cycle.

(10) Sector Erase (SE)

The Sector Erase (SE) instruction is for erasing the data of the chosen sector to be "1". The instruction is used for any 4K-byte sector. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Sector Erase (SE). Any address of the sector (see *Table 4*) is a valid address for Sector Erase (SE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of the address been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing SE instruction is: CS# goes low → sending SE instruction code→ 3-byte address on SI →CS# goes high. (Please refer to *Figure 19*)

The self-timed Sector Erase Cycle time (tSE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Sector Erase cycle is in progress. The WIP sets during the tSE timing, and clears when Sector Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the sector is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(11) Block Erase (BE)

The Block Erase (BE) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 64K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Block Erase (BE). Any address of the block (see *Table 4*) is a valid address for Block Erase (BE) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE instruction is: CS# goes low → sending BE instruction code → 3-byte address on SI → CS# goes high. (Please refer to *Figure 20*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(12) Block Erase (BE32K)

The Block Erase (BE32) instruction is for erasing the data of the chosen block to be "1". The instruction is used for 32K-byte block erase operation. A Write Enable (WREN) instruction must be executed to set the Write Enable

Latch (WEL) bit before sending the Block Erase (BE32). Any address of the block (see *Table 4*) is a valid address for Block Erase (BE32) instruction. The CS# must go high exactly at the byte boundary (the least significant bit of address byte been latched-in); otherwise, the instruction will be rejected and not executed.

The sequence of issuing BE32 instruction is: CS# goes low → sending BE32 instruction code → 3-byte address on SI → CS# goes high. (Please refer to *Figure 20*)

The self-timed Block Erase Cycle time (tBE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Block Erase cycle is in progress. The WIP sets during the tBE timing, and clears when Block Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the block is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit still be reset.

(13) Chip Erase (CE)

The Chip Erase (CE) instruction is for erasing the data of the whole chip to be "1". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Chip Erase (CE). The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

The sequence of issuing CE instruction is: CS# goes low → sending CE instruction code → CS# goes high. (Please refer to *Figure 21*)

The self-timed Chip Erase Cycle time (tCE) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Chip Erase cycle is in progress. The WIP sets during the tCE timing, and clears when Chip Erase Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the chip is protected, the Chip Erase (CE) instruction will not be executed, but WEL will be reset.

(14) Page Program (PP)

The Page Program (PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). The device programs only the last 256 data bytes sent to the device. If the entire 256 data bytes are going to be programmed, A7-A0 (the eight least significant address bits) should be set to 0. If the eight least significant address bits (A7-A0) are not all 0, all transmitted data going beyond the end of the current page are programmed from the start address of the same page (from the address A7-A0 are all 0). If more than 256 bytes are sent to the device, the data of the last 256-byte is programmed at the requested page and previous data will be disregarded. If less than 256 bytes are sent to the device, the data is programmed at the requested address of the page without effect on other address of the same page.

The sequence of issuing PP instruction is: CS# goes low→ sending PP instruction code→ 3-byte address on SI→ at least 1-byte on data on SI→ CS# goes high. (Please refer to *Figure 22*)

The CS# must be kept to low during the whole Page Program cycle; The CS# must go high exactly at the byte boundary(the latest eighth bit of data being latched in), otherwise, the instruction will be rejected and will not be executed.

The self-timed Page Program Cycle time (tPP) is initiated as soon as Chip Select (CS#) goes high. The Write in Progress (WIP) bit still can be checked while the Page Program cycle is in progress. The WIP sets during the tPP timing, and clears when Page Program Cycle is completed, and the Write Enable Latch (WEL) bit is cleared. If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

(15) 4 x I/O Page Program (4PP)

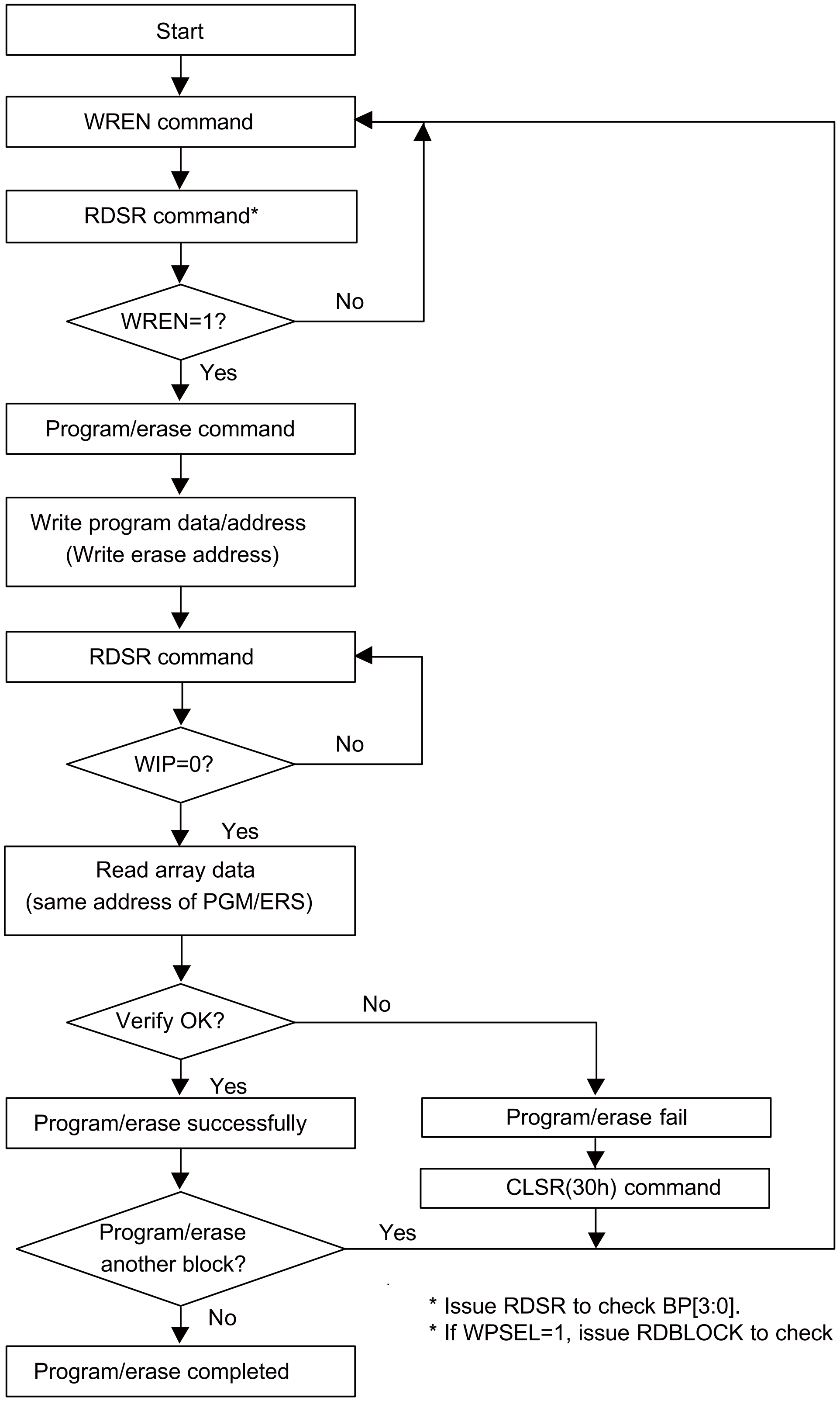
The Quad Page Program (4PP) instruction is for programming the memory to be "0". A Write Enable (WREN) instruction must be executed to set the Write Enable Latch (WEL) bit and Quad Enable (QE) bit must be set to "1" before sending the Quad Page Program (4PP). The Quad Page Programming takes four pins: SIO0, SIO1, SIO2, and SIO3, which can raise programer performance and and the effectiveness of application of lower clock less than 20MHz. For system with faster clock, the Quad page program cannot provide more performance, because the required internal page program time is far more than the time data flows in. Therefore, we suggest that while executing this command (especially during sending data), user can slow the clock speed down to 20MHz below. The other function descriptions are as same as standard page program.

The sequence of issuing 4PP instruction is: CS# goes low→ sending 4PP instruction code→ 3-byte address on SIO[3:0]→ at least 1-byte on data on SIO[3:0]→ CS# goes high. (Please refer to *Figure 23*)

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

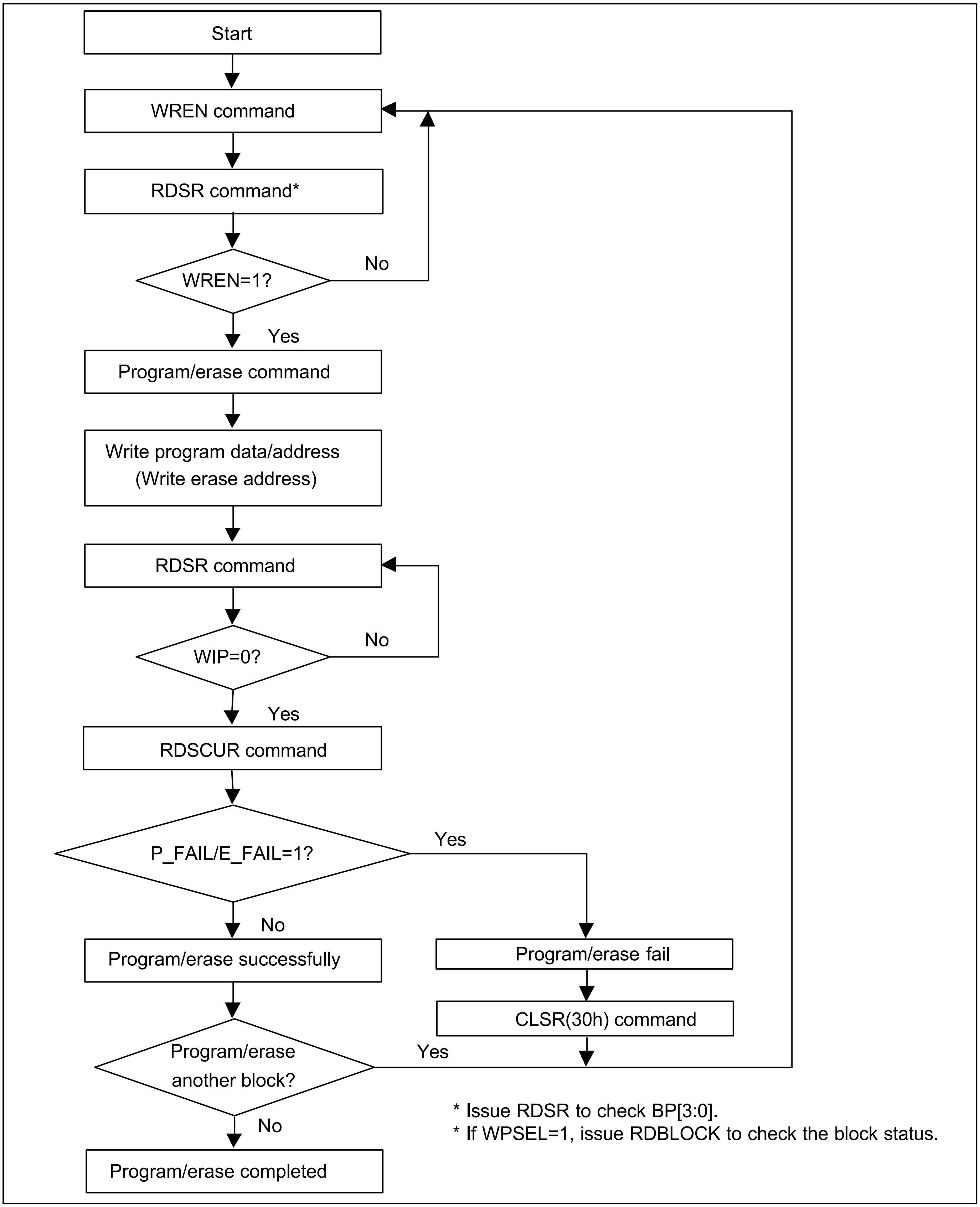
The Program/Erase function instruction function flow is as follows:

Program/Erase Flow(1) with read array data



* Issue RDSR to check BP[3:0].
* If WPSEL=1, issue RDBLOCK to check the block status.

Program/Erase Flow(2) without read array data



* Issue RDSR to check BP[3:0].
* If WPSEL=1, issue RDBLOCK to check the block status.

(16) Continuously program mode (CP mode)

The CP mode may enhance program performance by automatically increasing address to the next higher address after each byte data has been programmed.

The Continuously program (CP) instruction is for multiple byte program to Flash. A write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Continuously program (CP) instruction. CS# requires to go high before CP instruction is executing. After CP instruction and address input, two bytes of data is input sequentially from MSB(bit7) to LSB(bit0). The first byte data will be programmed to the initial address range with A0=0 and second byte data with A0=1. If only one byte data is input, the CP mode will not process. If more than two bytes data are input, the additional data will be ignored and only two byte data are valid. Any byte to be programmed should be in the erase state (FF) first. It will not roll over during the CP mode, once the last unprotected address has been reached, the chip will exit CP mode and reset write Enable Latch bit (WEL) as "0" and CP mode bit as "0". Please check the WIP bit status if it is not in write progress before entering next valid instruction. During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex). And the WRDI command is valid after completion of a CP programming cycle, which means the WIP bit=0.

The sequence of issuing CP instruction is : CS# goes low → sending CP instruction code → 3-byte address on SI pin → two data bytes on SI → CS# goes high to low → sending CP instruction and then continue two data bytes are programmed → CS# goes high to low → till last desired two data bytes are programmed → CS# goes high to low →sending WRDI (Write Disable) instruction to end CP mode → send RDSR instruction to verify if CP mode word program ends, or send RDSCUR to check bit4 to verify if CP mode ends. (Please refer to *Figure 24*)

Two methods to detect the completion of a program cycle during CP mode:
1) Software method-I: by checking WIP bit of Status Register to detect the completion of CP mode.
2) Software method-II: by waiting for a tBP time out to determine if it may load next valid command or not.
3) Hardware method: by writing ESRY (enable SO to output RY/BY#) instruction to detect the completion of a program cycle during CP mode. The ESRY instruction must be executed before CP mode execution. Once it is enable in CP mode, the CS# goes low will drive out the RY/BY# status on SO, "0" indicates busy stage, "1" indicates ready stage, SO pin outputs tri-state if CS# goes high. DSRY (disable SO to output RY/BY#) instruction to disable the SO to output RY/BY# and return to status register data output during CP mode. Please note that the ESRY/DSRY command are not accepted unless the completion of CP mode.

If the page is protected by BP3~0 (WPSEL=0) or by individual lock (WPSEL=1), the array data will be protected (no change) and the WEL bit will still be reset.

(17) Deep Power-down (DP)

The Deep Power-down (DP) instruction is for setting the device to minimum power consumption (the standby current is reduced from ISB1 to ISB2). The Deep Power-down mode requires the Deep Power-down (DP) instruction to enter, during the Deep Power-down mode, the device is not active and all Write/Program/Erase instruction are ignored.

The sequence of issuing DP instruction is: CS# goes low→ sending DP instruction code→ CS# goes high. (Please refer to *Figure 25*)

Once the DP instruction is set, all instruction will be ignored except the Release from Deep Power-down mode (RDP) and Read Electronic Signature (RES) instruction. (those instructions allow the ID being reading out). When Power-down, the deep power-down mode automatically stops, and when power-up, the device automatically is in standby mode. For RDP instruction the CS# must go high exactly at the byte boundary (the latest eighth bit of instruction code been latched-in); otherwise, the instruction will not executed. As soon as Chip Select (CS#) goes high, a delay of tDP is required before entering the Deep Power-down mode and reducing the current to ISB2.

(18) Release from Deep Power-down (RDP), Read Electronic Signature (RES)

The Release from Deep Power-down (RDP) instruction is completed by driving Chip Select (CS#) High. When Chip Select (CS#) is driven High, the device is put in the Standby Power mode. If the device was not previously in the Deep Power-down mode, the transition to the standby Power mode is immediate. If the device was previously in the Deep Power-down mode, though, the transition to the standby Power mode is delayed by tRES2, and Chip Select (CS#) must remain High for at least tRES2(max), as specified in *Table 11*. Once in the standby mode, the device waits to be selected, so that it can receive, decode and execute instructions.

RES instruction is for reading out the old style of 8-bit Electronic Signature, whose values are shown as table of *ID Definitions*. This is not the same as RDID instruction. It is not recommended to use for new design. For new design, please use RDID instruction. Even in Deep power-down mode, the RDP and RES are also allowed to be executed, only except the device is in progress of program/erase/write cycles; there's no effect on the current program/erase/write cycles in progress. The sequence is shown as *Figure 26*, *Figure 27*.

The RES instruction is ended by CS# goes high after the ID been read out at least once. The ID outputs repeatedly if continuously send the additional clock cycles on SCLK while CS# is at low. If the device was not previously in Deep Power-down mode, the device transition to standby mode is immediate. If the device was previously in Deep Power-down mode, there's a delay of tRES2 to transit to standby mode, and CS# must remain to high at least tRES2(max). Once in the standby mode, the device waits to be selected, so it can be receive, decode, and execute instruction.

The RDP instruction is for releasing from Deep Power-down Mode.

(19) Read Electronic Manufacturer ID & Device ID (REMS), (REMS2), (REMS4)

The REMS, REMS2 and REMS4 instruction provides both the JEDEC assigned Manufacturer ID and the specific Device ID.

The instruction is initiated by driving the CS# pin low and shift the instruction code "90h", "DFh" or "EFh" followed by two dummy bytes and one bytes address (A7~A0). After which, the Manufacturer ID for MXIC (C2h) and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in Figure 34. The Device ID values are listed in table of *ID Definitions*. If the one-byte address is initially set to 01h, then the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving CS# high.

Table 6. ID Definitions

Command Type	MX25L6436E		
RDID	manufacturer ID	memory type	memory density
	C2	20	17
RES	electronic ID		
	16		
REMS/REMS2/REMS4	manufacturer ID	device ID	
	C2	16	

(20) Enter Secured OTP (ENSO)

The ENSO instruction is for entering the additional 4K-bit Secured OTP mode. While device is in 4K-bit Secured OTP mode, main array access is not available. The additional 4K-bit Secured OTP is independent from main array, and may be used to store unique serial number for system identifier. After entering the Secured OTP mode, follow standard read or program procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down.

The sequence of issuing ENSO instruction is: CS# goes low→ sending ENSO instruction to enter Secured OTP mode→ CS# goes high.

Please note that WRSR/WRSCUR/WPSEL/SBLK/GBLK/SBULK/GBULK/CE/BE/SE/BE32K commands are not acceptable during the access of secure OTP region, once Security OTP is lock down, only read related commands are valid.

(21) Exit Secured OTP (EXSO)

The EXSO instruction is for exiting the additional 4K-bit Secured OTP mode.

The sequence of issuing EXSO instruction is: CS# goes low→ sending EXSO instruction to exit Secured OTP mode→ CS# goes high.

(22) Read Security Register (RDSCUR)

The RDSCUR instruction is for reading the value of Security Register. The Read Security Register can be read at any time (even in program/erase/write status register/write security register condition) and continuously.

The sequence of issuing RDSCUR instruction is : CS# goes low→ sending RDSCUR instruction → Security Register data out on SO→ CS# goes high.

The definition of the Security Register is as below:

Secured OTP Indicator bit. The Secured OTP indicator bit shows the chip is locked by factory before ex- factory or not. When it is "0", it indicates non-factory lock; "1" indicates factory- lock.

Lock-down Secured OTP (LDSO) bit. By writing WRSCUR instruction, the LDSO bit may be set to "1" for customer lock-down purpose. However, once the bit is set to "1" (lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more.

Continuously Program Mode (CP mode) bit. The Continuously Program Mode bit indicates the status of CP mode, "0" indicates not in CP mode; "1" indicates in CP mode.

Program Fail Flag bit. If the program operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more program operations. This fail flag bit will be reset by command CLSR (30h).

Erase Fail Flag bit. If the erase operation fails on a protected memory region or locked OTP region, this bit will also be set. This bit can be the failure indication of one or more erase operations. This fail flag bit will be reset by command CLSR (30h).

Write Protection Select bit. The Write Protection Select bit indicates that WPSEL has been executed successfully. Once this bit has been set (WPSEL=1), all the blocks or sectors will be write-protected after the power-on every time. Once WPSEL has been set, it cannot be changed again, which means it's only for individual WP mode.

Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

Security Register Definition

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
WPSEL	E_FAIL	P_FAIL	Continuously Program mode (CP mode)	x	x	LDSO (lock-down 4K-bit Secured OTP)	4K-bit Secured OTP
0=normal WP mode 1=individual WP mode (default=0)	0=normal Erase succeed 1=indicate Erase failed (default=0)	0=normal Program succeed 1=indicate Program failed (default=0)	0=normal Program mode 1=CP mode (default=0)	reserved	reserved	0 = not lockdown 1 = lock-down (cannot program/ erase OTP)	0 = nonfactory lock 1 = factory lock
non-volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	volatile bit	non-volatile bit	non-volatile bit
OTP	Read Only	Read Only	Read Only	Read Only	Read Only	OTP	Read Only

(23) Write Security Register (WRSCUR)

The WRSCUR instruction is for changing the values of Security Register Bits. Unlike write status register, the WREN instruction is not required before sending WRSCUR instruction. The WRSCUR instruction may change the values of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to "1", the Secured OTP area cannot be updated any more.

The sequence of issuing WRSCUR instruction is :CS# goes low→ sending WRSCUR instruction → CS# goes high.

The CS# must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

(24) Write Protection Selection (WPSEL)

There are two write protection methods, (1) BP protection mode (2) individual block protection mode. If WPSEL=0, flash is under BP protection mode . If WPSEL=1, flash is under individual block protection mode. The default value of WPSEL is “0”. WPSEL command can be used to set WPSEL=1. **Please note that WPSEL is an OTP bit. Once WPSEL is set to 1, there is no chance to recovery WPSEL back to “0”.** If the flash is put on BP mode, the individual block protection mode is disabled. Contrarily, if flash is on the individual block protection mode, the BP mode is disabled.

Every time after the system is powered-on the Security Register bit 7 is checked. If WPSEL=1, all the blocks and sectors will be write protected by default. User may only unlock the blocks or sectors via SBULK and GBULK instructions. Program or erase functions can only be operated after the Unlock instruction is executed.

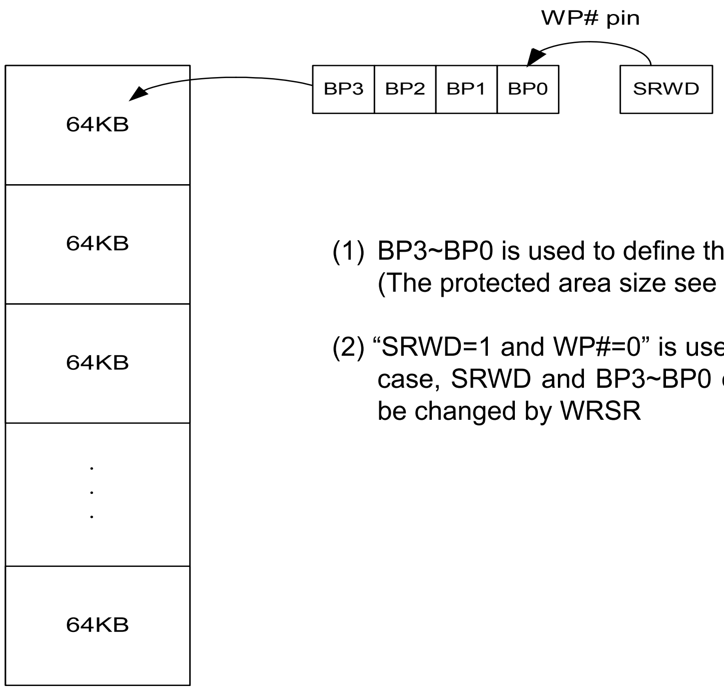
BP protection mode, WPSEL=0:
ARRAY is protected by BP3~BP0 and BP3~BP0 bits are protected by “SRWD=1 and WP#=0”, where SRWD is bit 7 of status register that can be set by WRSR command.

Individual block protection mode, WPSEL=1:
Blocks are individually protected by their own SRAM lock bits which are set to “1” after power up. SBULK and SBLK command can set SRAM lock bit to “0” and “1”. When the system accepts and executes WPSEL instruction, bit 7 in the security register will be set. It will activate SBLK, SBULK, RDBLOCK, GBLK, GBULK etc instructions to conduct block lock protection and replace the original Software Protect Mode (SPM) use (BP3~BP0) indicated block methods. Under the individual block protection mode (WPSEL=1), hardware protection is performed by driving WP#=0. Once WP#=0 all array blocks/sectors are protected regardless of the contents of SRAM lock bits.

The sequence of issuing WPSEL instruction is: CS# goes low → sending WPSEL instruction to enter the individual block protect mode → CS# goes high.

WPSEL instruction function flow is as follows:

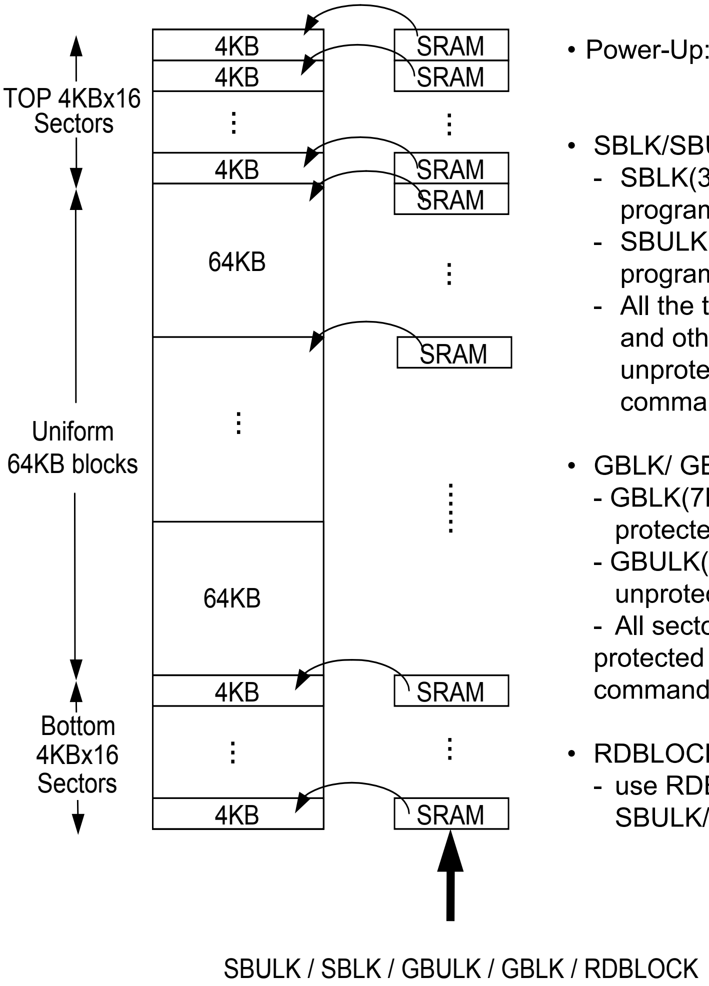
BP and SRWD if WPSEL=0



(1) BP3~BP0 is used to define the protection group region. (The protected area size see *Table 2*)

(2) “SRWD=1 and WP#=0” is used to protect BP3~BP0. In this case, SRWD and BP3~BP0 of status register bits can not be changed by WRSR

The individual block lock mode is effective after setting WPSEL=1



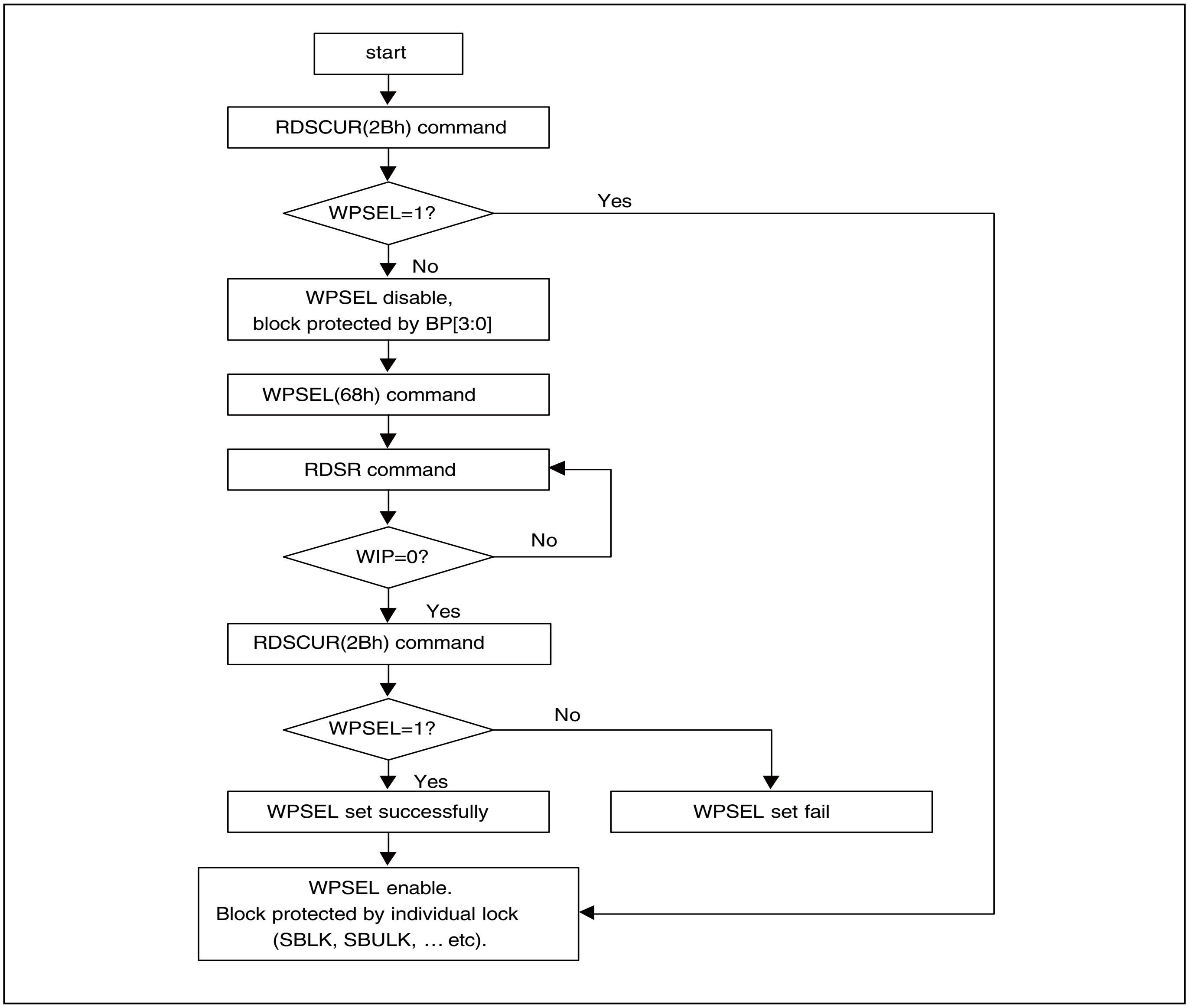
- Power-Up: All SRAM bits=1 (all blocks are default protected).
  All array cannot be programmed/erased

- SBLK/SBULK(36h/39h):
  - SBLK(36h): Set SRAM bit=1 (protect): array can not be programmed/erased
  - SBULK(39h): Set SRAM bit=0 (unprotect): array can be programmed/erased
  - All the top 4KBx16 sectors and bottom 4KBx16 sectors and other 64KB uniform blocks can be protected and unprotected with SRAM bits individually by SBLK/SBULK command set.

- GBLK/ GBULK(7Eh/98h):
  - GBLK(7Eh): Set all SRAM bits=1, the whole chip is protected and cannot be programmed/erased.
  - GBULK(98h): Set all SRAM bits=0, the whole chip is unprotected and can be programmed/erased.
  - All sectors and blocks SRAM bits of the whole chip can be protected and unprotected at one time by GBLK/GBULK command set.

- RDBLOCK(3Ch):
  - use RDBLOCK mode to check the SRAM bits status after SBULK/SBLK/GBULK/GBLK command set.

WPSEL Flow


start
RDSCUR(2Bh) command
WPSEL=1?
Yes
No
WPSEL disable,
block protected by BP[3:0]
WPSEL(68h) command
RDSR command
WIP=0?
No
Yes
RDSCUR(2Bh) command
WPSEL=1?
No
Yes
WPSEL set successfully
WPSEL set fail
WPSEL enable.
Block protected by individual lock
(SBLK, SBULK, … etc).

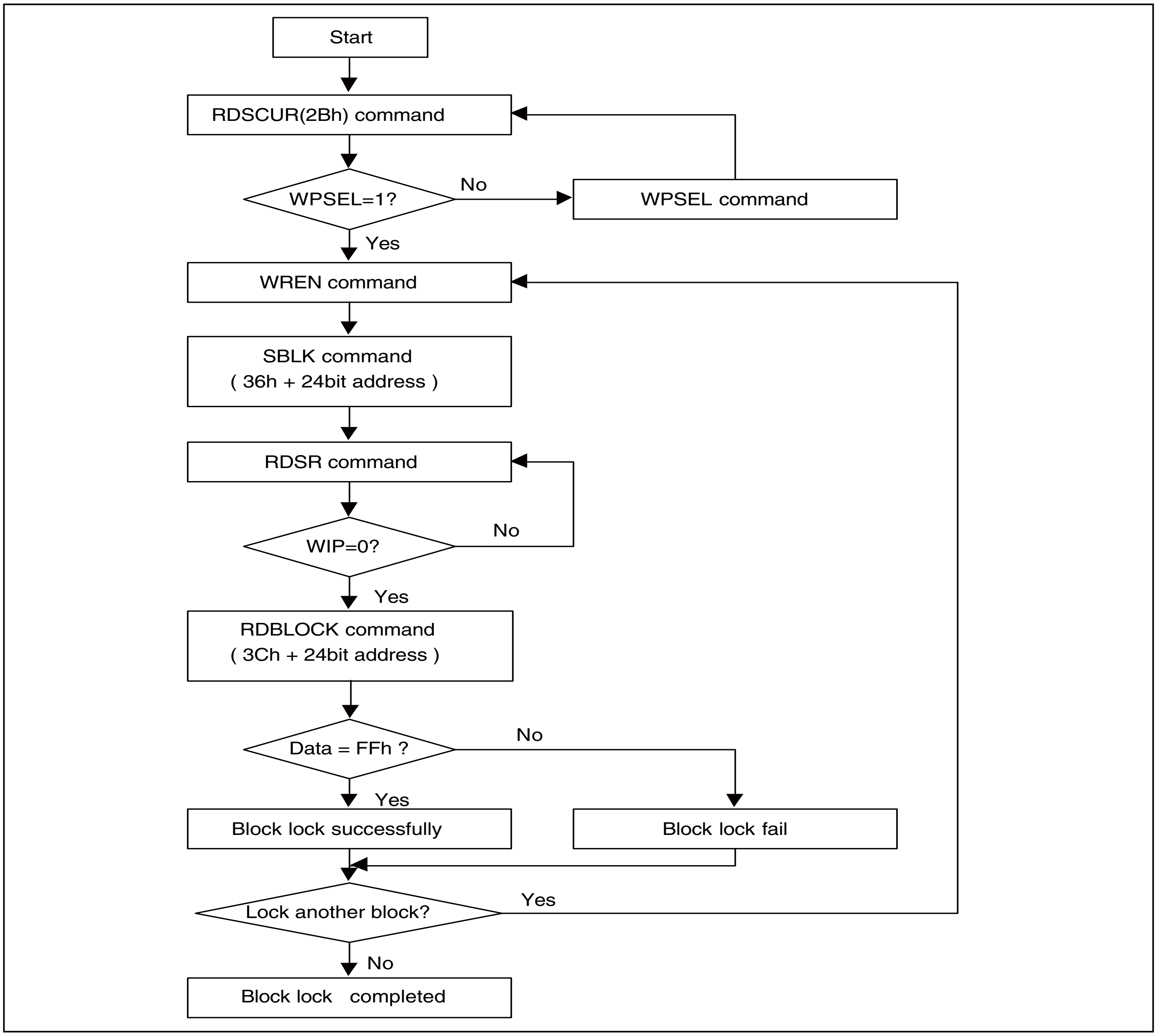
(25) Single Block Lock/Unlock Protection (SBLK/SBULK)

These instructions are only effective after WPSEL was executed. The SBLK instruction is for write protection a specified block(or sector) of memory, using A23-A16 or (A23-A12) address bits to assign a 64Kbyte block (or 4K bytes sector) to be protected as read only. The SBULK instruction will cancel the block (or sector) write protection state. This feature allows user to stop protecting the entire block (or sector) through the chip unprotect command (GBULK).

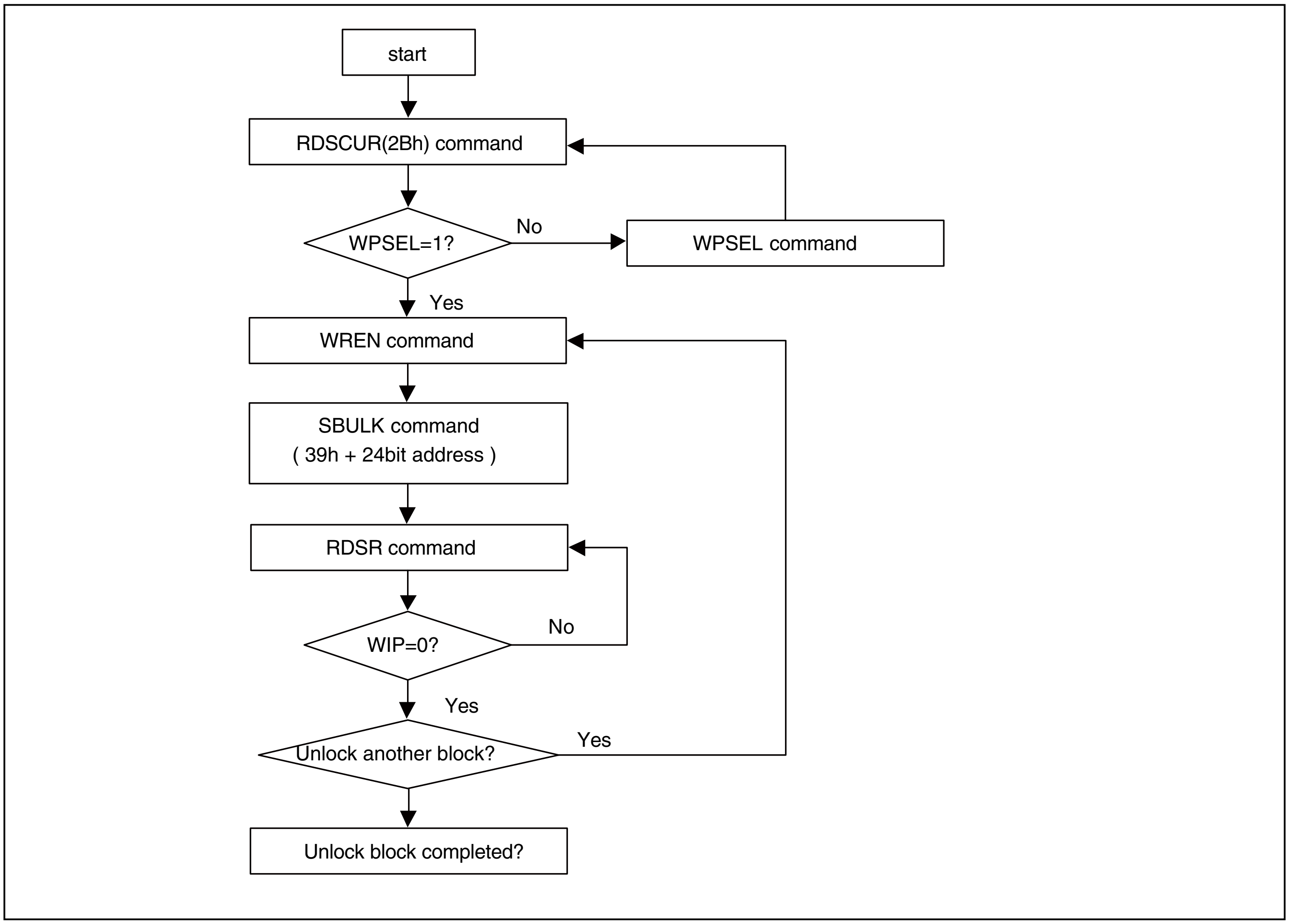
The WREN (Write Enable) instruction is required before issuing SBLK/SBULK instruction.
The sequence of issuing SBLK/SBULK instruction is: CS# goes low → send SBLK/SBULK (36h/39h) instruction → send 3 address bytes assign one block (or sector) to be protected on SI pin → CS# goes high. (Please refer to *Figure 30*)
The CS# must go high exactly at the byte boundary, otherwise the instruction will be rejected and not be executed.

SBLK/SBULK instruction function flow is as follows:

Block Lock Flow



Block Unlock Flow



(26) Read Block Lock Status (RDBLOCK)

This instruction is only effective after WPSEL was executed. The RDBLOCK instruction is for reading the status of protection lock of a specified block (or sector), using A23-A16 (or A23-A12) address bits to assign a 64K bytes block (4K bytes sector) and read protection lock status bit which the first byte of Read-out cycle. The status bit is"1" to indicate that this block has be protected, that user can read only but cannot write/program /erase this block. The status bit is "0" to indicate that this block hasn't be protected, and user can read and write this block.

The sequence of issuing RDBLOCK instruction is: CS# goes low → send RDBLOCK (3Ch) instruction → send 3 address bytes to assign one block on SI pin → read block's protection lock status bit on SO pin → CS# goes high. (Please refer to *Figure 31*)

(27) Gang Block Lock/Unlock (GBLK/GBULK)

These instructions are only effective after WPSEL was executed. The GBLK/GBULK instruction is for enable/disable the lock protection block of the whole chip.

The WREN (Write Enable) instruction is required before issuing GBLK/GBULK instruction.
The sequence of issuing GBLK/GBULK instruction is: CS# goes low → send GBLK/GBULK (7Eh/98h) instruction → CS# goes high. (Please refer to *Figure 32*)

The CS# must go high exactly at the byte boundary, otherwise, the instruction will be rejected and not be executed.

(28) Clear SR Fail Flags (CLSR)

The CLSR instruction is for resetting the Program/Erase Fail Flag bit of Security Register. It should be executed before program/erase another block during programming/erasing flow without read array data.

The sequence of issuing CLSR instruction is: CS# goes low → send CLSR instruction code → CS# goes high.

The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(29) Enable SO to Output RY/BY# (ESRY)

The ESRY instruction is for outputting the ready/busy status to SO during CP mode.
The sequence of issuing ESRY instruction is: CS# goes low → sending ESRY instruction code → CS# goes high.
The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(30) Disable SO to Output RY/BY# (DSRY)

The DSRY instruction is for resetting ESRY during CP mode. The ready/busy status will not output to SO after DSRY issued.

The sequence of issuing DSRY instruction is: CS# goes low → send DSRY instruction code → CS# goes high.
The CS# must go high exactly at the byte boundary; otherwise, the instruction will be rejected and not executed.

(31) Read SFDP Mode (RDSFDP)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI.

The sequence of issuing RDSFDP instruction is CS# goes low→send RDSFDP instruction (5Ah)→send 3 address bytes on SI pin→send 1 dummy byte on SI pin→read SFDP code on SO→to end RDSFDP operation can use CS# to high at any time during data out.

SFDP is a JEDEC Standard, JESD216.

Read Serial Flash Discoverable Parameter (RDSFDP) Sequence

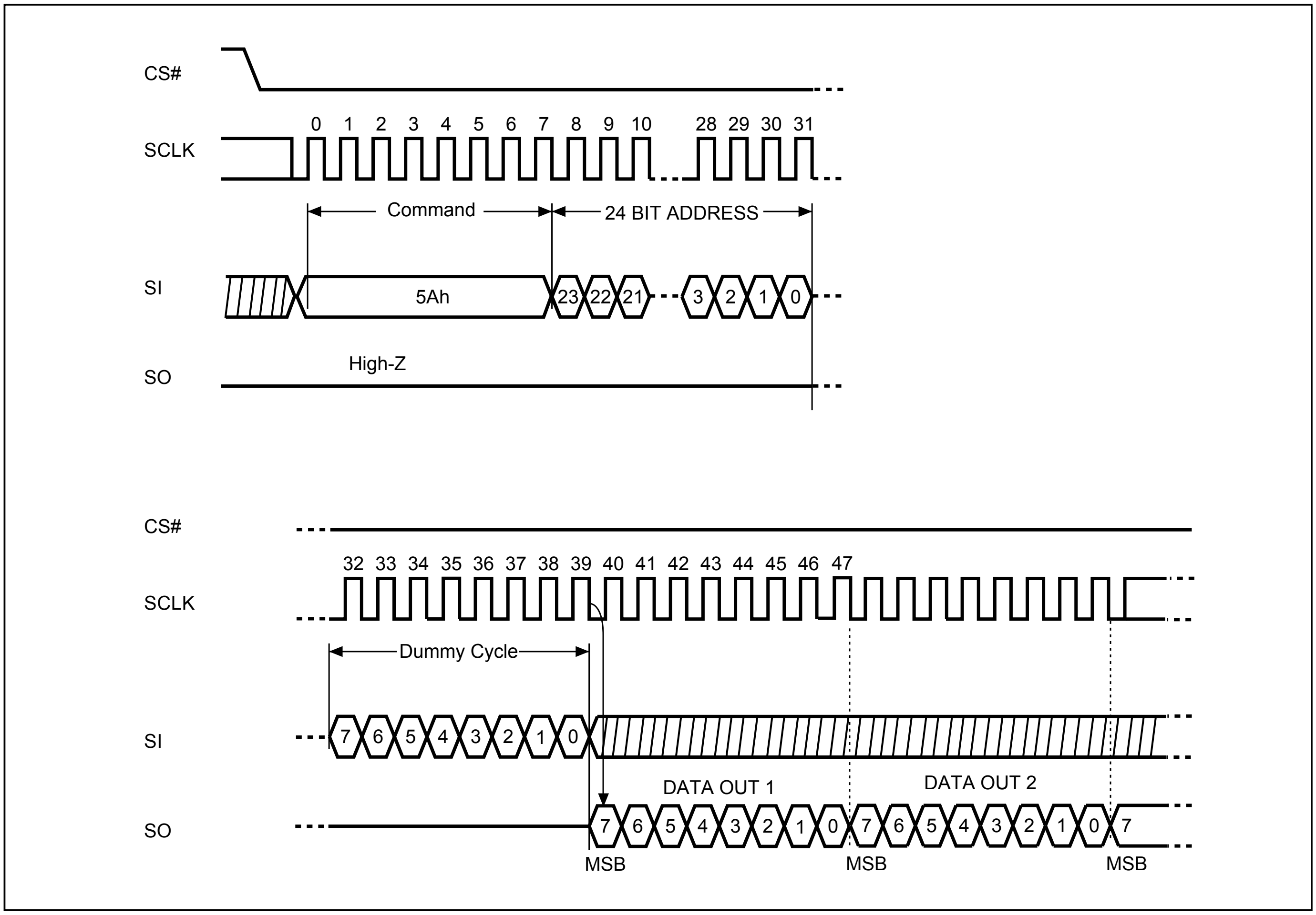


Table 7. Signature and Parameter Identification Data Values

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
SFDP Signature	Fixed: 50444653h	00h	07:00	53h	53h
		01h	15:08	46h	46h
		02h	23:16	44h	44h
		03h	31:24	50h	50h
SFDP Minor Revision Number	Start from 00h	04h	07:00	00h	00h
SFDP Major Revision Number	Start from 01h	05h	15:08	01h	01h
Number of Parameter Headers	This number is 0-based. Therefore, 0 indicates 1 parameter header.	06h	23:16	01h	01h
Unused		07h	31:24	FFh	FFh
ID number (JEDEC)	00h: it indicates a JEDEC specified header.	08h	07:00	00h	00h
Parameter Table Minor Revision Number	Start from 00h	09h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	0Ah	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	0Bh	31:24	09h	09h
Parameter Table Pointer (PTP)	First address of JEDEC Flash Parameter table	0Ch	07:00	30h	30h
		0Dh	15:08	00h	00h
		0Eh	23:16	00h	00h
Unused		0Fh	31:24	FFh	FFh
ID number (Macronix manufacturer ID)	it indicates Macronix manufacturer ID	10h	07:00	C2h	C2h
Parameter Table Minor Revision Number	Start from 00h	11h	15:08	00h	00h
Parameter Table Major Revision Number	Start from 01h	12h	23:16	01h	01h
Parameter Table Length (in double word)	How many DWORDs in the Parameter table	13h	31:24	04h	04h
Parameter Table Pointer (PTP)	First address of Macronix Flash Parameter table	14h	07:00	60h	60h
		15h	15:08	00h	00h
		16h	23:16	00h	00h
Unused		17h	31:24	FFh	FFh

Table 8. Parameter Table (0): JEDEC Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Block/Sector Erase sizes	00: Reserved, 01: 4KB erase, 10: Reserved, 11: not suport 4KB erase	30h	01:00	01b	E5h
Write Granularity	0: 1Byte, 1: 64Byte or larger		02	1b	
Write Enable Instruction Required for Writing to Volatile Status Registers	0: not required 1: required 00h to be written to the status register		03	0b	
Write Enable Opcode Select for Writing to Volatile Status Registers	0: use 50h opcode, 1: use 06h opcode Note: If target flash status register is nonvolatile, then bits 3 and 4 must be set to 00b.		04	0b	
Unused	Contains 111b and can never be changed		07:05	111b	
4KB Erase Opcode		31h	15:08	20h	20h
(1-1-2) Fast Read (Note2)	0=not support 1=support	32h	16	1b	C1h
Address Bytes Number used in addressing flash array	00: 3Byte only, 01: 3 or 4Byte, 10: 4Byte only, 11: Reserved		18:17	00b	
Double Transfer Rate (DTR) Clocking	0=not support 1=support		19	0b	
(1-2-2) Fast Read	0=not support 1=support		20	0b	
(1-4-4) Fast Read	0=not support 1=support		21	0b	
(1-1-4) Fast Read	0=not support 1=support		22	1b	
Unused			23	1b	
Unused		33h	31:24	FFh	FFh
Flash Memory Density		37h:34h	31:00	03FF FFFFh	
(1-4-4) Fast Read Number of Wait states (Note3)	0 0000b: Wait states (Dummy Clocks) not support	38h	04:00	0 0000b	00h
(1-4-4) Fast Read Number of Mode Bits (Note4)	000b: Mode Bits not support		07:05	000b	
(1-4-4) Fast Read Opcode		39h	15:08	FFh	FFh
(1-1-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ah	20:16	0 1000b	08h
(1-1-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-1-4) Fast Read Opcode		3Bh	31:24	6Bh	6Bh

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
(1-1-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Ch	04:00	0 1000b	08h
(1-1-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		07:05	000b	
(1-1-2) Fast Read Opcode		3Dh	15:08	3Bh	3Bh
(1-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	3Eh	20:16	0 0000b	00h
(1-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(1-2-2) Fast Read Opcode		3Fh	31:24	FFh	FFh
(2-2-2) Fast Read	0=not support 1=support	40h	00	0b	EEh
Unused			03:01	111b	
(4-4-4) Fast Read	0=not support 1=support		04	0b	
Unused			07:05	111b	
Unused		43h:41h	31:08	FFh	FFh
Unused		45h:44h	15:00	FFh	FFh
(2-2-2) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	46h	20:16	0 000b	00h
(2-2-2) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(2-2-2) Fast Read Opcode		47h	31:24	FFh	FFh
Unused		49h:48h	15:00	FFh	FFh
(4-4-4) Fast Read Number of Wait states	0 0000b: Wait states (Dummy Clocks) not support	4Ah	20:16	0 0000b	00h
(4-4-4) Fast Read Number of Mode Bits	000b: Mode Bits not support		23:21	000b	
(4-4-4) Fast Read Opcode		4Bh	31:24	FFh	FFh
Sector Type 1 Size	Sector/block size = 2^N bytes (Note5) 0x00b: this sector type doesn't exist	4Ch	07:00	0Ch	0Ch
Sector Type 1 erase Opcode		4Dh	15:08	20h	20h
Sector Type 2 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	4Eh	23:16	0Fh	0Fh
Sector Type 2 erase Opcode		4Fh	31:24	52h	52h
Sector Type 3 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	50h	07:00	10h	10h
Sector Type 3 erase Opcode		51h	15:08	D8h	D8h
Sector Type 4 Size	Sector/block size = 2^N bytes 0x00b: this sector type doesn't exist	52h	23:16	00h	00h
Sector Type 4 erase Opcode		53h	31:24	FFh	FFh

Table 9. Parameter Table (1): Macronix Flash Parameter Tables

Description	Comment	Add (h) (Byte)	DW Add (Bit)	Data (h/b) (Note1)	Data (h)
Vcc Supply Maximum Voltage	2000h=2.000V 2700h=2.700V 3600h=3.600V	61h:60h	07:00 15:08	00h 36h	00h 36h
Vcc Supply Minimum Voltage	1650h=1.650V 2250h=2.250V 2350h=2.350V 2700h=2.700V	63h:62h	23:16 31:24	00h 27h	00h 27h
H/W Reset# pin	0=not support 1=support	65h:64h	00	0b	4FF4h
H/W Hold# pin	0=not support 1=support		01	0b	
Deep Power Down Mode	0=not support 1=support		02	1b	
S/W Reset	0=not support 1=support		03	0b	
S/W Reset Opcode	Reset Enable (66h) should be issued before Reset Opcode		11:04	1111 1111b (FFh)	
Program Suspend/Resume	0=not support 1=support		12	0b	
Erase Suspend/Resume	0=not support 1=support		13	0b	
Unused			14	1b	
Wrap-Around Read mode	0=not support 1=support		15	0b	
Wrap-Around Read mode Opcode		66h	23:16	FFh	FFh
Wrap-Around Read data length	08h:support 8B wrap-around read 16h:8B&16B 32h:8B&16B&32B 64h:8B&16B&32B&64B	67h	31:24	FFh	FFh
Individual block lock	0=not support 1=support	6Bh:68h	00	1b	C8D9h
Individual block lock bit (Volatile/Nonvolatile)	0=Volatile 1=Nonvolatile		01	0b	
Individual block lock Opcode			09:02	0011 0110b (36h)	
Individual block lock Volatile protect bit default protect status	0=protect 1=unprotect		10	0b	
Secured OTP	0=not support 1=support		11	1b	
Read Lock	0=not support 1=support		12	0b	
Permanent Lock	0=not support 1=support		13	0b	
Unused			15:14	11b	
Unused			31:16	FFh	FFh
Unused		6Fh:6Ch	31:00	FFh	FFh

Note 1: h/b is hexadecimal or binary.

Note 2: **(x-y-z)** means I/O mode nomenclature used to indicate the number of active pins used for the opcode (x), address (y), and data (z). At the present time, the only valid Read SFDP instruction modes are: (1-1-1), (2-2-2), and (4-4-4)

Note 3: **Wait States** is required dummy clock cycles after the address bits or optional mode bits.

Note 4: **Mode Bits** is optional control bits that follow the address bits. These bits are driven by the system controller if they are specified. (eg,read performance enhance toggling bits)

Note 5: 4KB=2^0Ch,32KB=2^0Fh,64KB=2^10h

Note 6: All unused and undefined area data is blank FFh.

POWER-ON STATE

The device is at the following states after power-up:

- Standby mode (please note it is not Deep Power-down mode)
- Write Enable Latch (WEL) bit is reset

The device must not be selected during power-up and power-down stage until the VCC reaches the following levels:

- VCC minimum at power-up stage and then after a delay of tVSL
- GND at power-down

Please note that a pull-up resistor on CS# may ensure a safe and proper power-up/down level.

An internal Power-on Reset (POR) circuit may protect the device from data corruption and inadvertent data change during power up state.

For further protection on the device, if the VCC does not reach the VCC minimum level, the correct operation is not guaranteed. The read, write, erase, and program command should be sent after the time delay:

- tVSL after VCC reached VCC minimum level

The device can accept read command after VCC reached VCC minimum and a time delay of tVSL.

Please refer to the figure of "*Power-up Timing*".

Note:

- To stabilize the VCC level, the VCC rail decoupled by a suitable capacitor close to package pins is recommended. (generally around 0.1uF)

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

RATING		VALUE
Ambient Operating Temperature	Industrial grade	-40°C to 85°C
Storage Temperature		-65°C to 150°C
Applied Input Voltage		-0.5V to 4.6V
Applied Output Voltage		-0.5V to 4.6V
VCC to Ground Potential		-0.5V to 4.6V

NOTICE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is stress rating only and functional operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.
2. Specifications contained within the following tables are subject to change.
3. During voltage transitions, all pins may overshoot Vss to -2.0V and Vcc to +2.0V for periods up to 20ns, see Figure 2, 3.

Figure 3. Maximum Negative Overshoot Waveform

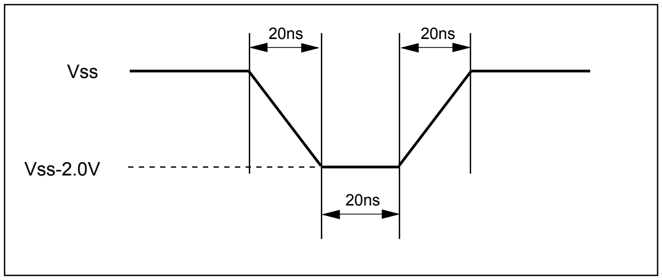
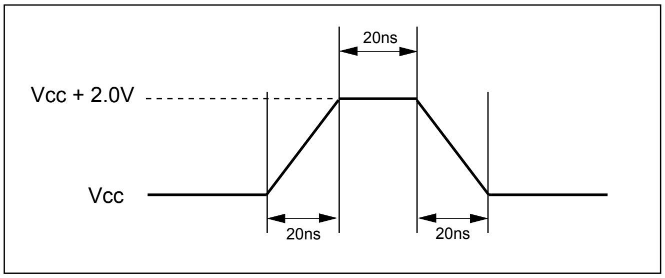


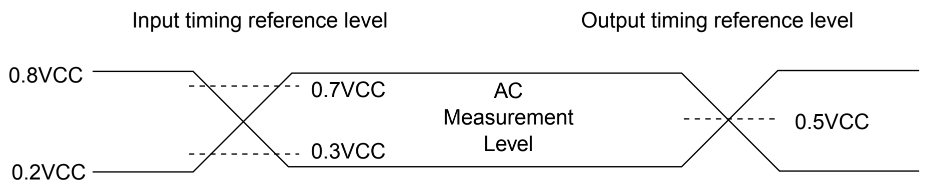
Figure 4. Maximum Positive Overshoot Waveform



CAPACITANCE TA = 25°C, f = 1.0 MHz

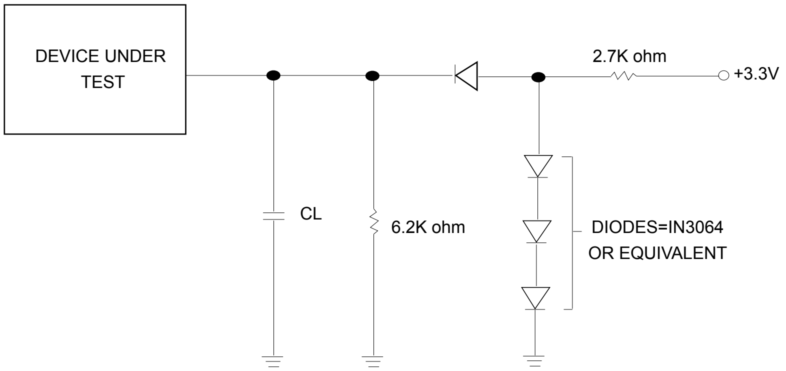
Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			10	pF	VIN = 0V
COUT	Output Capacitance			8	pF	VOUT = 0V

Figure 5. INPUT TEST WAVEFORMS AND MEASUREMENT LEVEL



Note: Input pulse rise and fall time are <5ns

Figure 6. OUTPUT LOADING



CL=30/15pF Including jig capacitance

Table 10. DC CHARACTERISTICS

Symbol	Parameter	Notes	Min.	Max.	Units	Test Conditions
ILI	Input Load Current	1		± 2	uA	VCC = VCC Max, VIN = VCC or GND
ILO	Output Leakage Current	1		± 2	uA	VCC = VCC Max, VOUT=VCC or GND
ISB1	VCC Standby Current	1		50	uA	VIN = VCC or GND, CS# = VCC
ISB2	Deep Power-down Current			20	uA	VIN = VCC or GND, CS# = VCC
ICC1	VCC Read	1		22	mA	fQ=75MHz (4 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				19	mA	f=104MHz SCLK=0.1VCC/0.9VCC, SO=Open
				17	mA	fT=70MHz (2 x I/O read) SCLK=0.1VCC/0.9VCC, SO=Open
				15	mA	f=66MHz SCLK=0.1VCC/0.9VCC, SO=Open
				10	mA	f=33MHz, SCLK=0.1VCC/0.9VCC, SO=Open
ICC2	VCC Program Current (PP)	1		25	mA	Program in Progress, CS# = VCC
ICC3	VCC Write Status Register (WRSR) Current			20	mA	Program status register in progress, CS#=VCC
ICC4	VCC Sector Erase Current (SE)	1		25	mA	Erase in Progress, CS#=VCC
ICC5	VCC Chip Erase Current (CE)	1		20	mA	Erase in Progress, CS#=VCC
VIL	Input Low Voltage		-0.5	0.8	V	
VIH	Input High Voltage		0.7VCC	VCC+0.4	V	
VOL	Output Low Voltage			0.4	V	IOL = 1.6mA
VOH	Output High Voltage		VCC-0.2		V	IOH = -100uA

Notes :

1. Typical values at VCC = 3.3V, T = 25°C. These currents are valid for all product versions (package and speeds).
2. Typical value is calculated by simulation.

Table 11. AC CHARACTERISTICS

Symbol	Alt.	Parameter			Min.	Typ.	Max.	Unit
fSCLK	fC	Clock Frequency for the following instructions: FAST_READ, RDSFDP, PP, SE, BE, CE, DP, RES, RDP, WREN, WRDI, RDID, RDSR, WRSR			D.C.		104	MHz
fRSCLK	fR	Clock Frequency for READ instructions					50	MHz
fTSCLK	fT	Clock Frequency for DREAD instructions					70	MHz
	fQ	Clock Frequency for QREAD instructions		VCC=2.7V-3.6V			75	MHz
				VCC=3.0V-3.6V			85	MHz
f4PP		Clock Frequency for 4PP (Quad page program)					20	MHz
tCH(1)	tCLH	Clock High Time		Fast_Read	4.5			ns
				Read	9			ns
tCL(1)	tCLL	Clock Low Time		Fast_Read	4.5			ns
				Read	9			ns
tCLCH(2)		Clock Rise Time (3) (peak to peak)			0.1			V/ns
tCHCL(2)		Clock Fall Time (3) (peak to peak)			0.1			V/ns
tSLCH	tCSS	CS# Active Setup Time (relative to SCLK)			5			ns
tCHSL		CS# Not Active Hold Time (relative to SCLK)			5			ns
tDVCH	tDSU	Data In Setup Time			2			ns
tCHDX	tDH	Data In Hold Time			5			ns
tCHSH		CS# Active Hold Time (relative to SCLK)			5			ns
tSHCH		CS# Not Active Setup Time (relative to SCLK)			5			ns
tSHSL(3)	tCSH	CS# Deselect Time		Read	15			ns
				Write/Erase/ Program	50			ns
tSHQZ(2)	tDIS	Output Disable Time		VCC=2.7V-3.6V			10	ns
				VCC=3.0V-3.6V			8	ns
tCLQV	tV	Clock Low to Output Valid VCC=2.7V~3.6V	Loading: 15pF	1 I/O			9	ns
				2 I/O & 4 I/O			9.5	ns
			Loading: 30pF	2 I/O & 4 I/O			12	ns
tCLQX	tHO	Output Hold Time			1			ns
tWHSL		Write Protect Setup Time			20			ns
tSHWL		Write Protect Hold Time			100			ns
tDP(2)		CS# High to Deep Power-down Mode					10	us
tRES1(2)		CS# High to Standby Mode without Electronic Signature Read					100	us
tRES2(2)		CS# High to Standby Mode with Electronic Signature Read					100	us
tW		Write Status Register Cycle Time				40	100	ms
tBP		Byte-Program				9	300	us
tPP		Page Program Cycle Time				1.4	5	ms
tSE		Sector Erase Cycle Time (4KB)				60	300	ms
tBE		Block Erase Cycle Time (32KB)				0.5	2	s
tBE		Block Erase Cycle Time (64KB)				0.7	2	s

Symbol	Alt.	Parameter	Min.	Typ.	Max.	Unit
tCE		Chip Erase Cycle Time		50	80	s
tWPS		Write Protection Selection Time			1	ms
tWSR		Write Security Register Time			1	ms

Notes:
1. tCH + tCL must be greater than or equal to 1/ fC.
2. Value guaranteed by characterization, not 100% tested in production.
3. Only applicable as a constraint for a WRSR instruction when SRWD is set at 1.

Timing Analysis

Figure 7. Serial Input Timing

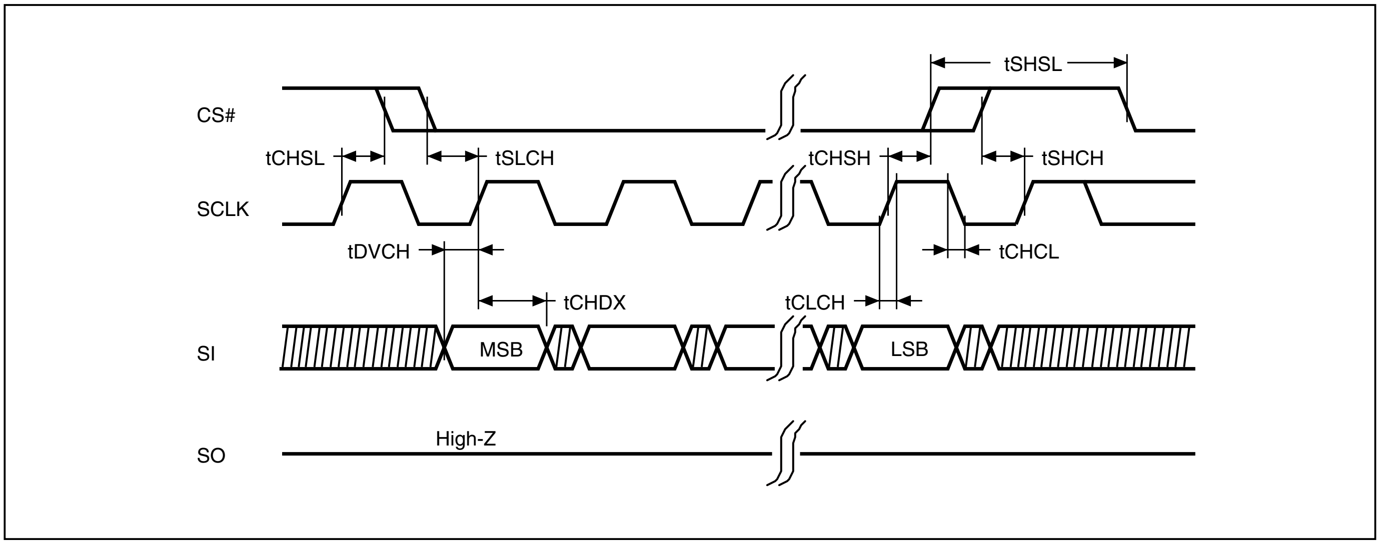


Figure 8. Output Timing

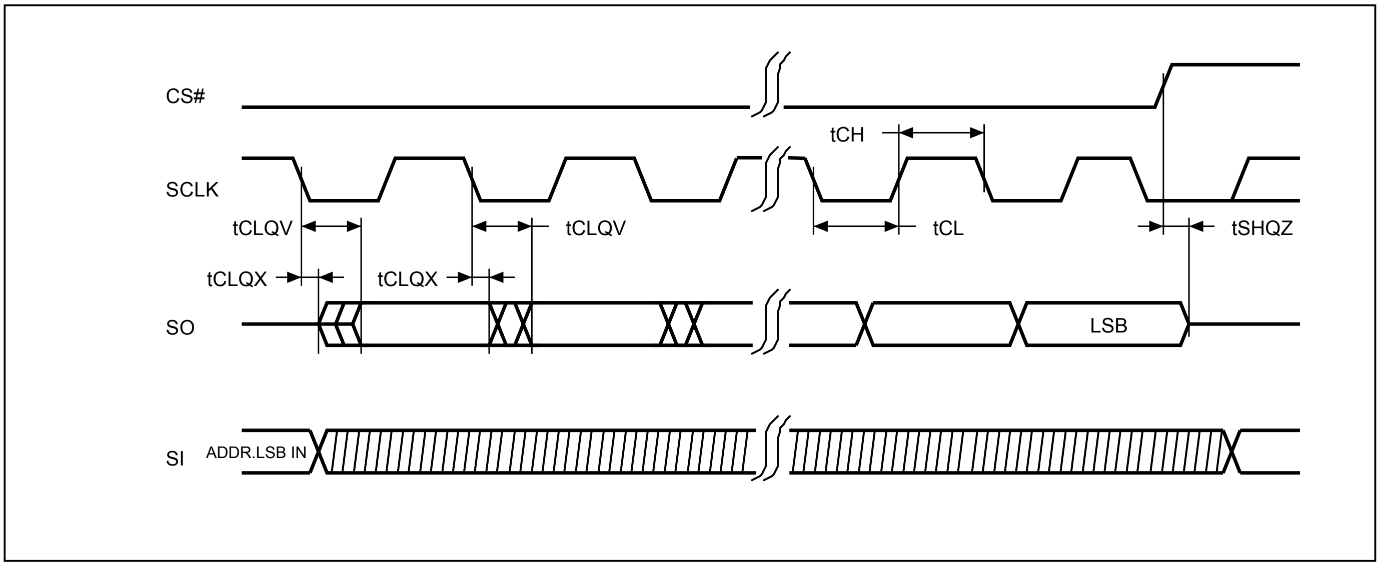


Figure 9. WP# Setup Timing and Hold Timing during WRSR when SRWD=1

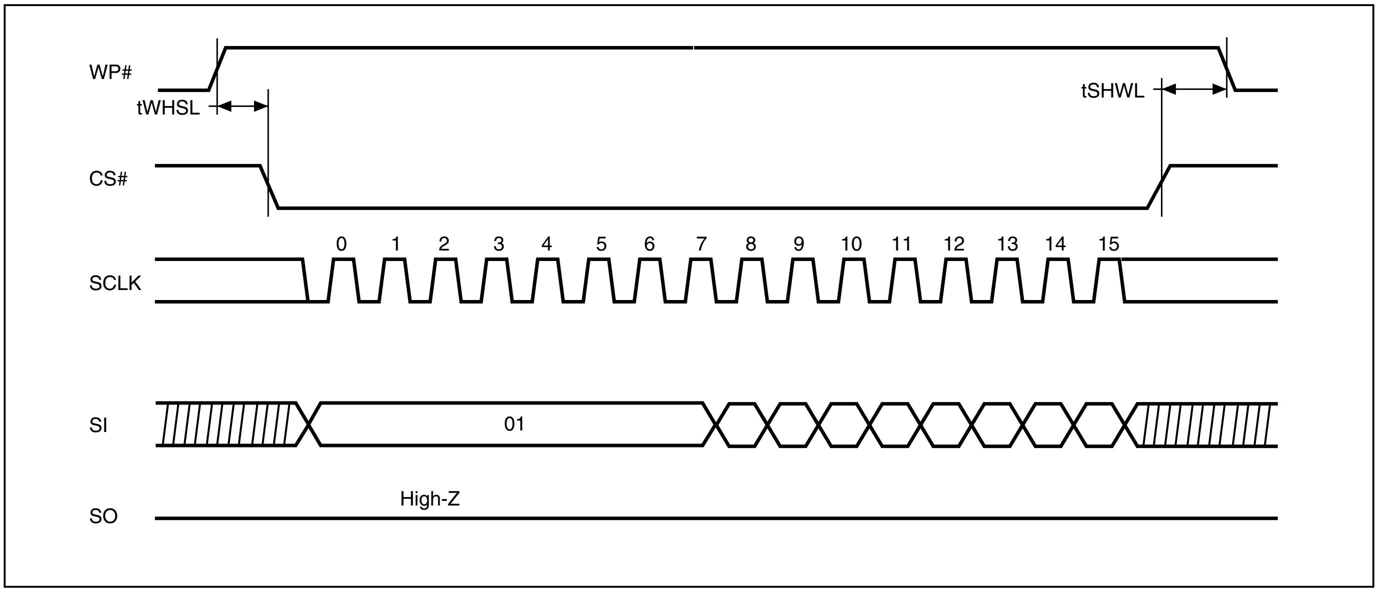


Figure 10. Write Enable (WREN) Sequence (Command 06)

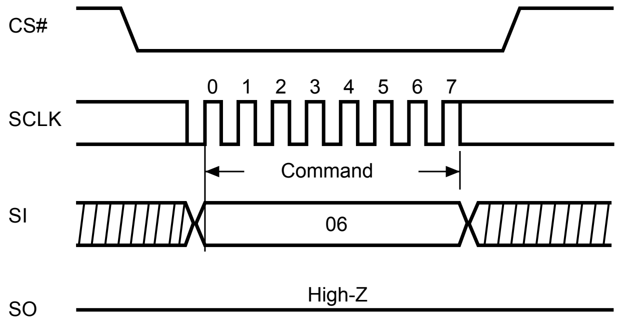


Figure 11. Write Disable (WRDI) Sequence (Command 04)

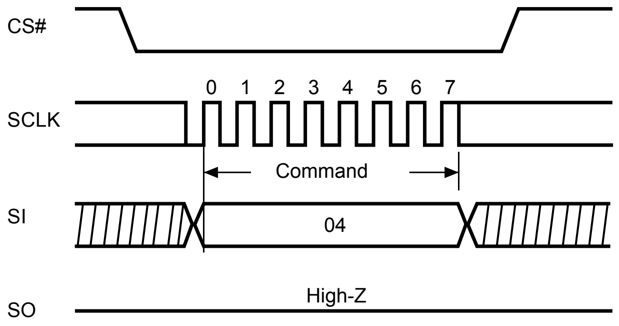


Figure 12. Read Identification (RDID) Sequence (Command 9F)

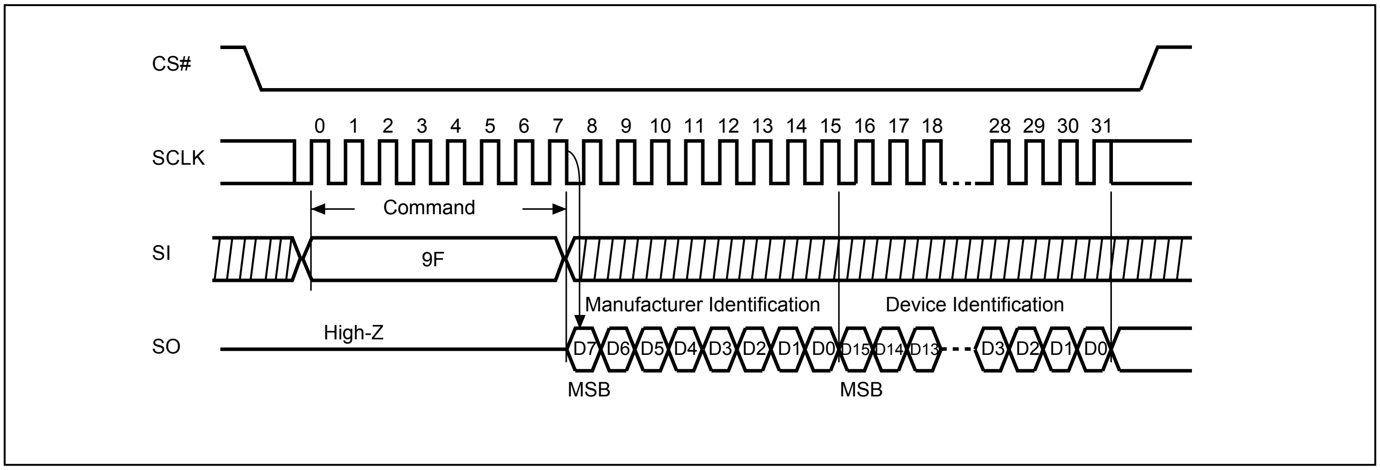


Figure 13. Read Status Register (RDSR) Sequence (Command 05)

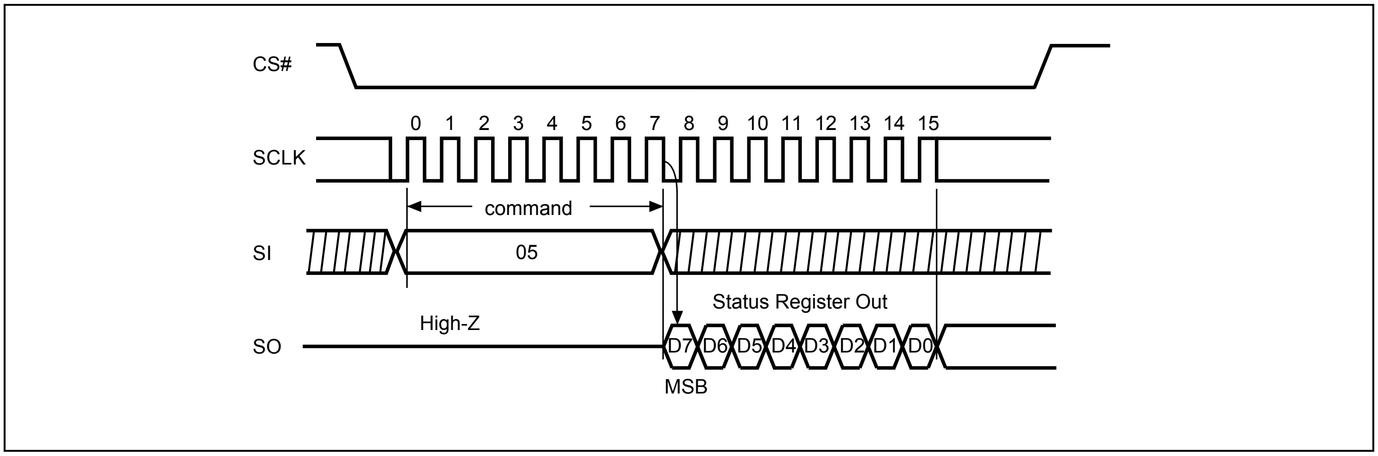


Figure 14. Write Status Register (WRSR) Sequence (Command 01)

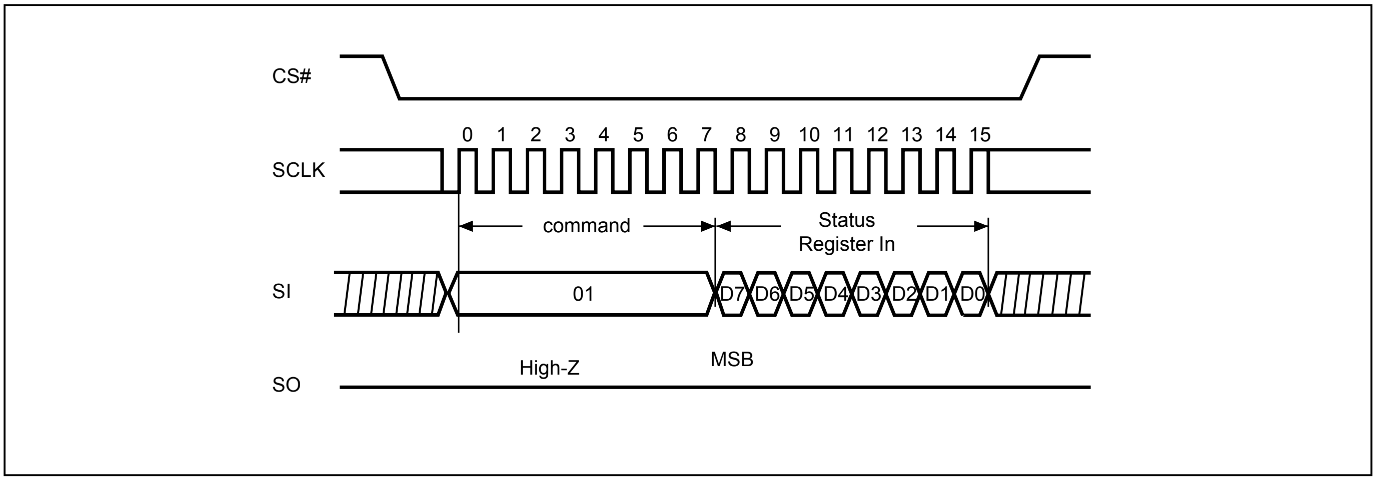


Figure 15. Read Data Bytes (READ) Sequence (Command 03)

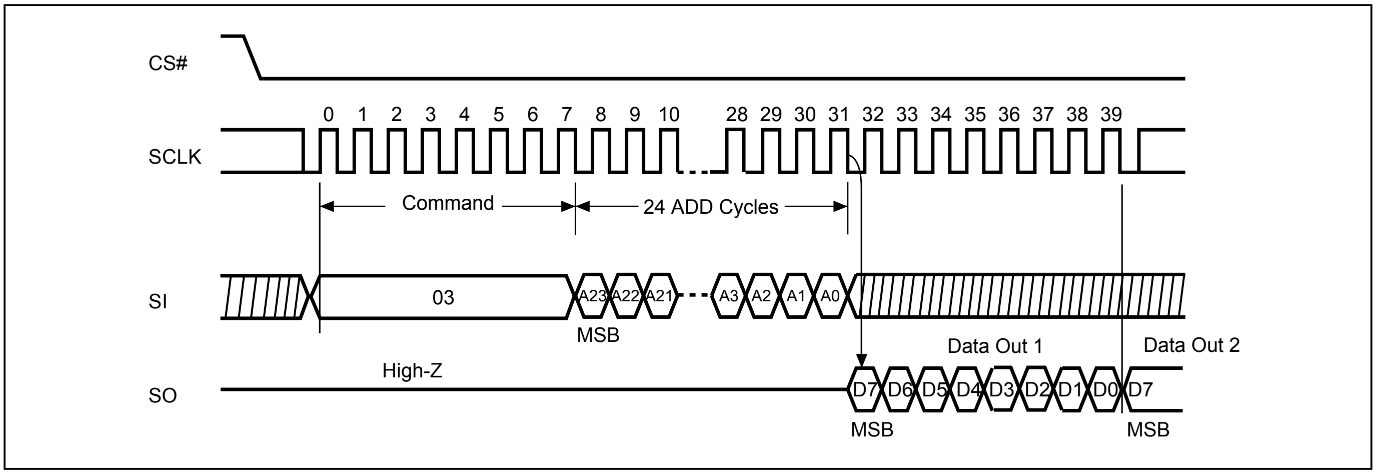


Figure 16. Read at Higher Speed (FAST_READ) Sequence (Command 0B)

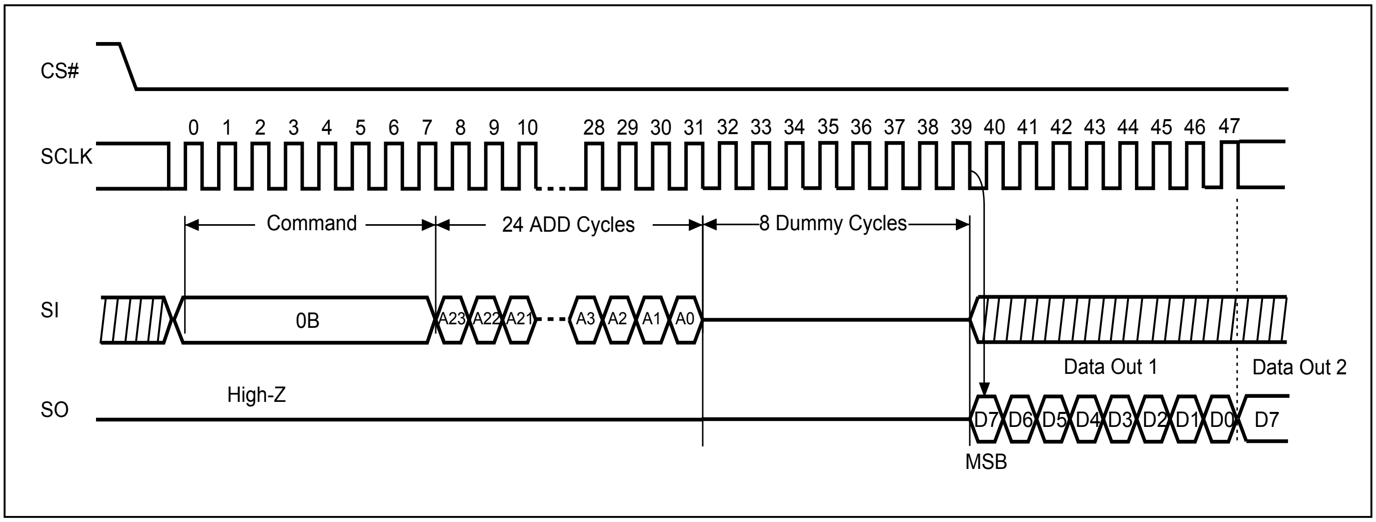


Figure 17. Dual Read Mode Sequence (Command 3B)

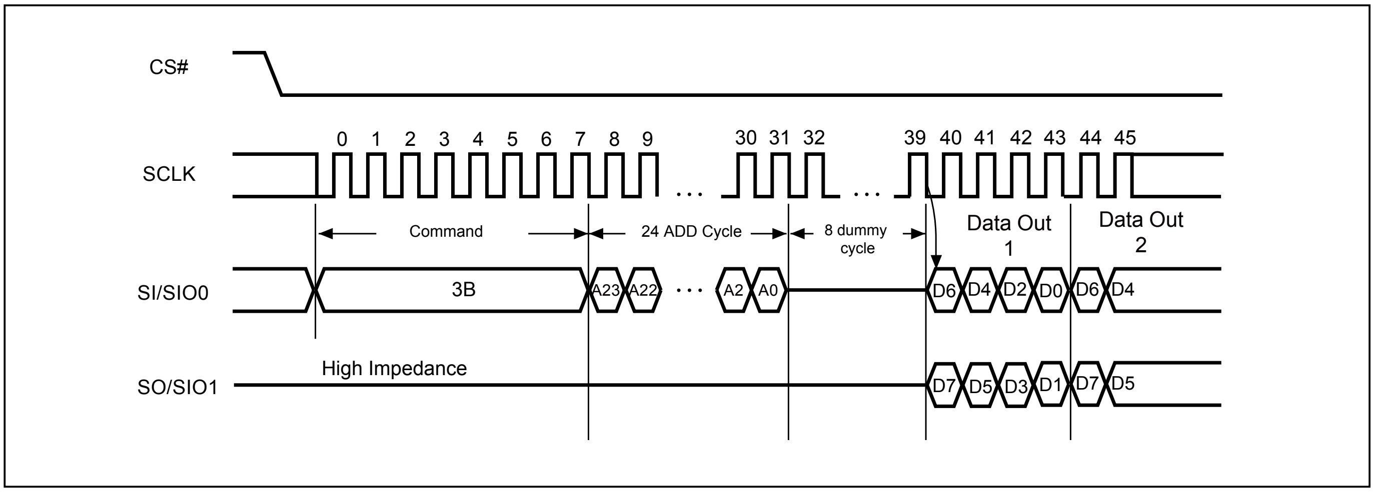


Figure 18. Quad Read Mode Sequence (Command 6B)

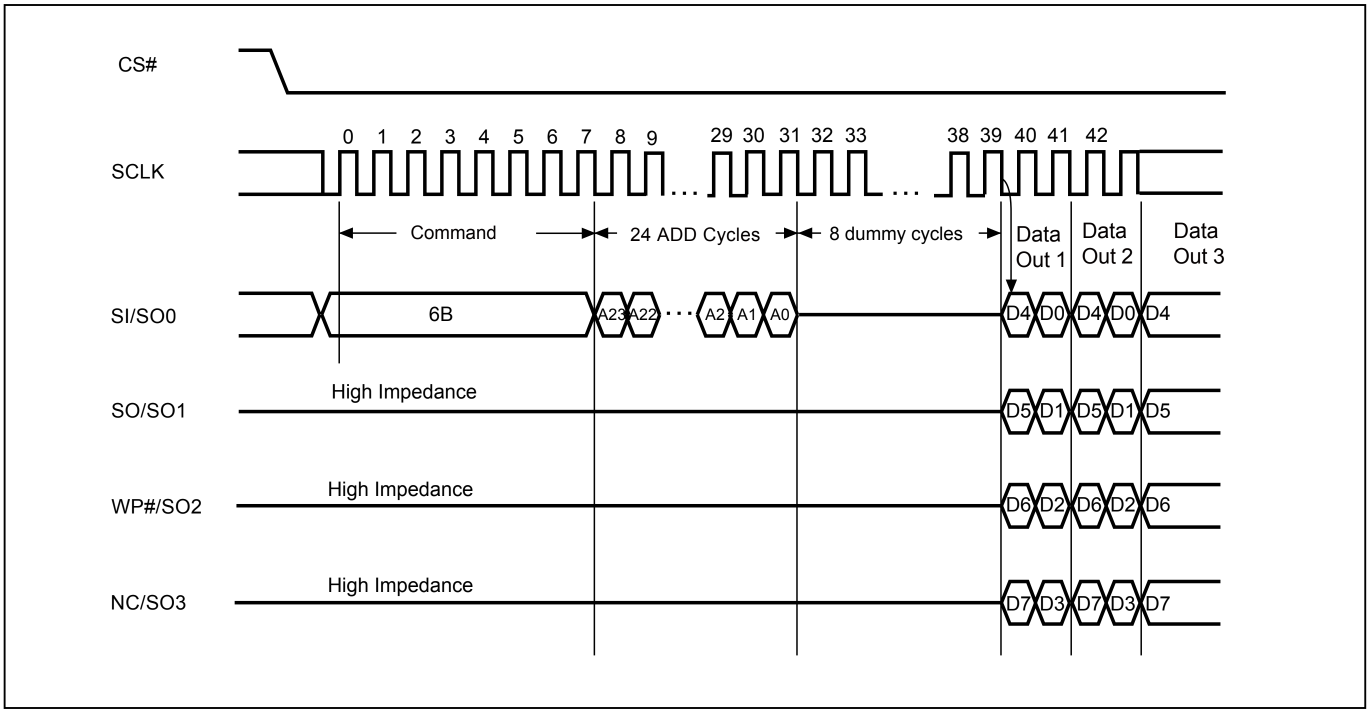


Figure 19. Sector Erase (SE) Sequence (Command 20)

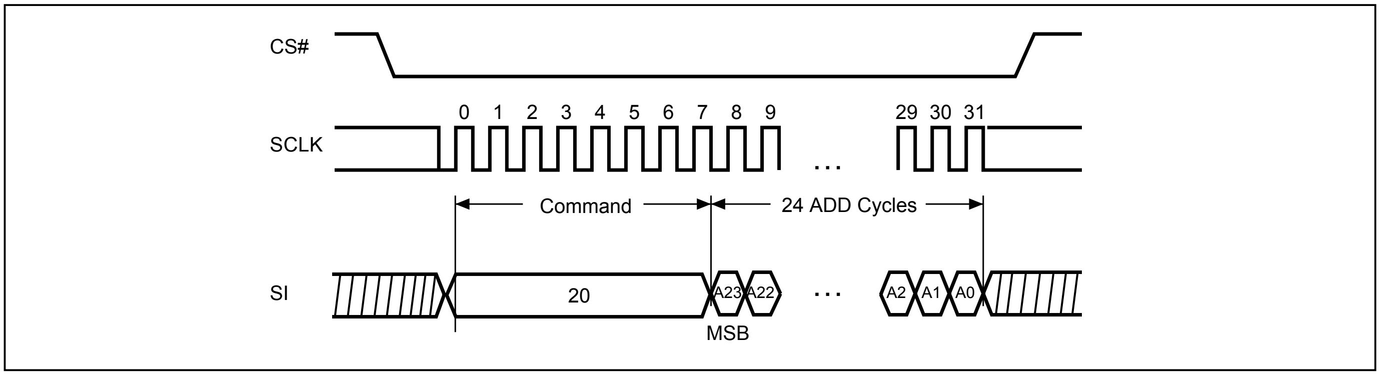


Figure 20. Block Erase (BE/BE32K) Sequence (Command D8/52)

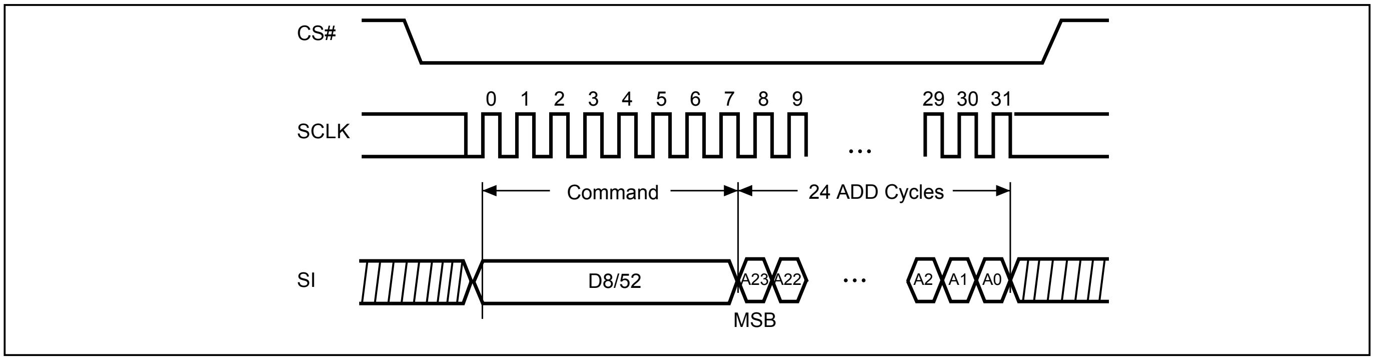


Figure 21. Chip Erase (CE) Sequence (Command 60 or C7)

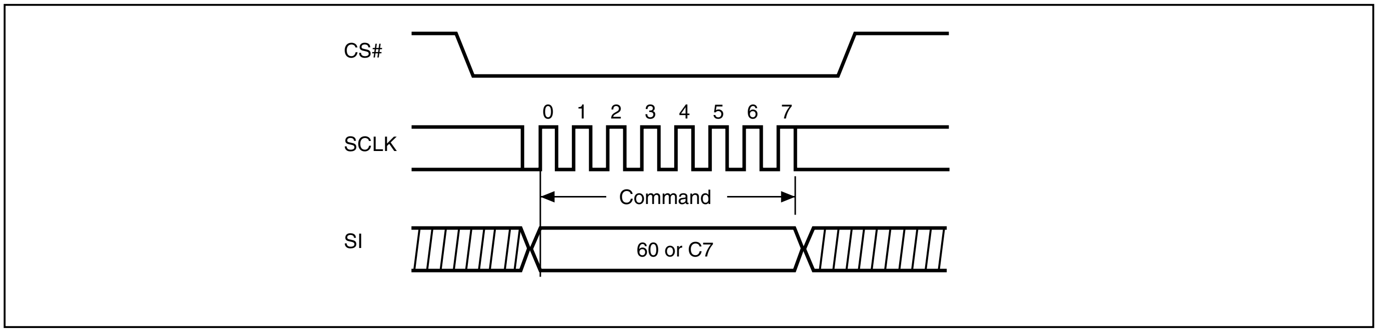


Figure 22. Page Program (PP) Sequence (Command 02)

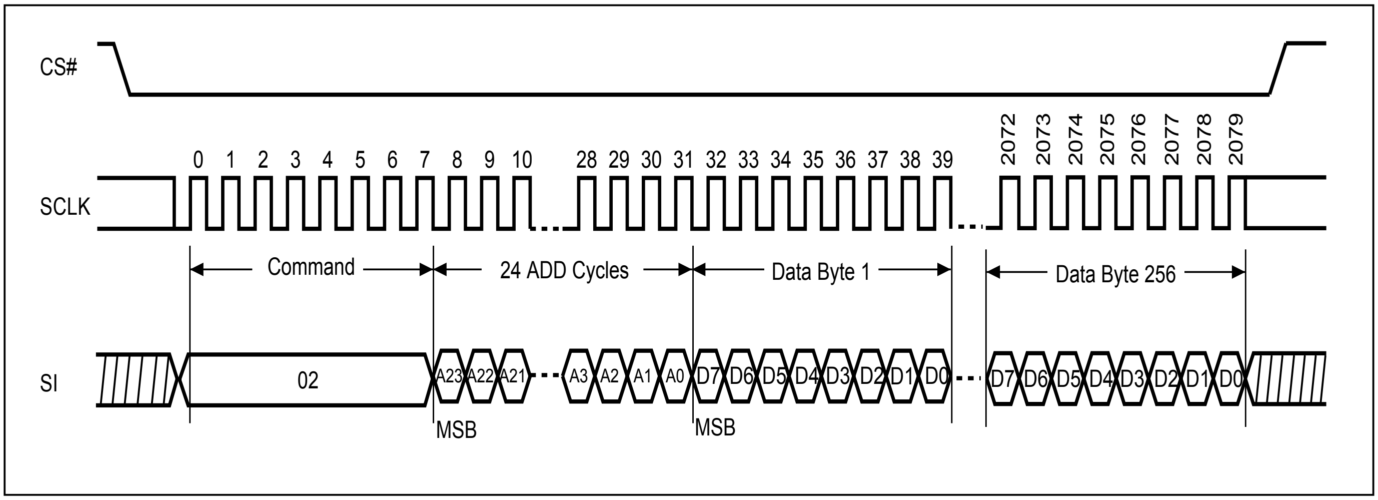


Figure 23. 4 x I/O Page Program (4PP) Sequence (Command 38)

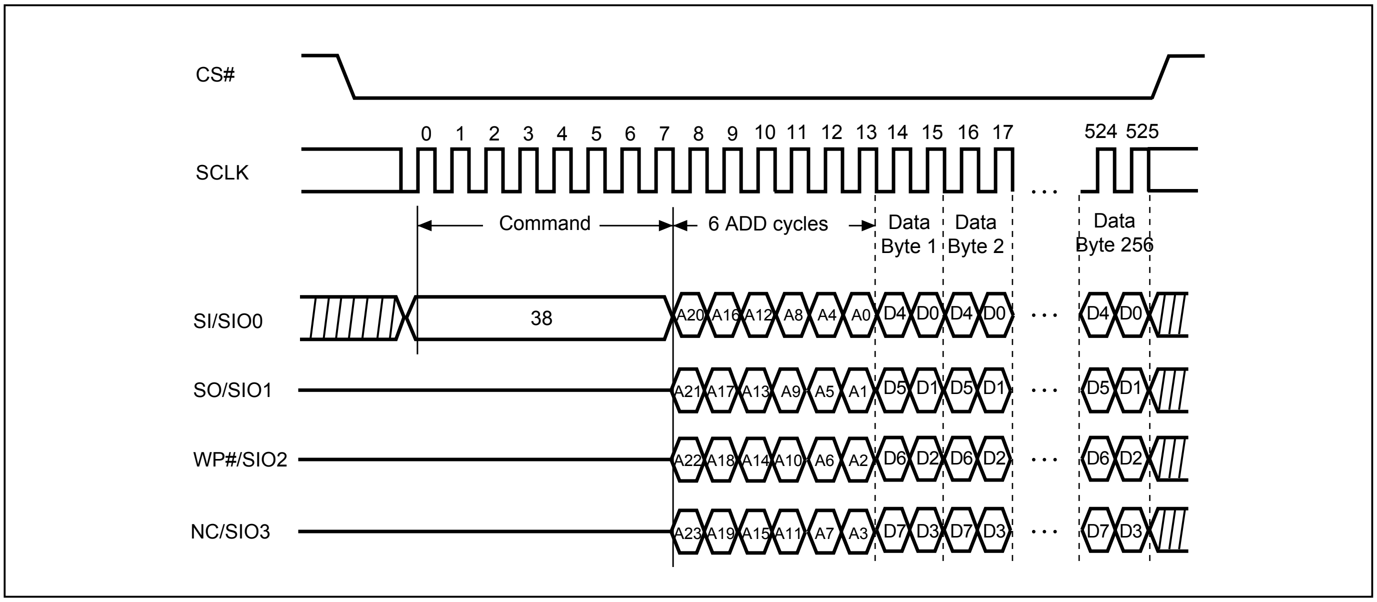
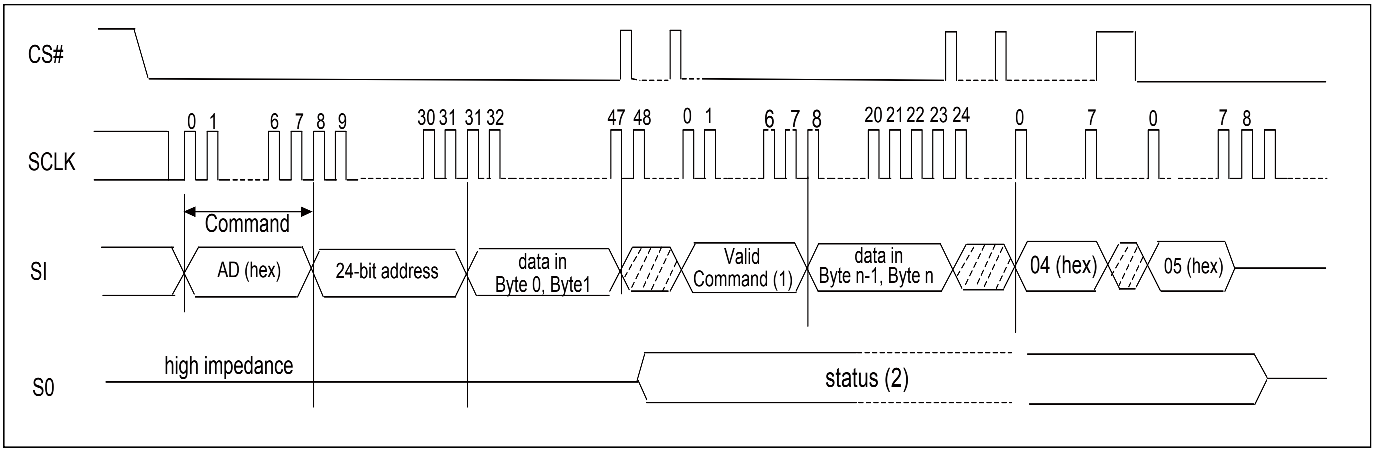


Figure 24. Continously Program (CP) Mode Sequence with Hardware Detection (Command AD)



Notes:

(1) During CP mode, the valid commands are CP command (AD hex), WRDI command (04 hex), RDSR command (05 hex), and RDSCUR command (2B hex).

(2) Once an internal programming operation begins, CS# goes low will drive the status on the SO pin and CS# goes high will return the SO pin to tri-state.

(3) To end the CP mode, either reaching the highest unprotected address or sending Write Disable (WRDI) command (04 hex) may achieve it and then it is recommended to send RDSR command (05 hex) to verify if CP mode is ended.

Figure 25. Deep Power-down (DP) Sequence (Command B9)

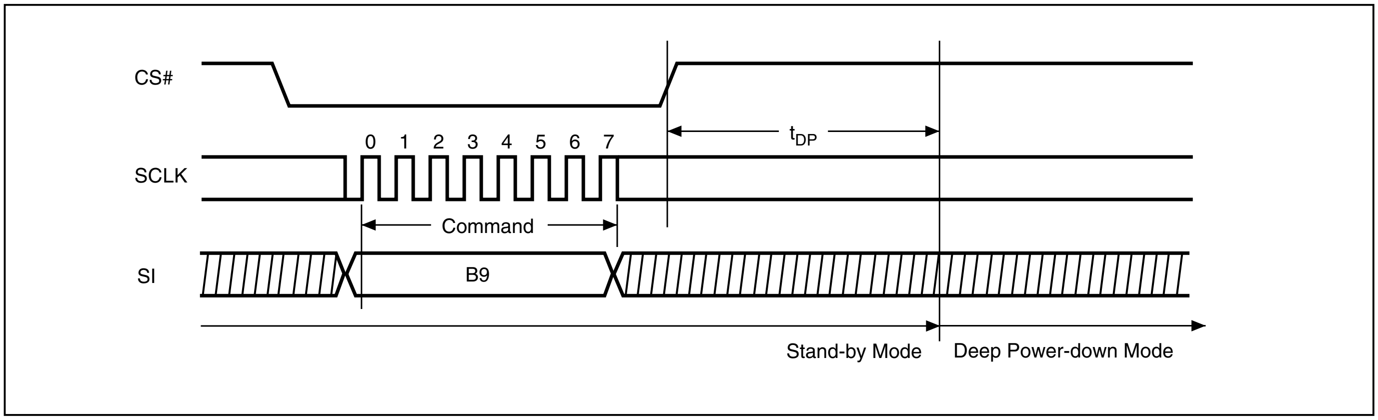


Figure 26. Read Electronic Signature (RES) Sequence (Command AB)

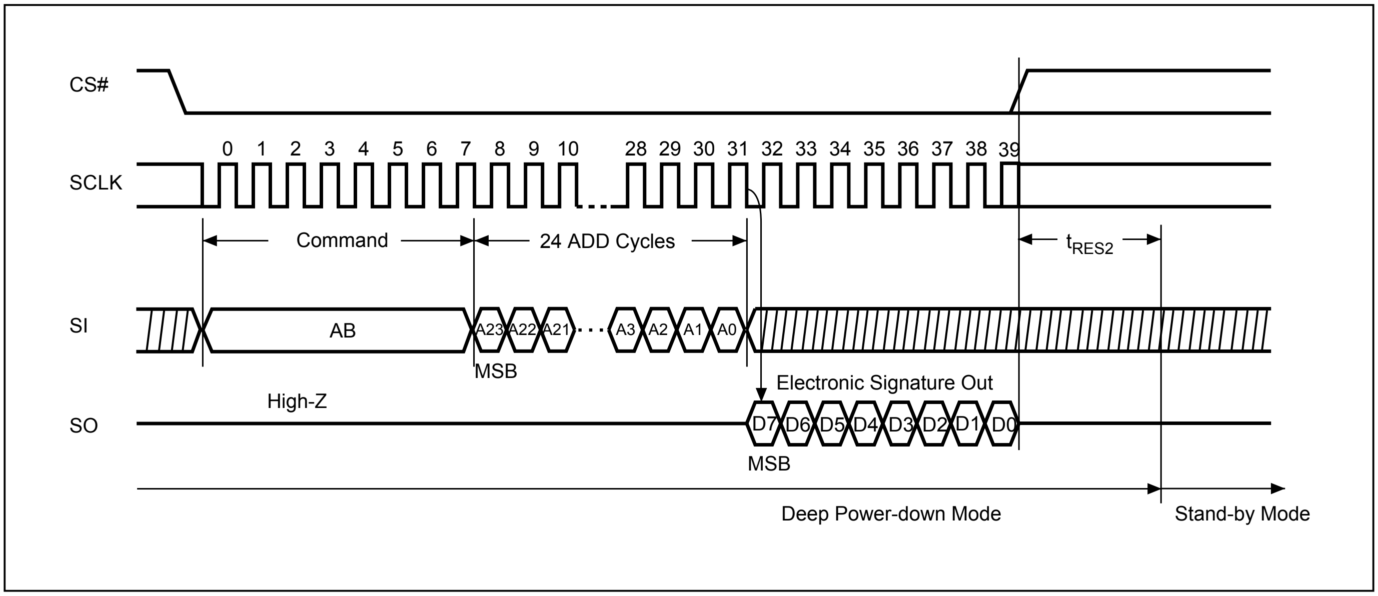


Figure 27. Release from Deep Power-down (RDP) Sequence (Command AB)

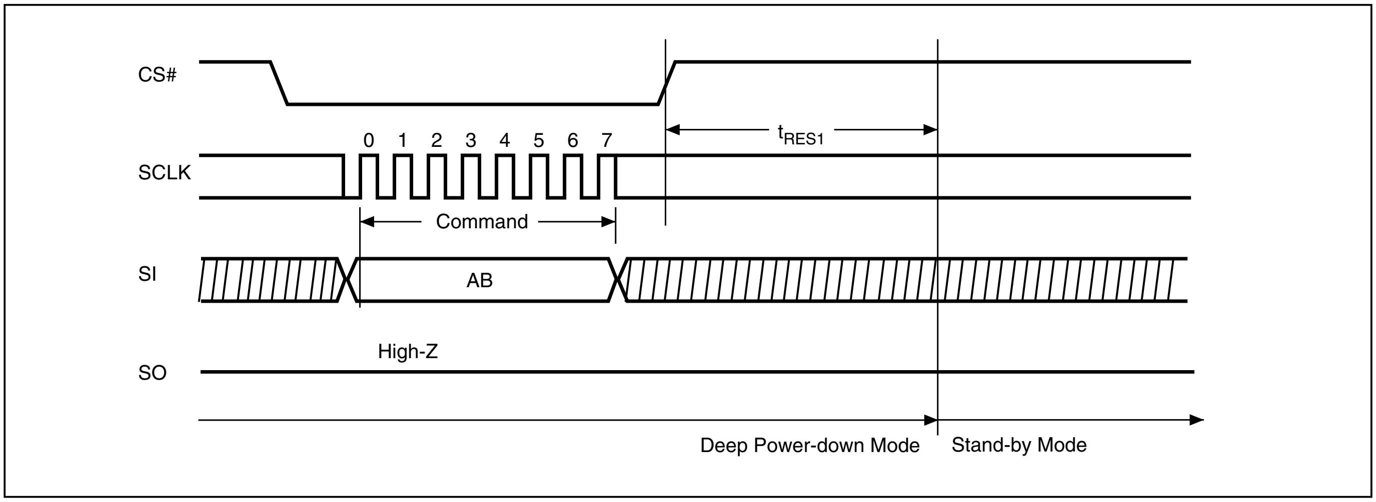
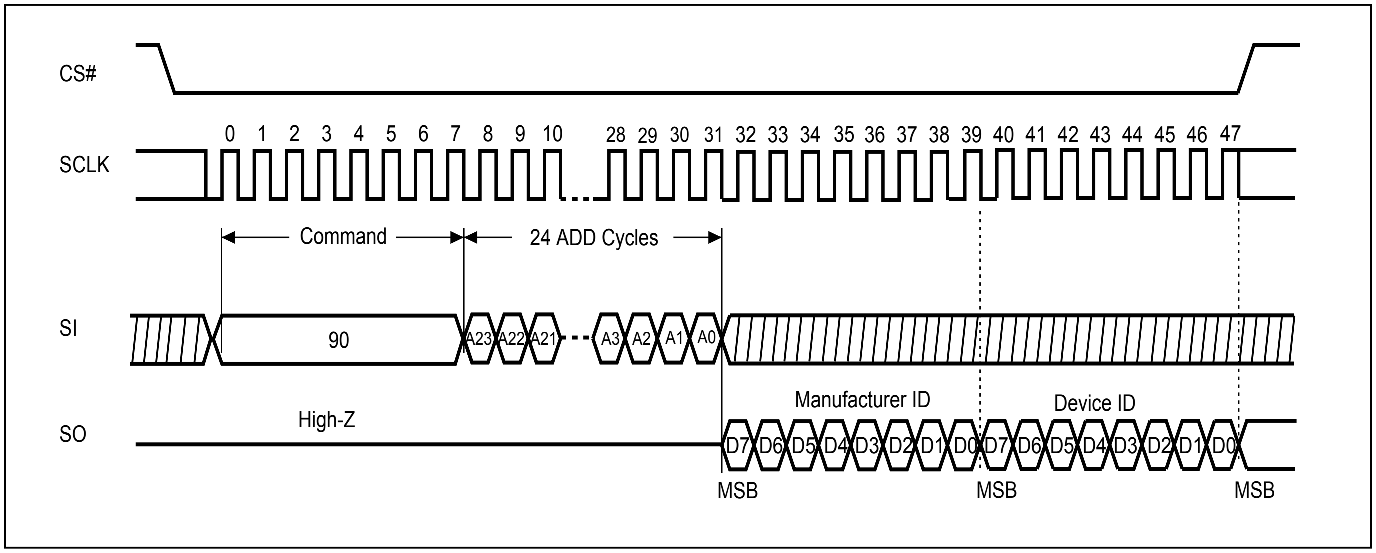


Figure 28. Read Electronic Manufacturer & Device ID (REMS) Sequence (Command 90 or EF or DF)



Notes:

1. A0=0 will output the Manufacturer ID first and A0=1 will output Device ID first. A1~A23 is don't care.
2. Instruction is either 90(hex) or EF(hex) or DF(hex).

Figure 29. Write Protection Selection (WPSEL) Sequence (Command 68)

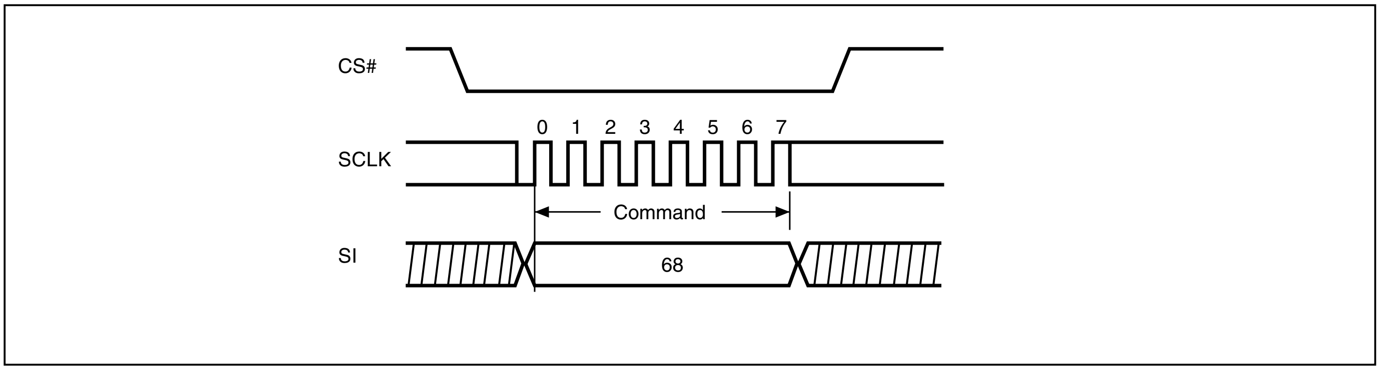


Figure 30. Single Block Lock/Unlock Protection (SBLK/SBULK) Sequence (Command 36/39)

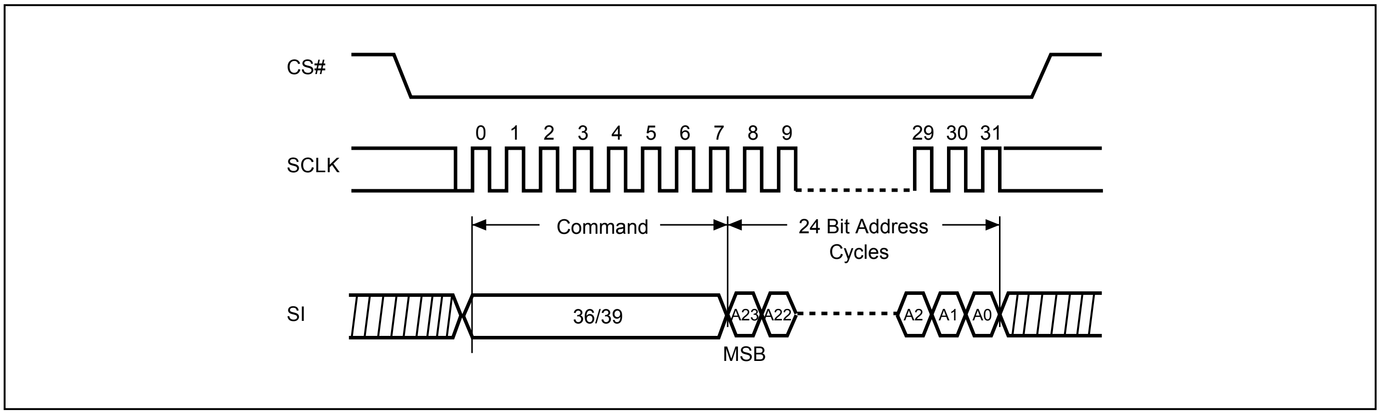


Figure 31. Read Block Protection Lock Status (RDBLOCK) Sequence (Command 3C)

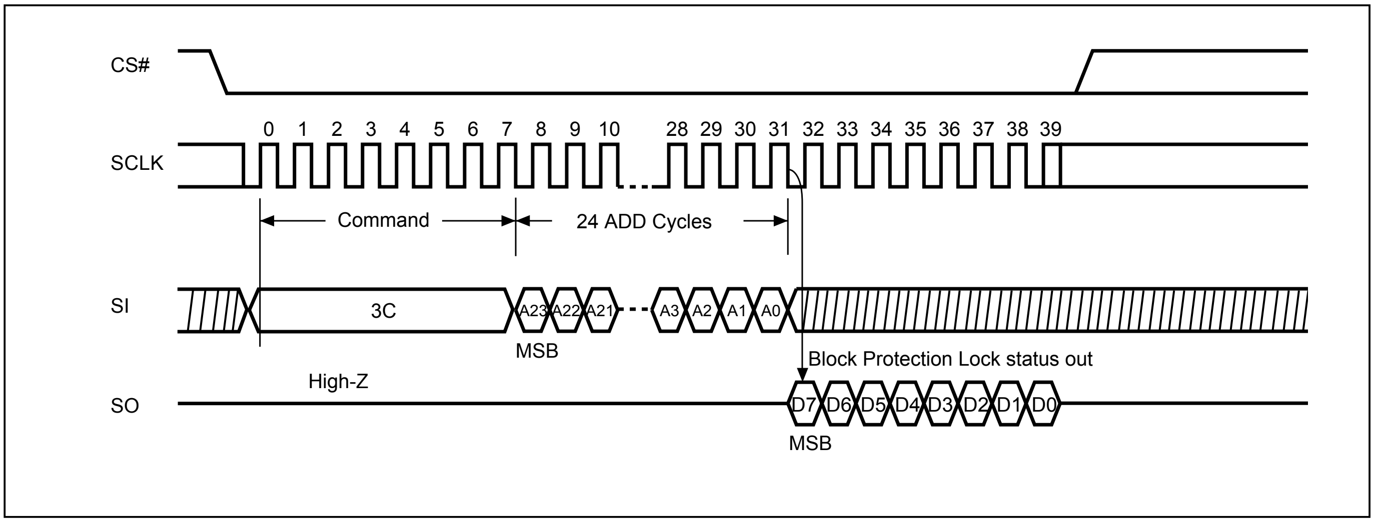


Figure 32. Gang Block Lock/Unlock (GBLK/GBULK) Sequence (Command 7E/98)

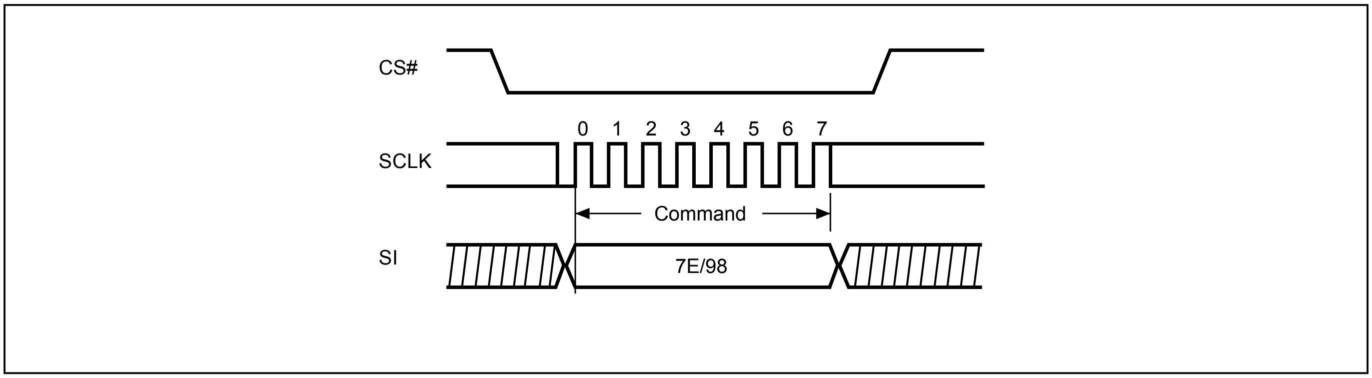
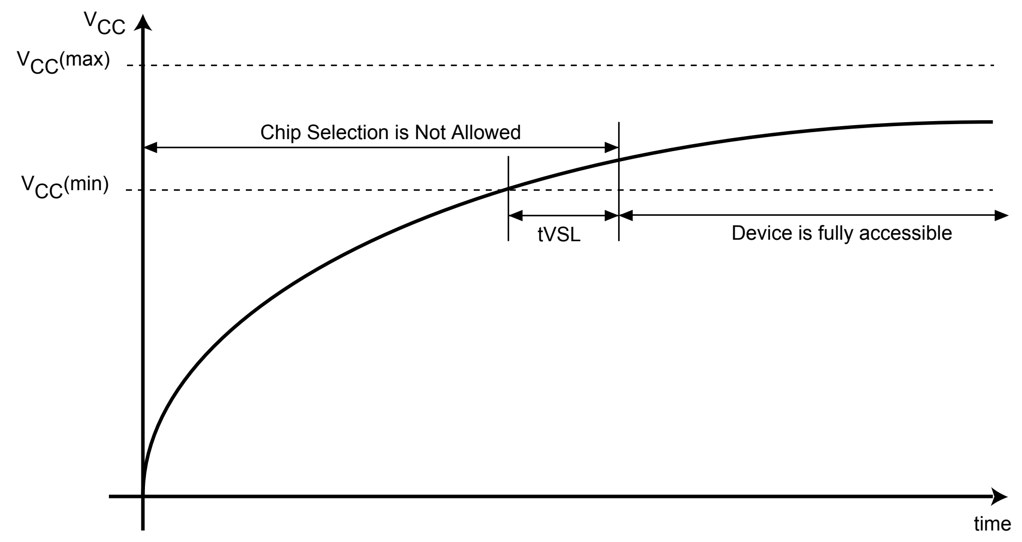


Figure 33. Power-up Timing



Note: VCC (max.) is 3.6V and VCC (min.) is 2.7V.

Table 12. Power-Up Timing

Symbol	Parameter	Min.	Max.	Unit
tVSL(1)	VCC(min) to CS# low	300		us

Note: The parameter is characterized only.

INITIAL DELIVERY STATE

The device is delivered with the memory array erased: all bits are set to 1 (each byte contains FFh). The Status Register contains 00h (all Status Register bits are 0).

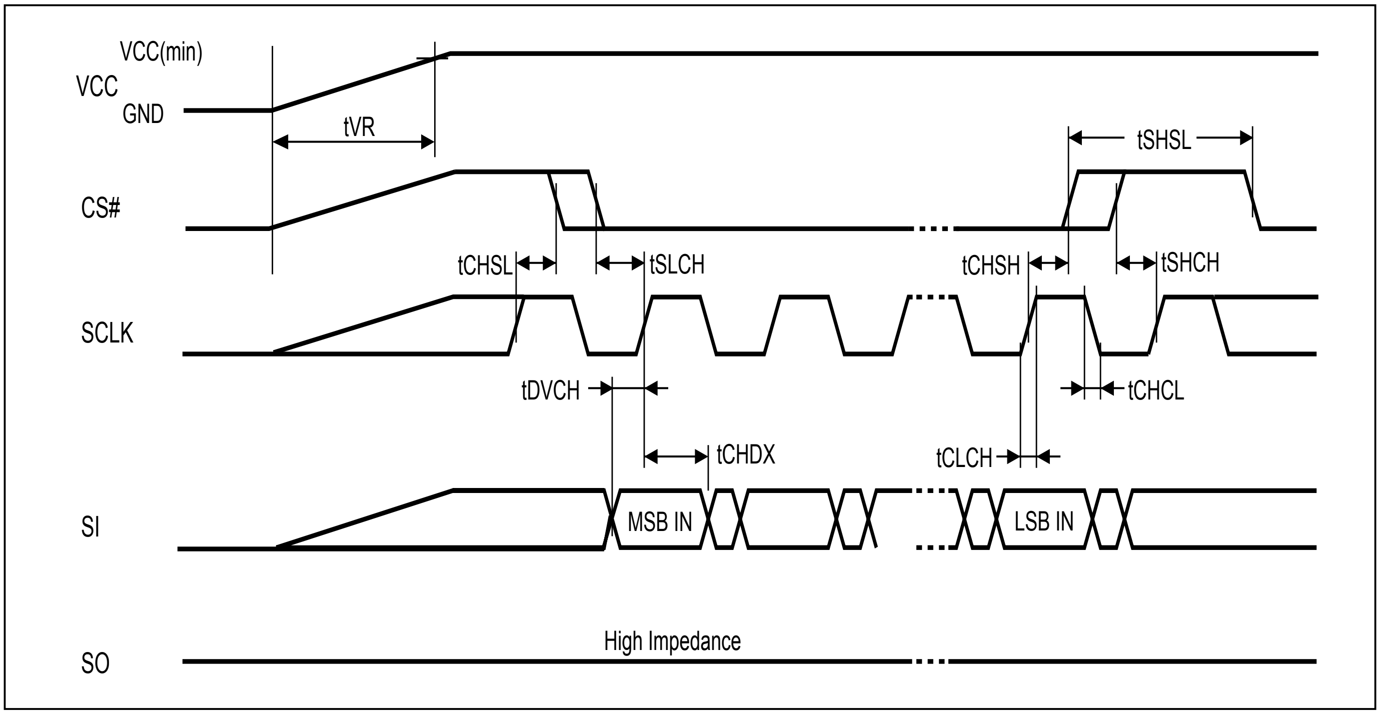
OPERATING CONDITIONS

At Device Power-Up and Power-Down

AC timing illustrated in *Figure 34* and *Figure 35* are for the supply voltages and the control signals at device power-up and power-down. If the timing in the figures is ignored, the device will not operate correctly.

During power-up and power-down, CS# needs to follow the voltage applied on VCC to keep the device not to be selected. The CS# can be driven low when VCC reach Vcc(min.) and wait a period of tVSL.

Figure 34. AC Timing at Device Power-Up

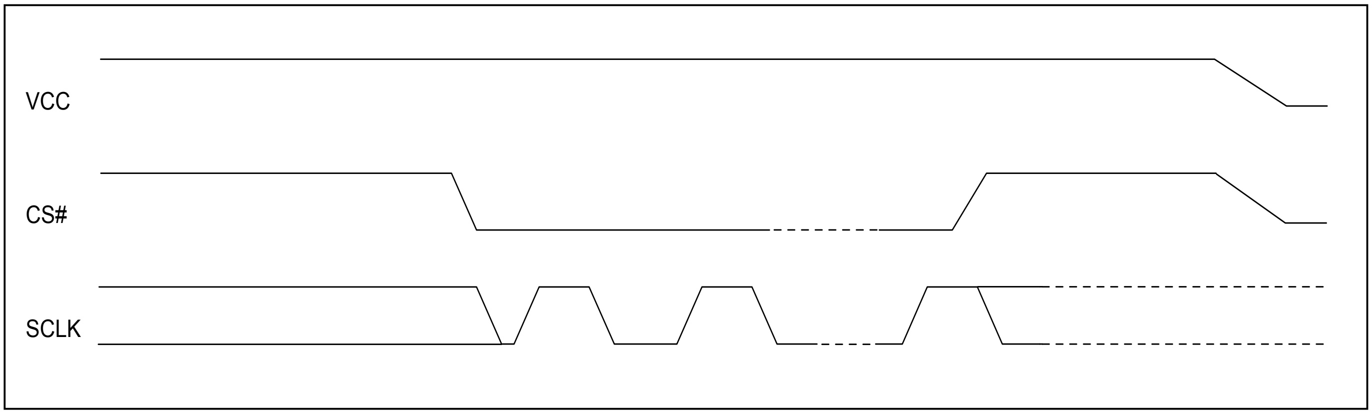


Symbol	Parameter	Notes	Min.	Max.	Unit
tVR	VCC Rise Time	1	20	500000	us/V

Notes :
1. Sampled, not 100% tested.
2. For AC spec tCHSL, tSLCH, tDVCH, tCHDX, tSHSL, tCHSH, tSHCH, tCHCL, tCLCH in the figure, please refer to *"Table 11. AC CHARACTERISTICS"*.

Figure 35. Power-Down Sequence

During power-down, CS# needs to follow the voltage drop on VCC to avoid mis-operation.



ERASE AND PROGRAMMING PERFORMANCE

Parameter	Typ. (1)	Max. (2)	Unit
Write Status Register Cycle Time	40	100	ms
Sector Erase Time (4KB)	60	300	ms
Block Erase Time (64KB)	0.7	2	s
Block Erase Time (32KB)	0.5	2	s
Chip Erase Time	50	80	s
Byte Program Time (via page program command)	9	300	us
Page Program Time	1.4	5	ms
Erase/Program Cycle	100,000		cycles

Notes:

1. Typical program and erase time assumes the following conditions: 25°C, 3.3V, and checker board pattern.
2. Under worst conditions of 85°C and 2.7V.
3. System-level overhead is the time required to execute the first-bus-cycle sequence for the programming command.

DATA RETENTION

Parameter	Condition	Min.	Max.	Unit
Data retention	55˚C	20		years

LATCH-UP CHARACTERISTICS

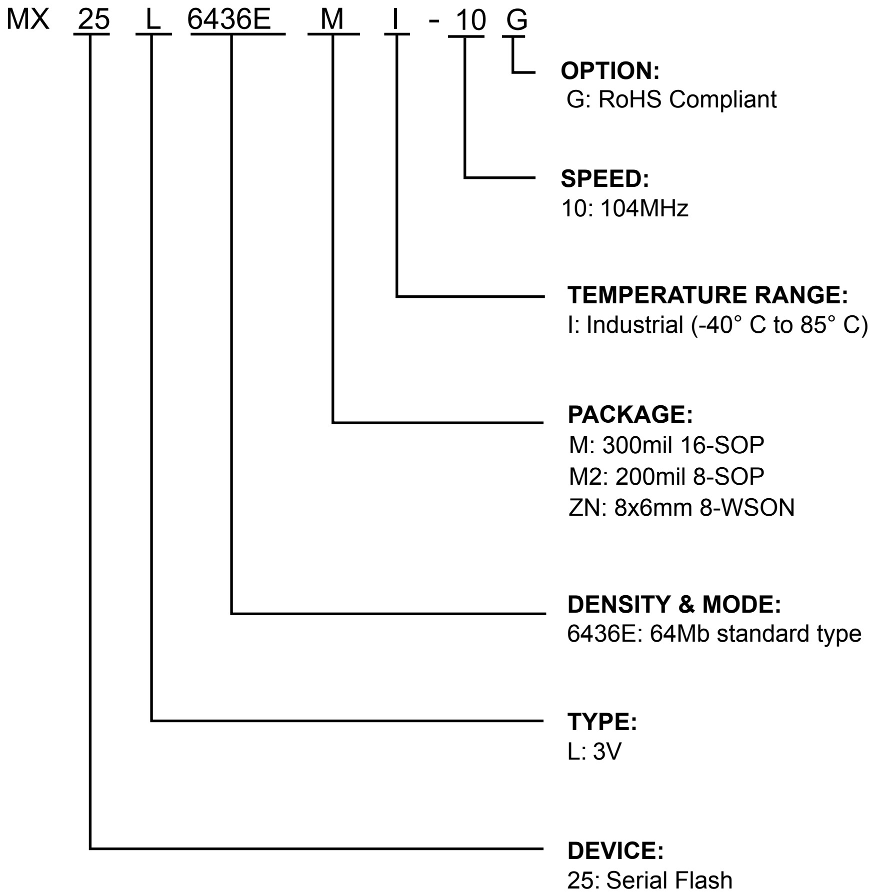
	Min.	Max.
Input Voltage with respect to GND on all power pins, SI, CS#	-1.0V	2 VCCmax
Input Voltage with respect to GND on SO	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

ORDERING INFORMATION

PART NO.	CLOCK (MHz)	TEMPERATURE	PACKAGE	Remark
MX25L6436EMI-10G*	104	-40°C~85°C	16-SOP (300mil)	RoHS Compliant
MX25L6436EM2I-10G	104	-40°C~85°C	8-SOP (200mil)	RoHS Compliant
MX25L6436EZNI-10G*	104	-40°C~85°C	8-WSON (8x6mm)	RoHS Compliant

* Advanced Information

PART NAME DESCRIPTION



MX 25 L 6436E M I - 10 G

OPTION:
G: RoHS Compliant

SPEED:
10: 104MHz

TEMPERATURE RANGE:
I: Industrial (-40° C to 85° C)

PACKAGE:
M: 300mil 16-SOP
M2: 200mil 8-SOP
ZN: 8x6mm 8-WSON

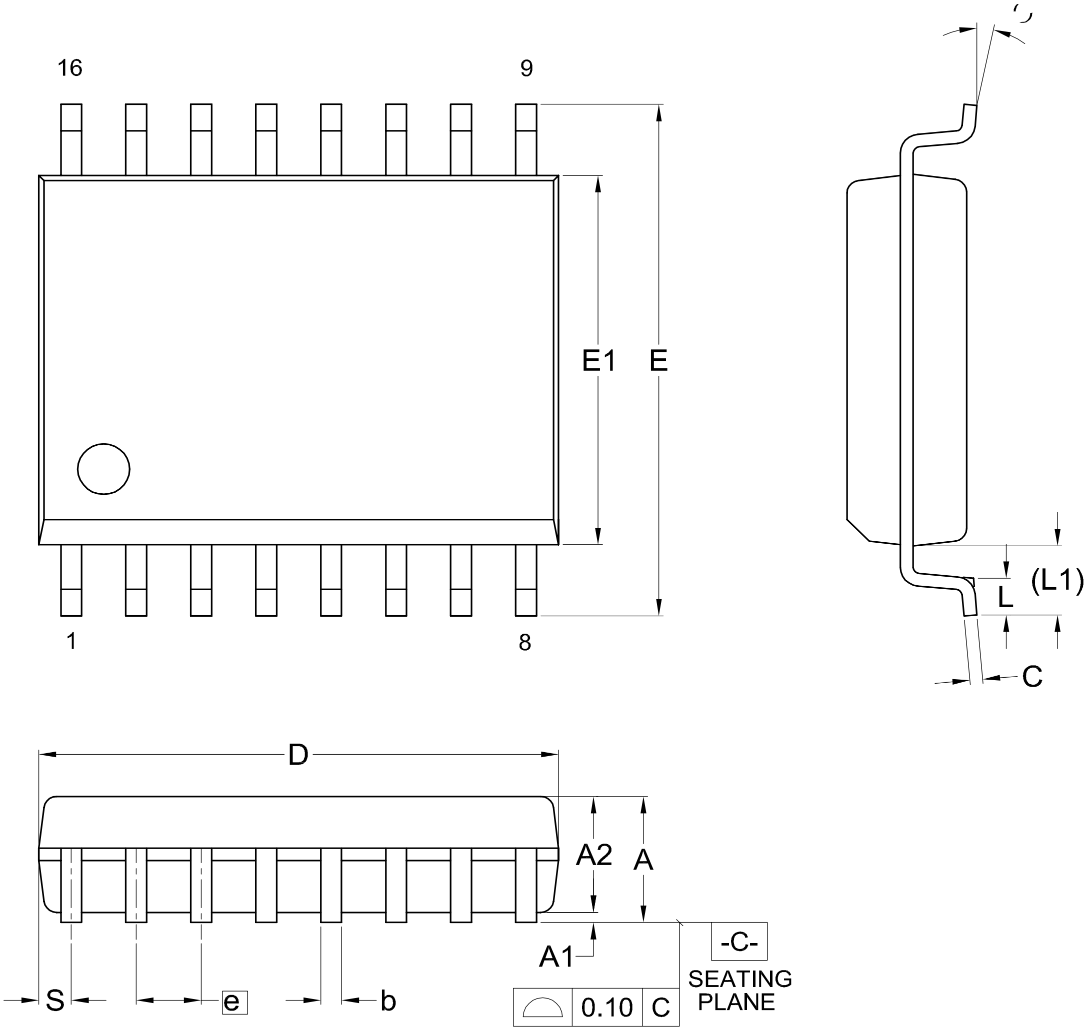
DENSITY & MODE:
6436E: 64Mb standard type

TYPE:
L: 3V

DEVICE:
25: Serial Flash

PACKAGE INFORMATION

Doc. Title: Package Outline for SOP 16L (300MIL)

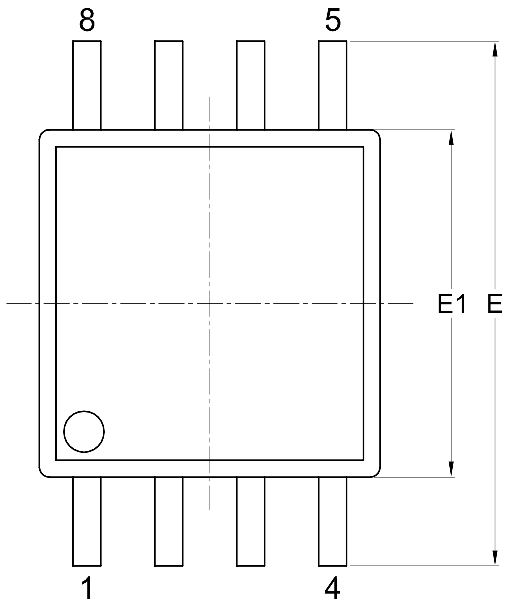


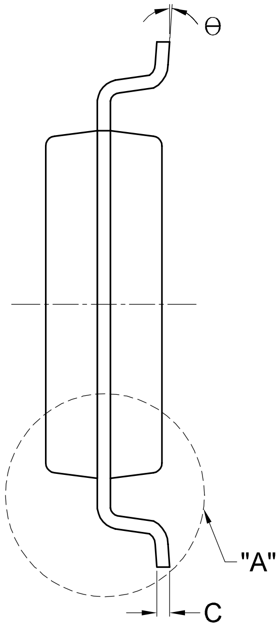
Dimensions (inch dimensions are derived from the original mm dimensions)

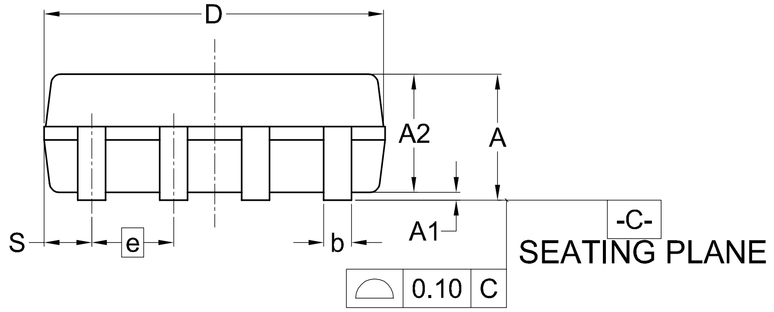
SYMBOL UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	**Min.**	---	0.10	2.34	0.36	0.20	10.10	10.10	7.42	---	0.40	1.31	0.51	0
	Nom.	---	0.20	2.39	0.41	0.25	10.30	10.30	7.52	1.27	0.84	1.44	0.64	5
	Max.	2.65	0.30	2.44	0.51	0.30	10.50	10.50	7.60	---	1.27	1.57	0.77	8
Inch	**Min.**	---	0.004	0.092	0.014	0.008	0.397	0.397	0.292	---	0.016	0.052	0.020	0
	Nom.	---	0.008	0.094	0.016	0.010	0.405	0.405	0.296	0.050	0.033	0.057	0.025	5
	Max.	0.104	0.012	0.096	0.020	0.012	0.413	0.413	0.299	---	0.050	0.062	0.030	8

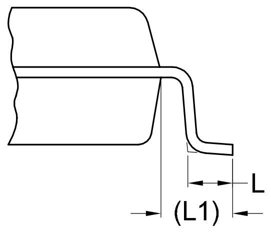
Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1402	10	MS-013			

Doc. Title: Package Outline for SOP 8L 200MIL (official name - 209MIL)









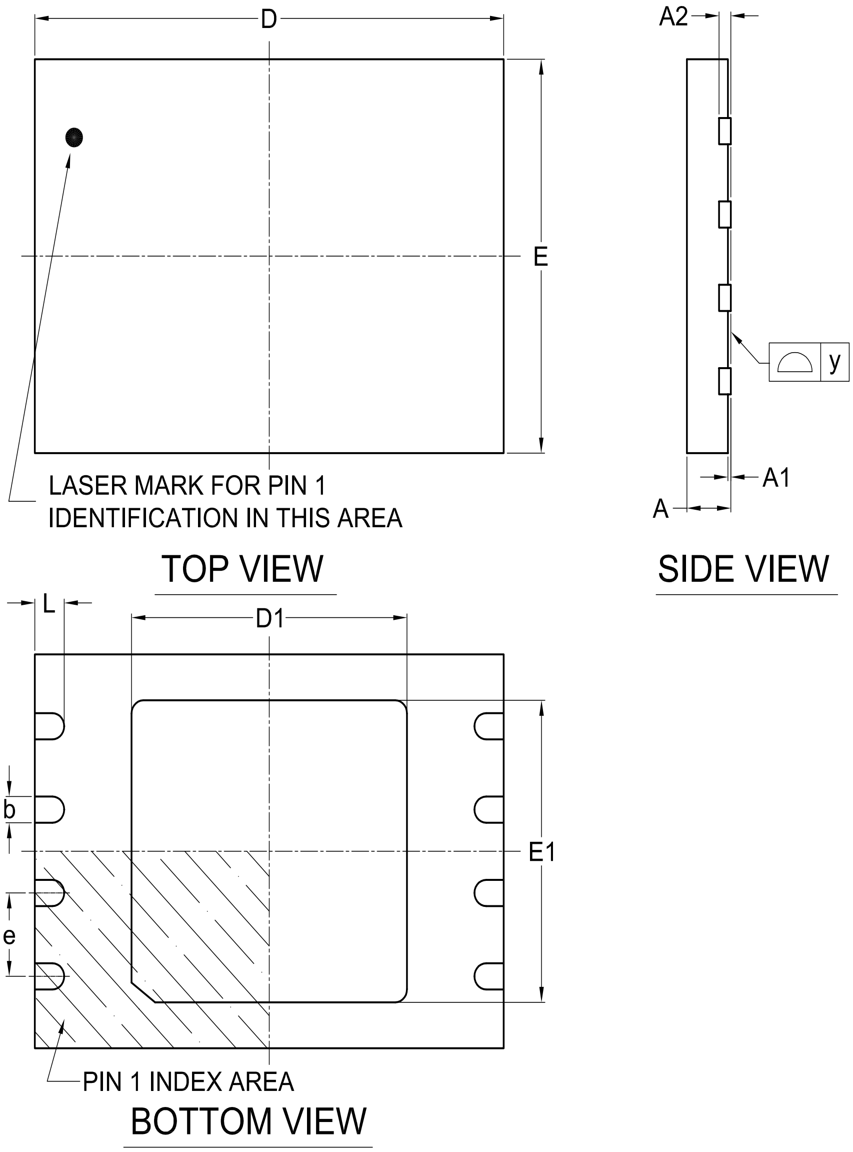
DETAIL "A"

Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.05	1.70	0.36	0.19	5.13	7.70	5.18	---	0.50	1.21	0.62	0
	Nom.	---	0.15	1.80	0.41	0.20	5.23	7.90	5.28	1.27	0.65	1.31	0.74	5
	Max.	2.16	0.20	1.91	0.51	0.25	5.33	8.10	5.38	---	0.80	1.41	0.88	8
Inch	Min.	---	0.002	0.067	0.014	0.007	0.202	0.303	0.204	---	0.020	0.048	0.024	0
	Nom.	---	0.006	0.071	0.016	0.008	0.206	0.311	0.208	0.050	0.026	0.052	0.029	5
	Max.	0.085	0.008	0.075	0.020	0.010	0.210	0.319	0.212	---	0.031	0.056	0.035	8

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-1406	3				

Doc. Title: Package Outline for WSON 8L (8x6x0.8MM, LEAD PITCH 1.27MM)



Dimensions (inch dimensions are derived from the original mm dimensions)
*1 : This package has exposed metal pad underneath the package , it can't contact to metal trace or pad on board.
*2 : The exposed pad size must not violate the min. metal separtion requirement, 0.2mm with terminals.

UNIT \ SYMBOL		A	A1	A2	b	D	D1	E	E1	L	e	y
mm	Min.	0.70	---	---	0.35	7.90	4.60	5.90	4.50	0.40	---	0.00
	Nom.	---	---	0.20	0.40	8.00	4.70	6.00	4.60	0.50	1.27	---
	Max.	0.80	0.05	---	0.48	8.10	4.80	6.10	4.70	0.60	---	0.08
Inch	Min.	0.028	---	---	0.014	0.311	0.181	0.232	0.177	0.016	---	0.00
	Nom.	---	---	0.008	0.016	0.315	0.185	0.236	0.181	0.020	0.05	---
	Max.	0.032	0.002	---	0.019	0.319	0.189	0.240	0.185	0.024	---	0.003

Dwg. No.	Revision	Reference			
		JEDEC	EIAJ		
6110-3402	7	MO-220			

REVISION HISTORY

Revision No.	Description	Page	Date
1.1	1. Added 64Mb general feature description.	P5	NOV/18/2009
	2. Aligned pin name.	P7,10,18,19, P23,48,50	
	3. Update dummy cycle at 2 x I/O, 4 x I/O read mode.	P5	
	4. Rename CFI to DMC.	P6,14,16,36	
	5. Added DMC contents.	P36~38	
	6. Revised Address 19 Data.	P37	
	7. Revised Address 09 Data.	P38	
1.2	1. Added 8-WSON package information	P6,8,63,64,67	APR/15/2010
	2. Separated power consumption by I/O number	P5,42,43	
	3. Modified tSLCH & tSHCH from 8ns to 5ns	P44,45	
	4. Modified Figure 6. Output Timing	P47	
	5. Modified Discoverable Memory Capabilities (DMC) table & note	P36,38	
	6. Modified Figure 33	P61	
	7. Added Figure 34	P62	
	8. Modified Ordering Information	P64	
1.3	1. Removed DMC descriptions	P6,14,16, P36-38	JUL/06/2010
1.4	1. Removed Advanced Information from MX25L12836EZNI-10G	P61	NOV/18/2010
1.5	1. Modified Parameters for tCHDX in Table 8-1	P41	JAN/27/2011
	2. Modified Serial Parameters for tCHDX in Table 8-2	P42	
1.6	1. Removed MX25L12836E information from the previous combined version of MX25L6436E/MX25L12836E	All	OCT/20/2011
	2. Modified Input Capacitance	P36	
	3. Modified tCLQX	P39	
1.7	1. Corrected the REMS descriptions	P26,27,50	NOV/23/2011
1.8	1. Modified Figure 35. Power-Down Sequence	P60	DEC/26/2011
	2. Added Read SFDP (RDSFDP) Mode	P6,13,14, P35~40	
	3. Changed ordering information format	P62	
1.9	1. Modified QREAD Frequency from 70MHz to 75MHz	P5,7,44,45	APR/30/2012
	2. Modified SFDP wording	P35~40	
2.0	1. Revised SFDP table.	P37	AUG/02/2012

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