ADVANCE INFORMATION

MX26C2000B

2M-BIT [256K x 8] CMOS MULTIPLE-TIME-PROGRAMMABLE-EPROM

FEATURES

- 256Kx 8 organization
- Single +5V power supply
- +12V programming voltage
- Fast access time:90/100/120/150 ns
- Totally static operation
- Completely TTL compatible
- Operating current:30mA
- Standby current: 100uA
- Chip erase time: 1 (typ.)
- Chip program time: 12.5 (typ.)
- 50 minimum erase/program cycles
- Typical fast programming cycle duration 10us/byte
- Package type:
  - 32 pin plastic DIP
  - 32 pin PLCC
  - 32 pin TSOP
  - 32 pin SOP

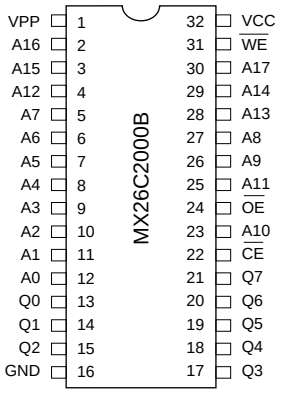
GENERAL DESCRIPTION

The MX26C2000B is a 5V only, 2M-bit, MTP EPROM™ (Multiple Time Programmable Read Only Memory). It is organized as 256K words by 8 bits per word, operates from a single + 5 volt supply, has a static standby mode, and features fast single address location programming. All programming signals are TTL levels, requiring a single pulse. It is design to be programmed and erased by an EPROM programmer or on-board. The MX26C2000B supports a intelligent fast programming algorithm which can result in programming time of less than one minute.

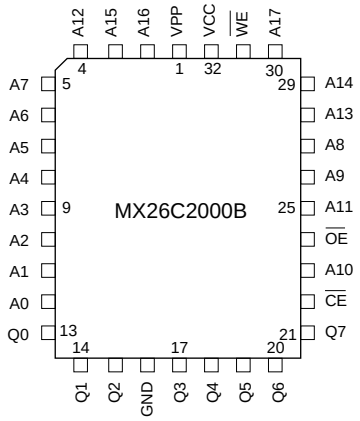
This MTP EPROM™ is packaged in industry standard 32 pin dual-in-line packages, 32 lead PLCC, 32 lead SOP and 32 lead TSOP packages.

PIN CONFIGURATIONS

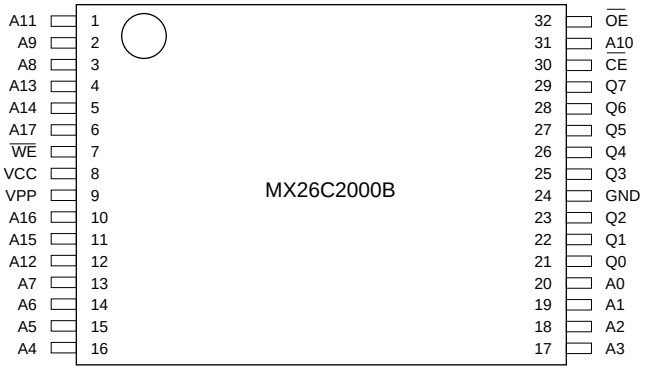
32 PDIP/SOP



32 PLCC



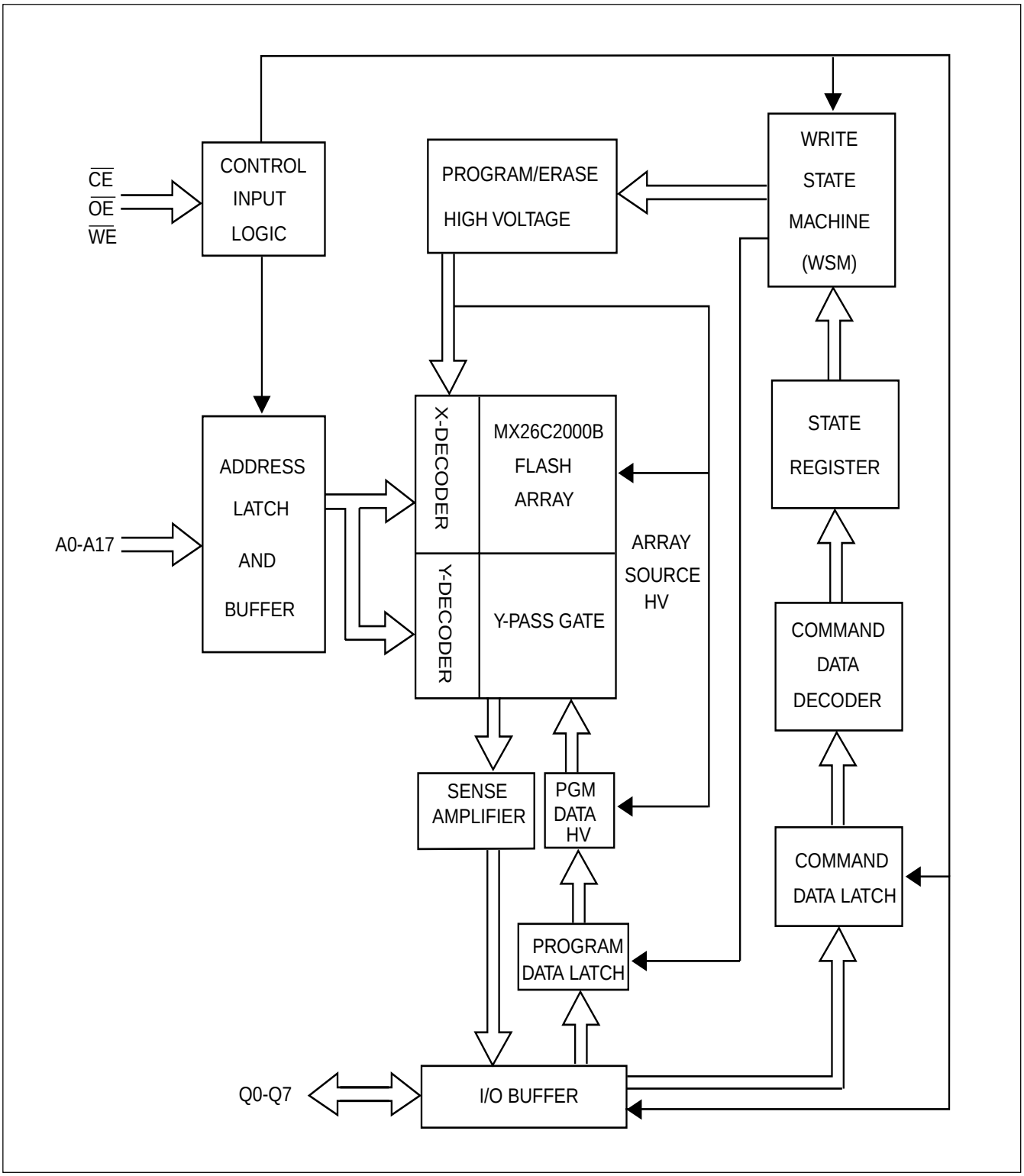
32 TSOP



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A17	Address Input
Q0~Q7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
VPP	Program Supply Voltage
NC	No Internal Connection
VCC	Power Supply Pin (+5V)
GND	Ground Pin

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

When the MX26C2000B is delivered, or it is erased, the chip has all 2000K bits in the "ONE", or HIGH state. "ZEROs" are loaded into the MX26C2000B through the procedure of programming.

ERASE ALGORITHM

The MX26C2000B do not required preprogramming before an erase operation. The erase algorithm is a close loop flow to simultaneously erase all bits in the entire array. Erase operation starts with the initial erase operation. Erase verification begins at address 0000H by reading data FFH from each byte. If any byte fails to erase. the entire chip is reerased. to a maximum for 30 pulse counts of 100ms duration for each pulse. The maximum cumulative erase time is 3s. However. the device is usually erased in no more than 3 pulses. Erase verification time can be reduced by storing the address of the last byte that failed. Following the next erase operation verification may start at the stored address location. JEDEC standard erase algorithm can also be used. But erase time will increase by performing the unnecessary preprogramming.

PROGRAM ALGORITHM

The device is programmed byte by byte. A maximum of 25 pulses. each of 10us duration is allowed for each byte being programmed. The byte may be programmed sequentially or by random. After each program pulse, a program verify is done to determine if the byte has been successfully programmed.

Programming then proceeds to the next desired byte location. JEDEC standard program algorithms can be used.

RESET

The Reset command initializes the MTP EPROM™ device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase). The Reset command must be written two consecutive times after the set-up Program command (40H). This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. How ever, FFH data is considered null data during programming operations (memory cells are only programmed from logica "1" to "0". The second Reset command safely aborts the programming operation and resets the device to the Read mode.

This detailed information is for your reference. It may prove esier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

SET-UP PROGRAM/PROGRAM

A three-step sequence of commands is required to perform a complete program operation: Set Up Program-Program-Program Verify. The device is bulk erased and byte by byte programming. The command 40H is written to the command register to initiate Set Up Program operation. Address and data to be programmed into the byte are provided on the second $\overline{WE}$ pulse. Addresses are latched on the falling edge of the $\overline{WE}$ pulse, data are latched on the rising edge of the $\overline{WE}$ pulse. Program operation begins on the rising edge of the second $\overline{WE}$ pulse, and terminate of the next rising edge of the $\overline{WE}$ pulse. Refer to AC Characteristics and Waveforms for specific timing parameters.

COMMAND REGISTER

When high voltage is applied to V_{PP} the command register is enabled. Read, write, standby, output disable modes are available. The read, erase, erase verify, program, program verify and Device ID are accessed via the command register. Standard microprocessor write timings are used to input a command to the register. This register serves as the input to an internal state machine which controls the operation mode of the device. An internal latch is used for write cycles, addresses and data for programming and erase operations.

NO INTEGRATED STOP TIMER FOR ERASE

Leading industry flash technology requires a stop timer built into the flash chip to prevent the memory cells from going into depletion due to over erase. The 2 Mbit MTP

EPROM™ is built on an innovative cell concept in which over erasing the memory cell is impossible.

DATA WRITE PROTECTION

The design of the device protects against accidental erasure or programming. The internal state machine is automatically reset to the read mode on power-up. Using control register architecture, alteration of memory can only occur after completion of proper command sequences. The command register is only active when V_{PP} is at high voltage. when $V_{PP} = V_{PPL}$, the device defaults to the Read Mode. Robust design features prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise. To avoid initiation of write cycle during V_{CC} power-up, a write cycle is locked out for V_{CC} less than 4V. The two- command program and erase write sequence to the command register provide additional software protection against spurious data changes.

PROGRAM VERIFY MODE

Verification should be performed on the programmed bits to determine that they were correctly programmed. Verification should be performed with $\overline{OE}$ and $\overline{CE}$, at VIL, $\overline{WE}$ at VIH, and VPP at its programming voltage.

ERASE VERIFY MODE

Verification should be performed on the erased chip to determine that the whole chip(all bits) was correctly erased. Verification should be performed with $\overline{OE}$ and $\overline{CE}$ at VIL, $\overline{WE}$ at VIH, and VCC = 5V, VPP = 12.5V

AUTO IDENTIFY MODE

The auto identify mode allows the reading out of a binary code from MTP EPROM that will identify its manufacturer and device type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25℃ ± 5℃ ambient temperature range that is required when programming the MX26C2000B.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the device. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from VIL to VIH. All other address lines must be held at VIL during auto identify mode.

Byte 0 (A0 = VIL) represents the manufacturer code, and byte 1 (A0 = VIH), the device identifier code. For the MX26C2000B, these two identifier bytes are given in the Mode Select Table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

READ MODE

The MX26C2000B has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is available at the outputs tOE after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least tACC - tOE.

STANDBY MODE

The MX26C2000B has a CMOS standby mode which reduces the maximum VCC current to 100 uA. It is placed in CMOS standby when $\overline{CE}$ is at VCC ± 0.3 V. The MX26C2000B also has a TTL-standby mode which reduces the maximum VCC current to 1.5 mA. It is placed in TTL-standby when $\overline{CE}$ is at VIH. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

SYSTEM CONSIDERATIONS

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 uF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between VCC and GND to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive

effects of the printed circuit board traces on EPROM arrays, a 4.7 uF bulk electrolytic capacitor should be used between VCC and GND for each of the eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

OUTPUT DISABLE

Output is disabled when $\overline{OE}$ is at logre high. When in output disabled all circuitry is enabled. Except the output pins are in a high impedance state(TRI-ATATE).

Table 1: BUS OPERATIONS

Mode		VPP(1)	A0	A9	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Q0~Q7
READ-ONLY MODE	Read	VPPL	A0	A9	VIL	VIL	VIH	Data Out
	Output Disable	VPPL	X	X	VIL	VIH	VIH	Tri-State
	Standby	VPPL	X	X	VIH	X	X	Tri-State
	Manufacturer Identification	VPPL	VIL	VID(2)	VIL	VIL	VIH	Data=C2H
	Device Identification	VPPL	VIH	VID(2)	VIL	VIL	VIH	Data=C3H
COMMAND MODE	Read	VPPH	A0	A9	VIL	VIL	VIH	Data Out(3)
	Output Disable	VPPH	X	X	VIL	VIH	VIH	Tri-State
	Standby(4)	VPPH	X	X(5)	VIH	X	X	Tri-State
	Program	VPPH	A0	A9	VIL	VIH	VIL	Data Inb

Note:
1. Refer to DC Characteristics. When VPP=VPPL memory contents can be read but not written or erased.
2. VID is the intelligent identifier high voltage. Refer to DC Characteristics.
3. Read operations with VPP=VPPH may access array data or the intelligent identifier codes.
4. With VPP at high voltage the standby current equals ICC+IPP(standby).
5. Refer to Table 2 for vaild data-in during a write operation.
6. X can be VIL or VIH.

COMMAND MODE

The 2 Mbit MTP EPROM™ is in Command mode when high voltage V_{PPH} is applied to the V_{PP} pin. In this state the available functions are Read, Program, Program Verify, Eraseand Erase Verify. Reset are selected by writing commands to the input register. Data from the register are input to the state machine. The output from the state machine determines the function of the device. The command register serves as a latch to store data for executing commands. It does not occupy address- able memory location. Standard microprocessor write timing is used. Table 2 defines the register commands. The command register is written by bringing $\overline{WE}$ to a logic-low Level (V_{IL}), while $\overline{CE}$ is low. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse.

Standby and Output disable functions are the same as in Read Mode, controlled by $\overline{CE}$ and $\overline{OE}$. If the device is deselected during erasure, programming, or erase/program verification, the device draws active current until the operations terminate.

READ COMMAND

To read memory content, write 00H into the command register while high voltage is applied to V_{PP} pin ($V_{PP} = V_{PPH}$). Microprocessor read cycle retrieves the data . The device remains enable for read until the data in the command register are altered. The device is default in read mode when power up. This is to ensure no accidental alteration of the memory occurs during power transition. Refer to AC Read Characteristics and Waveforms for specific timing parameters.

SET UP ERASE/ERASE

Preprogram operation is not required prior to the erase operation. A sequence of commands is required to perform a complete erase operation: set up erase, erase, and erase verify. High voltage is applied to the V_{PP} pin ($V_{PP}=V_{PPH}$). The command 20H is written to the command register to initiate the set-up erase mode.

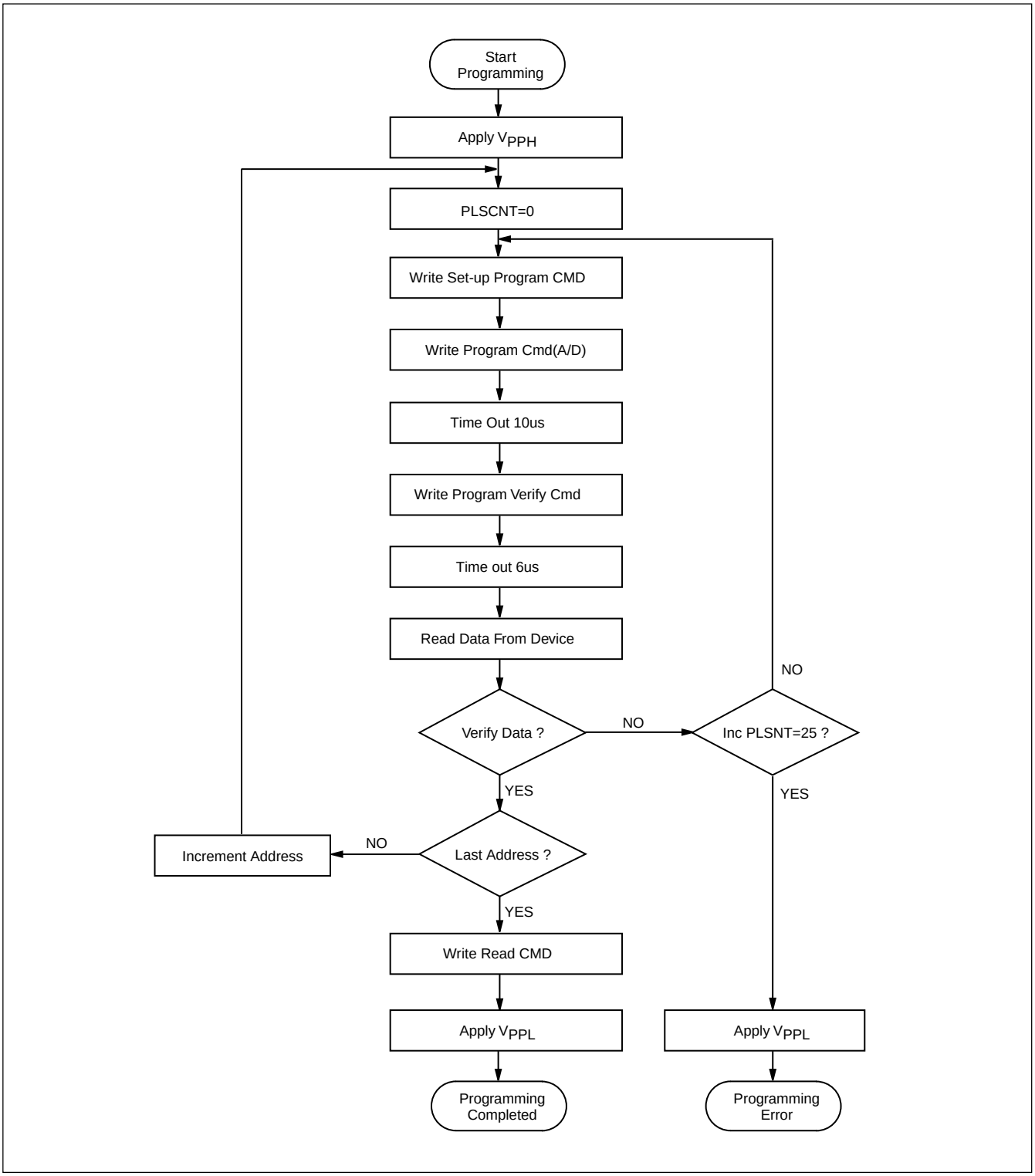
ERASE OPERATION

The same command, 20H, is again written to the command register. This second command starts bulk erase operation. The two-step command prevents accidental alteration to memory array. Erase operation starts with the rising edge of the $\overline{WE}$ pulse and terminates with the rising edge of the next $\overline{WE}$ pulse, which in this case is the erase verify command.

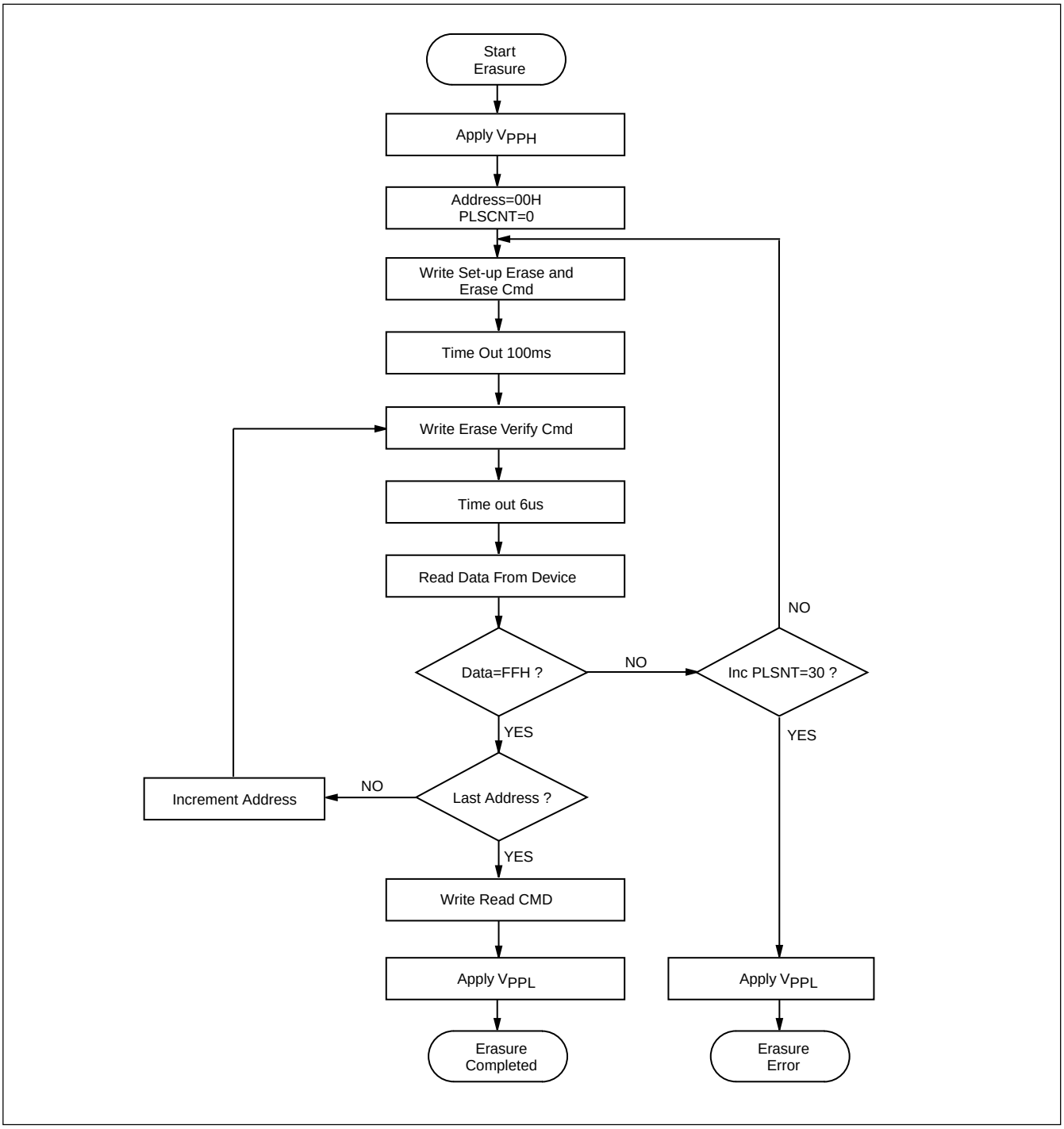
ERASE VERIFY

Each erase operation is followed by an erase verify. The command A0H is written into the command register. The address of the bytes to be verified is supplied with the command. The address is latched on the falling edge of the $\overline{WE}$ pulse. A reading FFH is returned to confirm all bits in the byte are erased. This sequence of Set Up Erase- Erase continues for each address until FFH is returned. This indicates the entire memory array is erased and completes the operation. Erase verify operation starts at address 0000H and ends at the last address. Maximum erase pulse duration for the 2Mbit MTP EPROM™ is 100ms with a maximum 30 pulses. Refer to AC Characteristics and Waveforms for specific timing parameters.

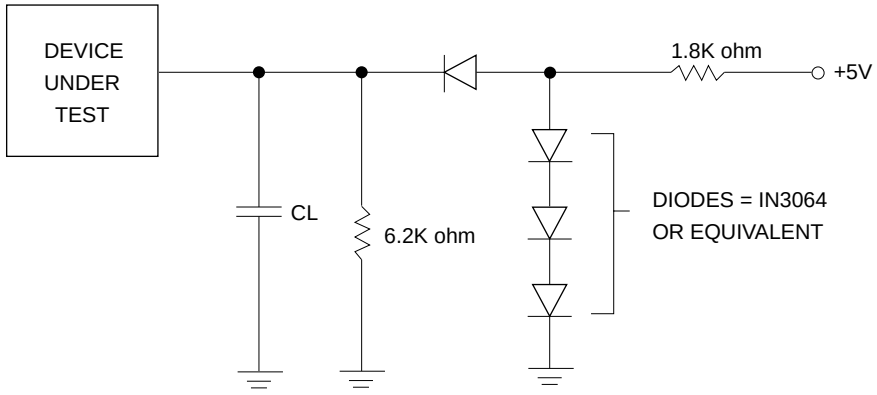
PROGRAMMING ALGORITHM FLOW CHART



ERASE ALGORITHM FLOW CHART

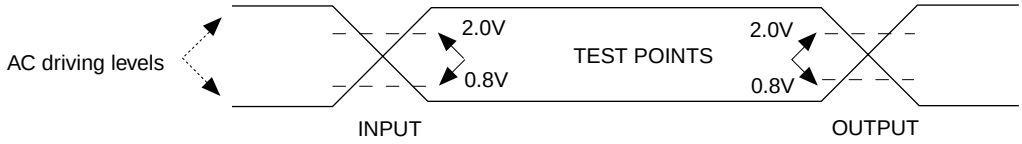


SWITCHING TEST CIRCUITS



CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



AC TESTING: AC driving levels are 2.4V/0.4V for commercial grade.
Input pulse rise and fall times are equal to or less than 10ns.

ABSOLUTE MAXIMUM RATINGS

RATING	VALUE
Ambient Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 125°C
Applied Input Voltage	-0.5V to 7.0V
Applied Output Voltage	-0.5V to VCC + 0.5V
VCC to Ground Potential	-0.5V to 7.0V
A9 & VPP	-0.5V to 13.5V

NOTICE:
Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

NOTICE:
Specifications contained within the following tables are subject to change.

DC/AC OPERATING CONDITION FOR READ OPERATION

		MX26C2000B			
		-90	**-100**	**-120**	-150
Operating Temperature	Industrial	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃	-40℃ to 85℃
Vcc Power Supply		5V ± 10%	5V ± 10%	5V ± 10%	5V ± 10%

CAPACITANCE TA = 25°C, f = 1.0 MHz (Sampled only)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT	CONDITIONS
CIN	Input Capacitance	8	12	pF	VIN = 0V
COUT	Output Capacitance	8	12	pF	VOUT = 0V
CVPP	VPP Capacitance	18	25	pF	VPP = 0V

DC CHARACTERISTICS TA = -45℃ ~ 85℃, VCC=5V±10%

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
VIL	Input Low Voltage	-0.3	0.8	V	
VIH	Input High Voltage	2.0	VCC + 0.5	V	
VOL	Output Low Voltage		0.4	V	IOL = 2.1mA, VCC=VCC MIN
VOH	Output High Voltage	2.4		V	IOH = -0.4mA
ICC1	VCC Active Current		30	mA	$\overline{CE}$ = VIL, $\overline{OE}$=VIH, f=5MHz
ISB	VCC Standby Current (CMOS)		100	uA	$\overline{CE}$=VCC+0.2V, VCC=VCC MAX
ISB	VCC Standby Current (TTL)		1.5	mA	$\overline{CE}$=VIH, VCC=VCC MAX
IPP	VPP Read Current		100	uA	$\overline{CE}$ = $\overline{OE}$ = VIL, VPP = 5.5V
IPP2	VPP Supply Current (Program/Erase)		30	mA	$\overline{CE}$=$\overline{WE}$=VIL, $\overline{OE}$=VIH
ILI	Input Leakage Current	-10	10	uA	VIN = 0 to 5.5V
ILO	Output Leakage Current	-10	10	uA	VOUT = 0 to 5.5V
VCC1	Fast Programming Supply Voltage	6.0	6.5	V	
VPP1	Fast Programming Voltage	12.5	13.0	V	

AC RAED CHARACTERISTICS OVER OPERATING RANGE WITH VPP=VCC

Symbol		Parameter	90		100		120		150		Unit
Jeded	STD		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tAVAV	TRC	Read Cycle Time	90		100		120		150		ns
tELQV	TCE	$\overline{CE}$ Access Time	0	90	0	100	0	120	0	150	ns
tAVQV	TACC	Address Access Time	0	90	0	100	0	120	0	150	ns
tGLQV	TOE	$\overline{OE}$ Access Time	0	40	0	45	0	50	0	65	ns
tELQX	TLZ	$\overline{CE}$ to Output in Low Z(Note 1)	0		0		0		0		ns
tEHQZ	TDF	Chip Disable to Output in High Z(Note 2)	0	30	0	35	0	35	0	50	ns
tGLQX	TOLZ	$\overline{OE}$ to Output in Low Z (Note 1)	0		0		0		0		ns
tGHQZ	TDF	Output Disable to Output in High Z (Note 1)	0	30	0	35	0	35	0	50	ns
tAXQX	TOH	Output Hold from Address, $\overline{CE}$ or $\overline{OE}$, change		0		0		0		0	ns
tWHGL	TWHGL	Write Recovery Time Before Read	6		6		6		6		us
tVCS	TVCS	VCC Setup Time to Valid Read (Note 2)		50		50		50		50	us

Note:
1. Sampled: not 100% tested.
2. Guaranteed by design. not tested.

AC CHARACTERISTICS - WRITE/ERASE/PROGRAM OPERATIONS

Symbol		Parameter	90		100		120		150		Unit
JEDED	STD		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
tAVAV	TWC	Write Cycle Time (Note 3)	90		100		120		150		ns
tAVWL	TAS	Address Setup Time	0		0		0		0		ns
tWLAX	TAH	Address Hold Time	40		40		40		40		ns
tDVWH	TDS	Data Setup Time	40		40		40		40		ns
tWHDX	TDH	Data Hold Time	10		10		10		10		ns
tWHGL	TWR	Write Recovery Time Before Read	6		6		6		6		us
tGHWL	TDES	Read Recovery Time Before Write	0		0		0		0		us
tELWL	tCS	$\overline{CE}$ Setup Time Before Write	0		0		0		0		ns
tWHEH	tCH	$\overline{CE}$ Hold Time	0		0		0		0		ns
tWLWH	tWP	Write Pulse Width	50		50		50		50		ns
tWHWL	tWPH	Write Pulse Width High	20		20		20		20		ns
tWHWH1		Duration of Programming Operation (Note2)	10		10		10		10		us
tWHWH2		Duration of Erase Operation(Note2)	100		100		100		100		ms
tVPEL		VPP Setup Time to Chip Enable Low (Note 3)	1		1		1		1		us
tVCS		VCC Setup Time to Chip Enable Low (Note 3)	50		50		50		50		us
tVPPR		VPP Rise Time (Note 3) 90% VPPH	500		500		500		500		ns
tVPPF		VPP Fall Time (Note 3) 10% VPPH	500		500		500		500		ns

Note:
1. Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only Operations.
2. Maximum pulse widths not required because the on-chip program/erase circuitry will terminate the pulse widths internally on the device.
3. Not 100% tested.

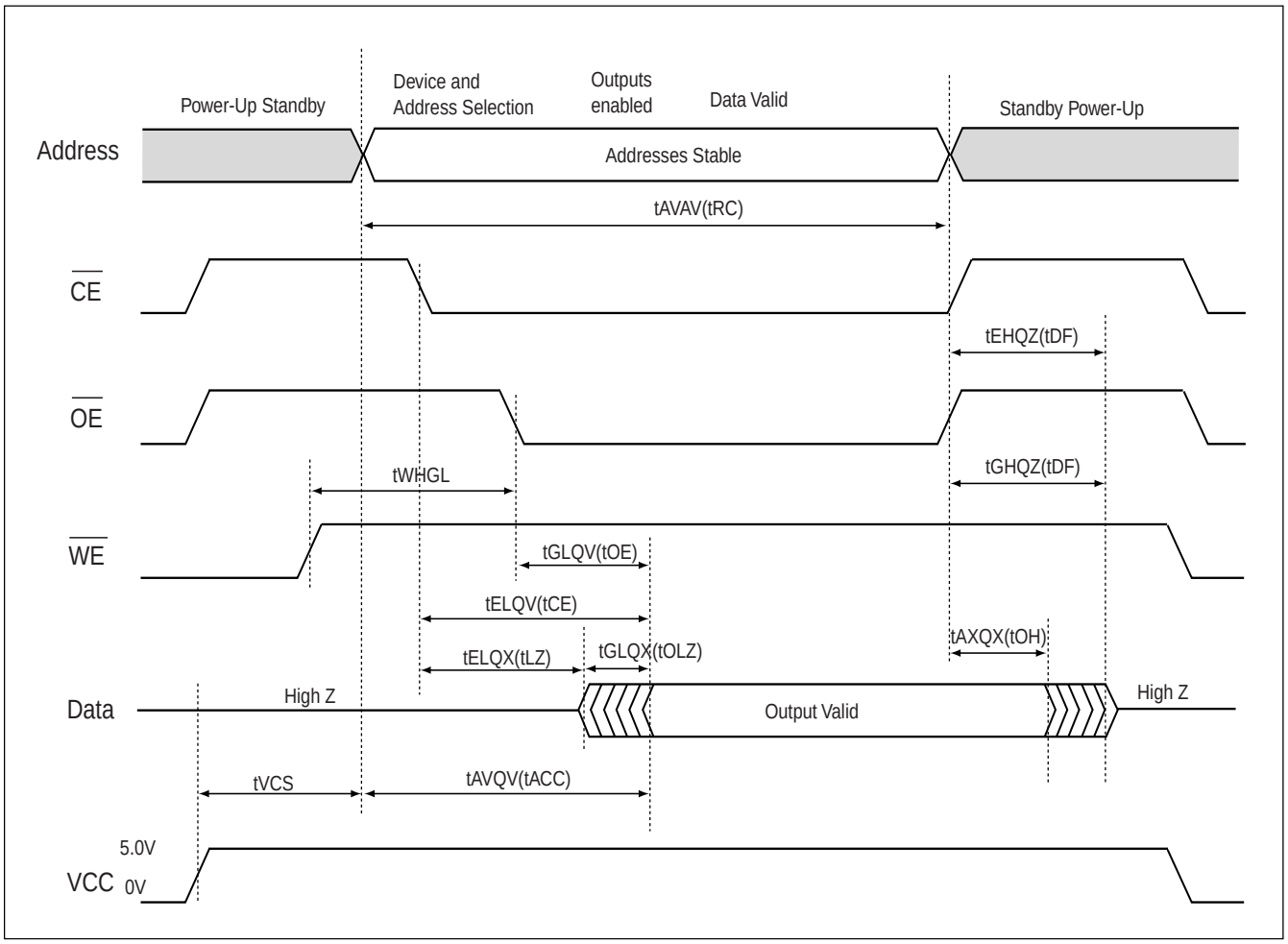
Table 2: Command Definitions

Command	Bus Cycles. Req	First Bus Cycle			Second Bus Cycle		
		Operation	Address[1]	Data[2]	Operation	Address[1]	Data[2]
Read Memory	1	Write	X	00H			
Setup Erase/Erase	2	Write	X	20H	Write	X	20H
Erase Verify	2	Write	EA	A0H	Read	X	EVD
Setup Program/Program	2	Write	X	40H	Write	PA	PD
Program Verify	2	Write	X	C0H	Read	X	PVD
Reset	2	Write	X	FFH	Write	X	FFH

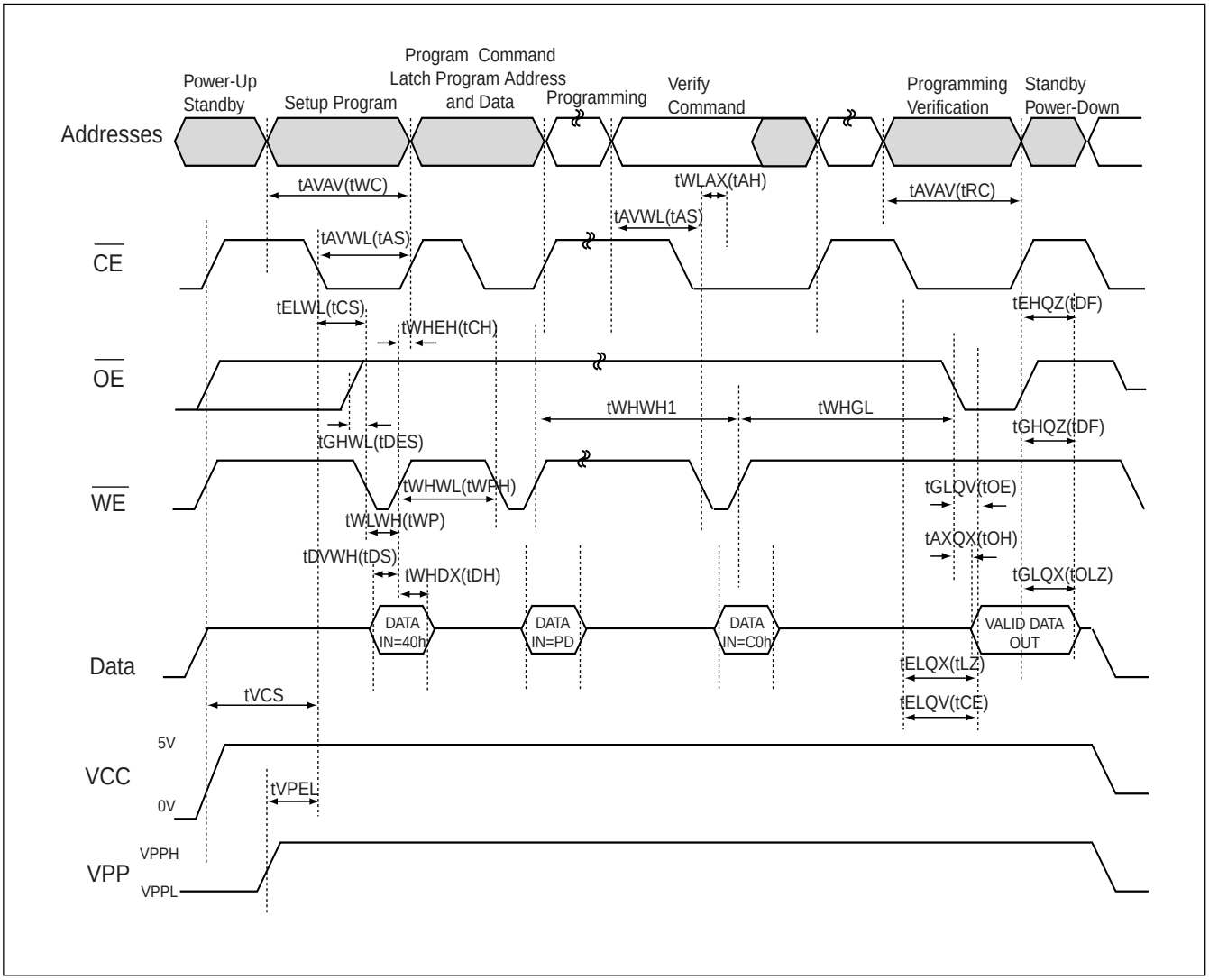
1 EA=Erase Address: address of memory location to be read during erase verify.
PA=Program Address: address of memory location to be Programmed.
Address are latched on the falling edge of the $\overline{WE}$ pulse.

2 EVD=Erase Verify Data: data read from location EA during erase verify.
PD=Program Data: data to be programmed at location PA. Data is latched on the rising edge of $\overline{WE}$.
PVD=Program Verify Data: data read from location PA during program verify. PA is latched on the Program command.

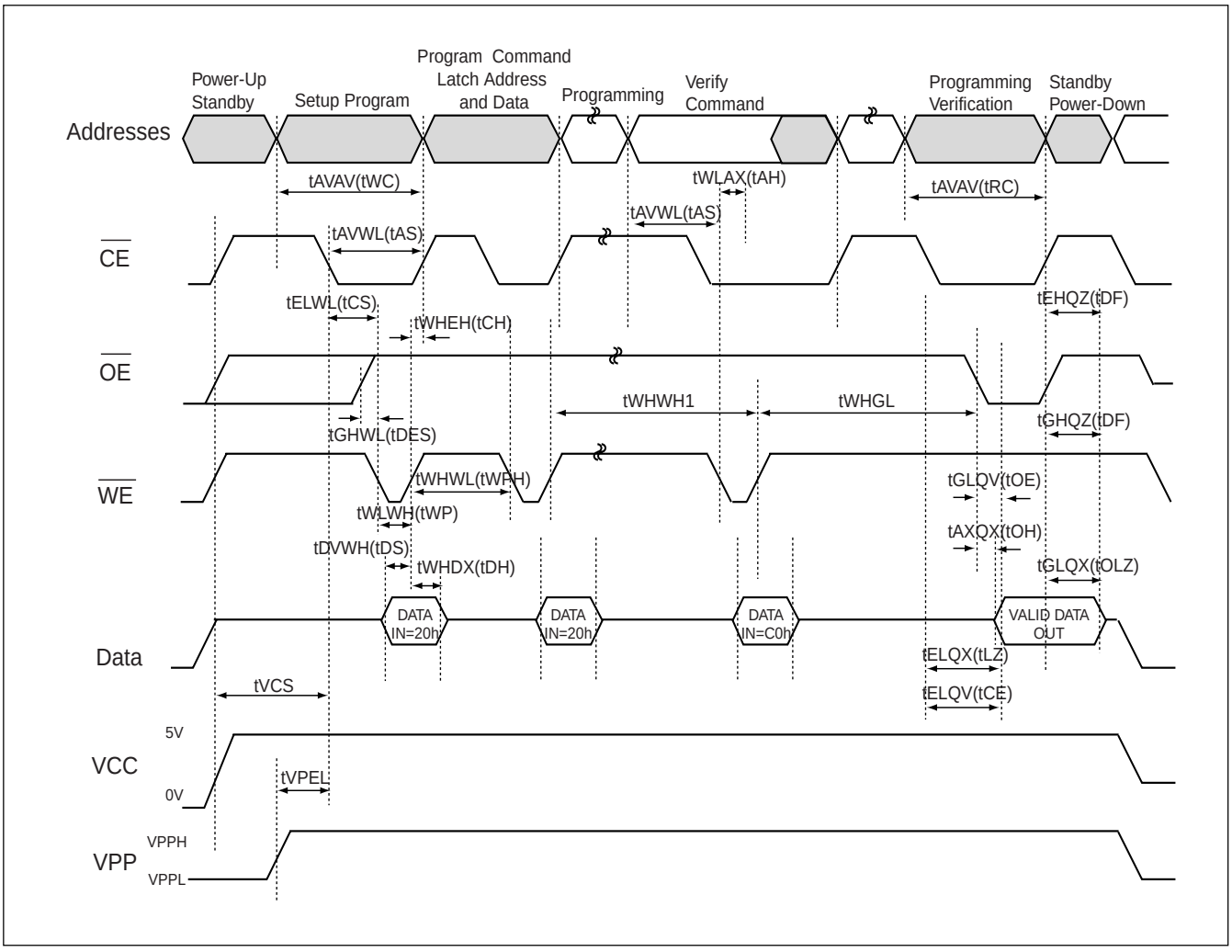
AC WAVEFORMS FOR READ OPERATIONS



AC WAVEFORMS FOR ERASE OPERATIONS



AC WAVEFORMS FOR PROGRAMMING OPERATIONS



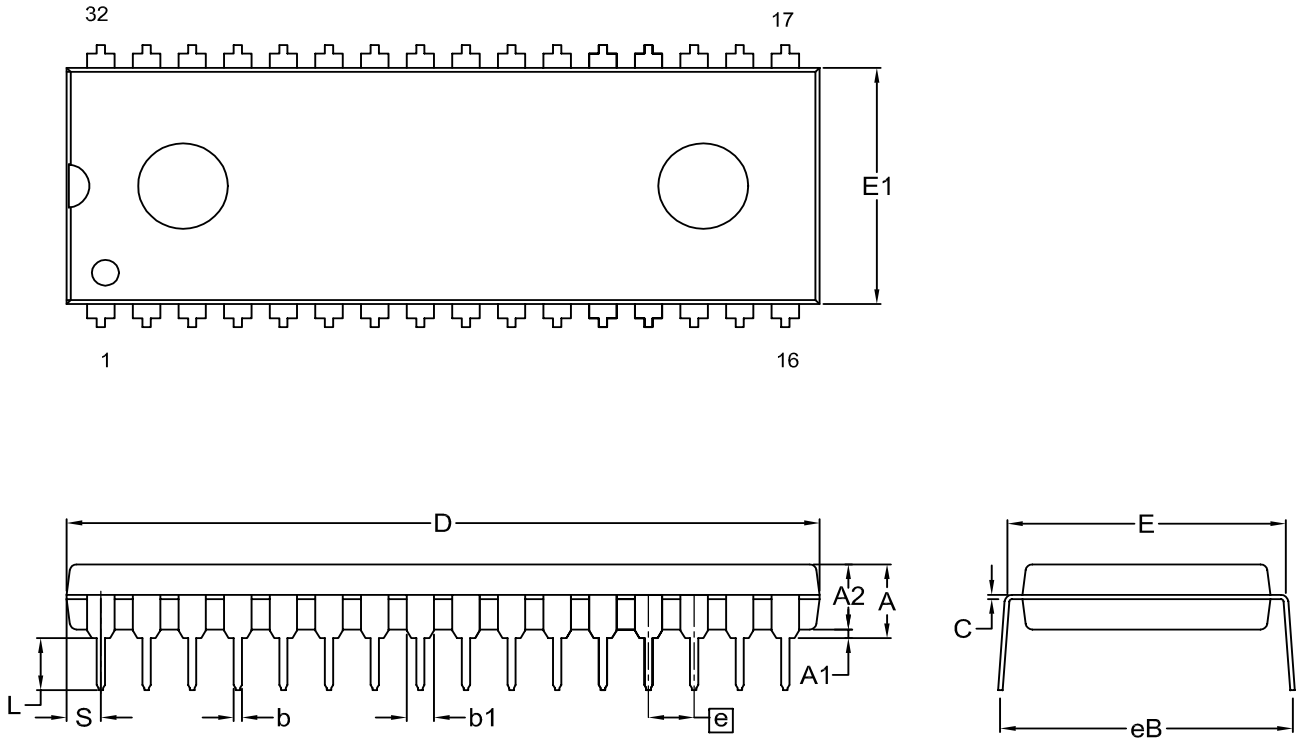
ORDERING INFORMATION

PLASTIC PACKAGE

PART NO.	ACCESS TIME(ns)	OPERATING Current MAX.(mA)	STANDBY Current MAX.(uA)	OPERATING TEMPERATURE	PACKAGE
MX26C2000BPC-90	90	30	100	0℃ to 70℃	32 Pin DIP
MX26C2000BQC-90	90	30	100	0℃ to 70℃	32 Pin PLCC
MX26C2000BMC-90	90	30	100	0℃ to 70℃	32 Pin SOP
MX26C2000BTC-90	90	30	100	0℃ to 70℃	32 Pin TSOP
MX26C2000BPC-10	100	30	100	0℃ to 70℃	32 Pin DIP
MX26C2000BQC-10	100	30	100	0℃ to 70℃	32 Pin PLCC
MX26C2000BMC-10	100	30	100	0℃ to 70℃	32 Pin SOP
MX26C2000BTC-10	100	30	100	0℃ to 70℃	32 Pin TSOP
MX26C2000BPC-12	120	30	100	0℃ to 70℃	32 Pin DIP
MX26C2000BQC-12	120	30	100	0℃ to 70℃	32 Pin PLCC
MX26C2000BMC-12	120	30	100	0℃ to 70℃	32 Pin SOP
MX26C2000BTC-12	120	30	100	0℃ to 70℃	32 Pin TSOP
MX26C2000BPC-15	150	30	100	0℃ to 70℃	32 Pin DIP
MX26C2000BQC-15	150	30	100	0℃ to 70℃	32 Pin PLCC
MX26C2000BMC-15	150	30	100	0℃ to 70℃	32 Pin SOP
MX26C2000BTC-15	150	30	100	0℃ to 70℃	32 Pin TSOP
MX26C2000BPI-90	90	30	100	-40℃ to 85℃	32 Pin DIP
MX26C2000BQI-90	90	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C2000BMI-90	90	30	100	-40℃ to 85℃	32 Pin SOP
MX26C2000BTI-90	90	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C2000BPI-10	100	30	100	-40℃ to 85℃	32 Pin DIP
MX26C2000BQI-10	100	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C2000BMI-10	100	30	100	-40℃ to 85℃	32 Pin SOP
MX26C2000BTI-10	100	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C2000BPI-12	120	30	100	-40℃ to 85℃	32 Pin DIP
MX26C2000BQI-12	120	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C2000BMI-12	120	30	100	-40℃ to 85℃	32 Pin SOP
MX26C2000BTI-12	120	30	100	-40℃ to 85℃	32 Pin TSOP
MX26C2000BPI-15	150	30	100	-40℃ to 85℃	32 Pin DIP
MX26C2000BQI-15	150	30	100	-40℃ to 85℃	32 Pin PLCC
MX26C2000BMI-15	150	30	100	-40℃ to 85℃	32 Pin SOP
MX26C2000BTI-15	150	30	100	-40℃ to 85℃	32 Pin TSOP

PACKAGE INFORMATION

Title: Package Outline for PDIP 32L(600MIL)

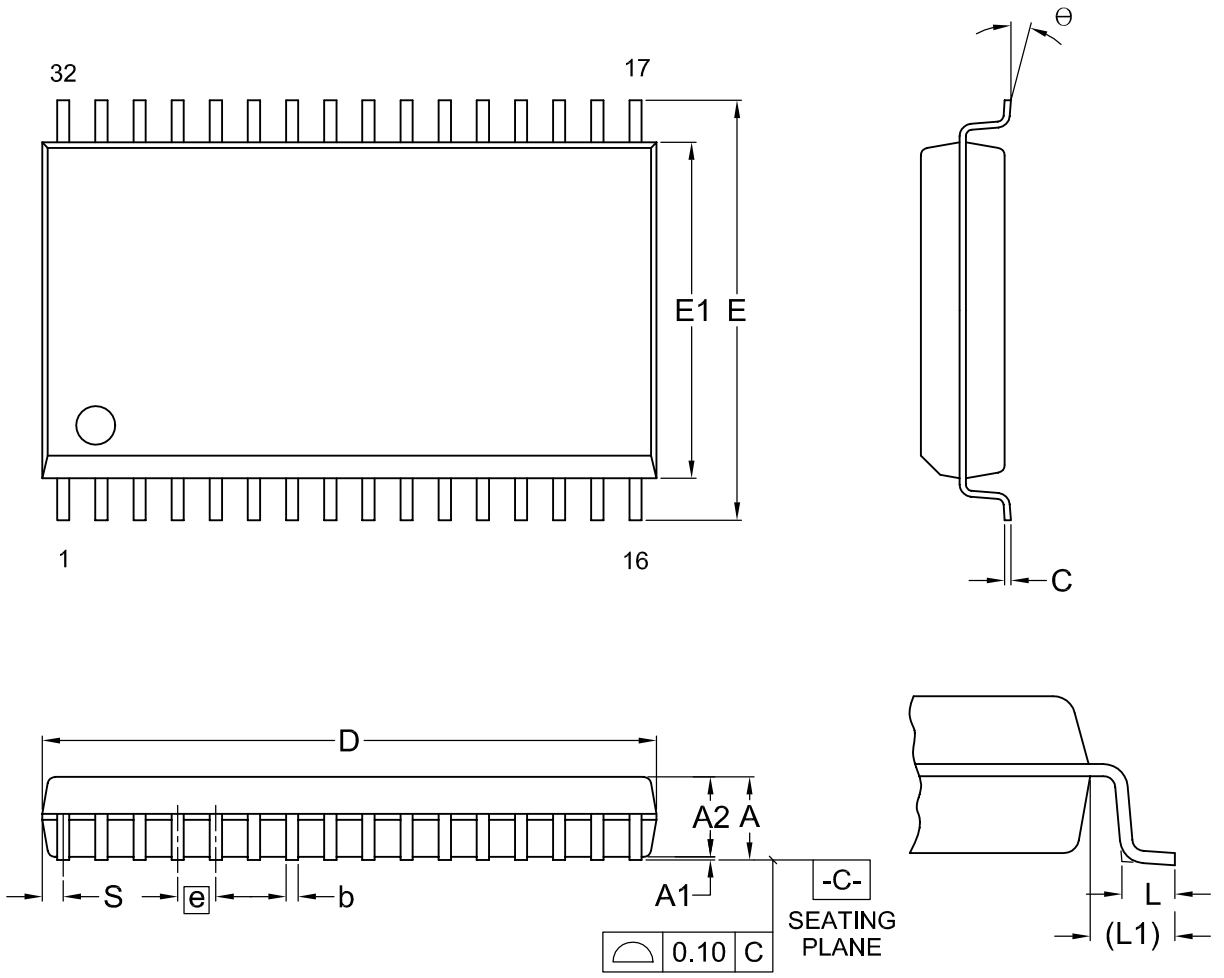


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	E	E1	e	eB	L	S
mm	Min.	---	0.51	3.73	0.38	1.14	0.20	41.78	15.11	13.84		15.75	2.92	1.65
	Nom.	---	0.64	3.94	0.46	1.27	0.25	41.91	15.24	13.97	2.54	16.51	3.30	1.90
	Max.	4.90	0.76	4.14	0.53	1.40	0.30	42.04	15.37	14.10		17.27	3.68	2.16
Inch	Min.	---	0.020	0.147	0.015	0.045	0.008	1.645	0.595	0.545		0.620	0.115	0.065
	Nom.	---	0.025	0.155	0.018	0.050	0.010	1.650	0.600	0.550	0.100	0.650	0.130	0.075
	Max.	0.193	0.030	0.163	0.021	0.055	0.012	1.655	0.605	0.555		0.680	0.145	0.085

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-0202.2	5				07-04-'02

Title: **Package Outline for SOP 32L (450MIL)**

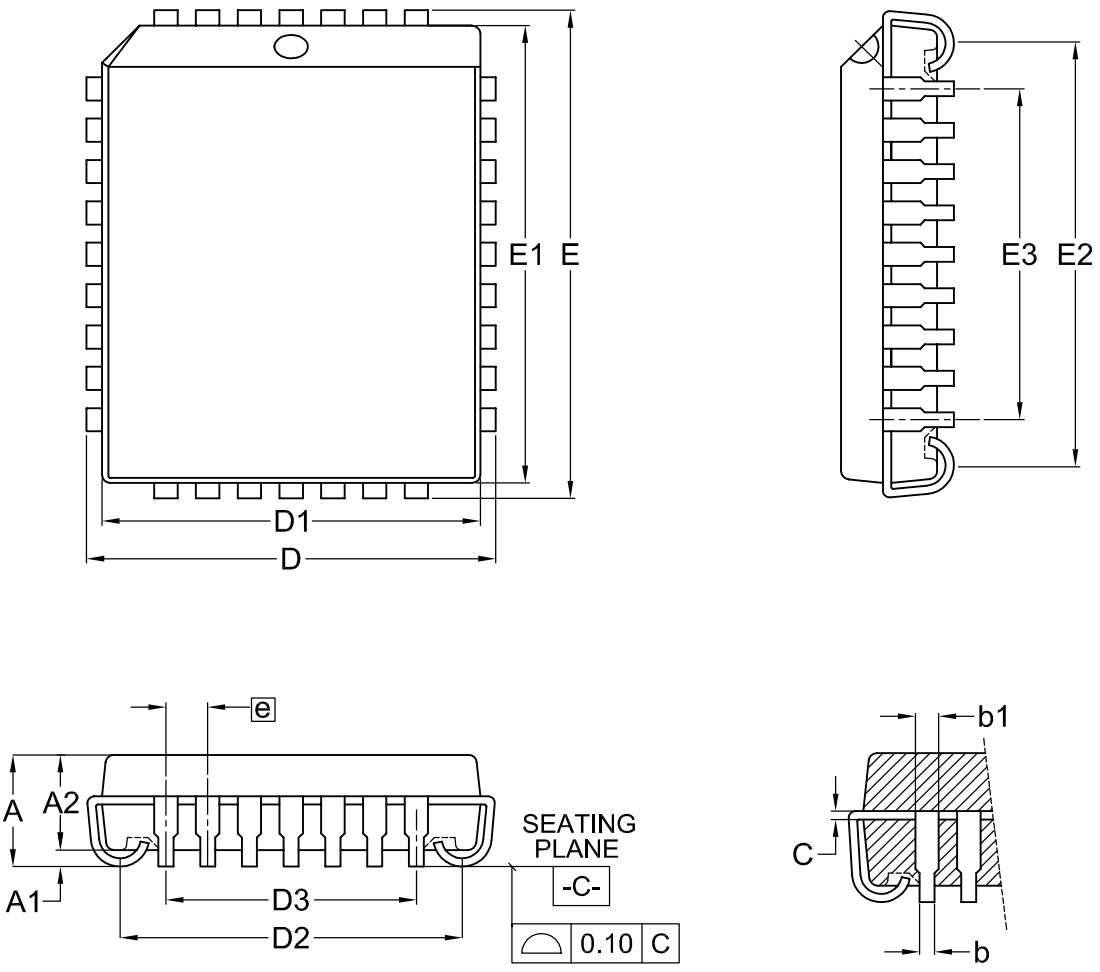


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	E	E1	e	L	L1	S	θ
mm	Min.	---	0.10	2.59	0.36	0.15	20.32	13.92	11.18		0.56	1.20	0.58	0
	Nom.	---	0.15	2.69	0.41	0.20	20.45	14.12	11.30	1.27	0.76	1.40	0.70	5
	Max.	3.00	0.20	2.80	0.51	0.25	20.57	14.32	11.43		0.96	1.60	0.83	8
Inch	Min.	---	0.004	0.102	0.014	0.006	0.800	0.548	0.440		0.022	0.047	0.023	0
	Nom.	---	0.006	0.106	0.016	0.008	0.805	0.556	0.445	0.050	0.030	0.055	0.028	5
	Max.	0.118	0.008	0.110	0.020	0.010	0.810	0.564	0.450		0.038	0.063	0.033	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1404	4	MO-099			09-24-'02

Title: **Package Outline for 32L PLCC**

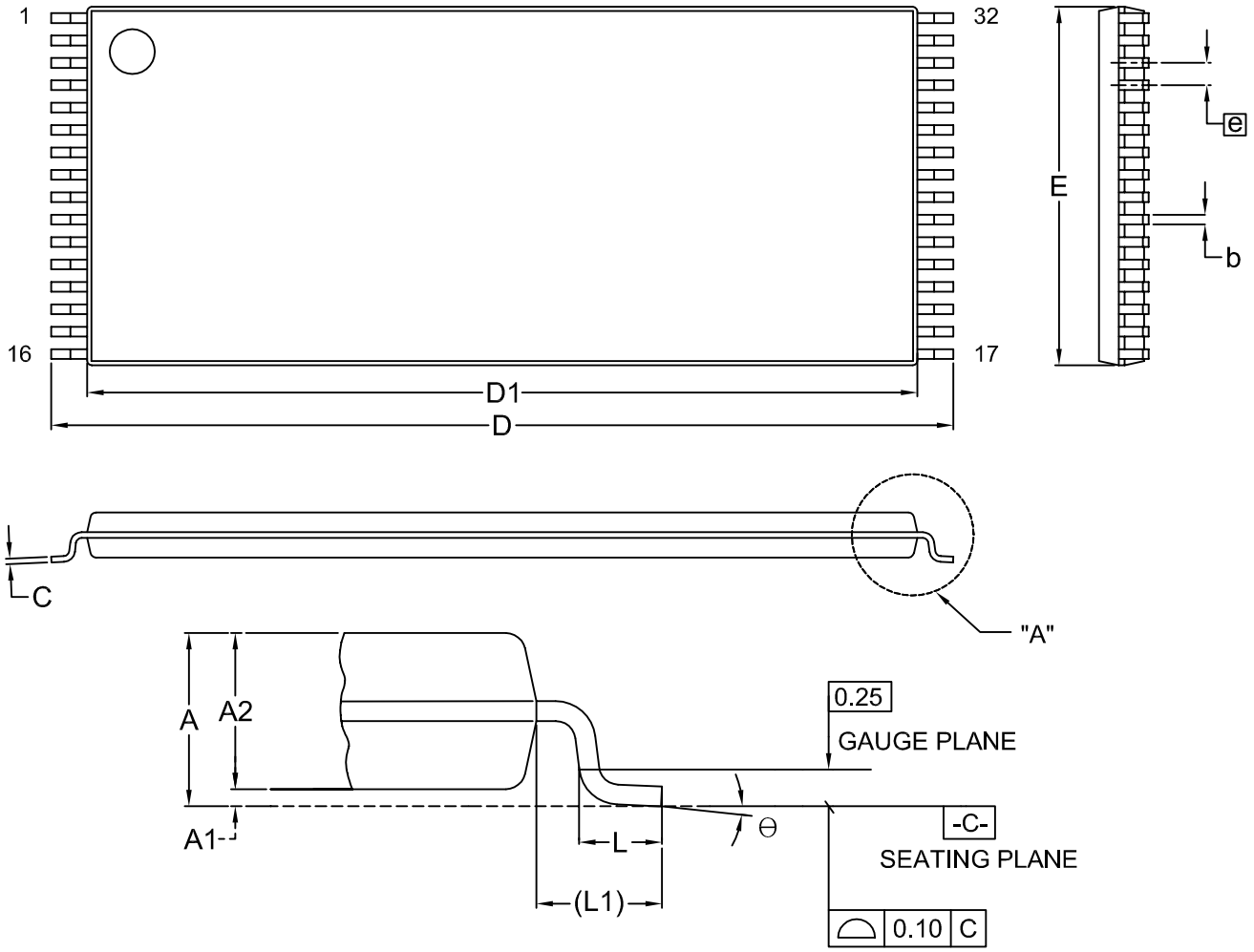


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	b1	C	D	D1	D2	D3	E	E1	E2	E3	e
mm	Min.	---	0.38	2.69	0.38	0.61	0.20	12.32	11.44	10.11		14.86	13.98	12.65		
	Nom.	---	0.50	2.79	0.46	0.71	0.25	12.45	11.51	10.41	7.62	14.99	14.05	12.95	10.16	1.27
	Max.	3.55	0.66	2.89	0.54	0.81	0.30	12.58	11.58	10.71		15.12	14.12	13.25		
Inch	Min.	---	0.015	0.106	0.015	0.024	0.008	0.485	0.450	0.398		0.585	0.550	0.498		
	Nom.	---	0.020	0.110	0.018	0.028	0.010	0.490	0.453	0.410	0.300	0.590	0.553	0.510	0.400	0.050
	Max.	0.140	0.026	0.114	0.021	0.032	0.012	0.495	0.456	0.422		0.595	0.556	0.522		

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-2002	4	MS-016			09-24-'02

Title: **Package Outline for TSOP(I) 32L (8X20mm)**



Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL / UNIT		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	---	0.05	0.95	0.17	0.10	19.80	18.30	7.90		0.50	0.70	0
	Nom.	---	0.10	1.00	0.20	0.15	20.00	18.40	8.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	8.10		0.70	0.90	8
Inch	Min.	---	0.002	0.037	0.007	0.004	0.780	0.720	0.311		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.006	0.787	0.724	0.315	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.319		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1604	8	MO-142			09-24-'02

Revision History

Revision No.	Description	Page	Date
0.1	To Add speed 100ns to MX26C2000B	P1,10,11,12,18	NOV/28/2000
	Modify the "DC CHARACTERISTICS" table	P10	
0.2	To add erase/program cycle	P1	DEC/18/2000
	Changed title from MX26C2000A to MX26C2000B	All	
0.3	Change Device ID code from 31H to CFH	P5	DEC/28/2000
0.4	To added 32SOP/TSOP types package and access time 150ns	P1,11,12,17,18	MAR/27/2001
	Modify device ID old CFH-->New C3H	P5	
	Modify read ID method	P4,5,6,13	
	Modify erase/program cycle from 100 to 50	P1	
	Modify VCC Standby Current(TTL) from 1mA to 1.5mA	P10	
0.5	To added VCC1 & VPP1 to DC Characteristics Table	P10	APR/23/2001
	Modify Package Information	P18~21	
0.6	To added chip erase time / chip program time	P1	JUL/04/2001
	Modify Package Information	P18~21	
0.7	Modify the Programming Operations Timing Waveforms	P15	OCT/04/2001
0.8	To modify Package Information	P18~21	NOV/20/2002

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