



MX29LV033M

32M-BIT SINGLE VOLTAGE 3V ONLY UNIFORM SECTOR FLASH MEMORY

FEATURES

GENERAL FEATURES

- Single Power Supply Operation
 - 2.7 to 3.6 volt for read, erase, and program operations
- Configuration
 - 4,194,304 x 8 byte structure
- Sector structure
 - 64KB x 64
- Sector Protection/Chip Unprotect
 - Provides sector group protect function to prevent program or erase operation in the protected sector group
 - Provides chip unprotect function to allow code changes
 - Provides temporary sector group unprotect function for code changes in previously protected sector groups
- Secured Silicon Sector
 - Provides a 256-byte OTP area for permanent, secure identification
 - Can be programmed and locked at factory or by customer
- Latch-up protected to 250mA from -1V to VCC + 1V
- Low VCC write inhibit is equal to or less than 1.5V
- Compatible with JEDEC standard
 - Pin-out and software compatible to single power supply Flash

PERFORMANCE

- High Performance
 - Fast access time: 70R/90ns
 - Page read time: 25ns
 - Sector erase time: 0.5s (typ.)
 - Effective write buffer byte programming time: 11us
 - 8 byte page read buffer
 - 32 byte write buffer: reduces programming time for multiple-byte updates

GENERAL DESCRIPTION

The MX29LV033M is a 32-mega bit Flash memory organized as 4M bytes of 8 bits. MXIC's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The MX29LV033M is packaged in 40-pin TSOP. It is designed to be reprogrammed and erased in system or in standard EPROM

- Low Power Consumption
 - Active read current: 18mA(typ.)
 - Active write current: 50mA(typ.)
 - Standby current: 20uA(typ.)
- Minimum 100,000 erase/program cycle
- 20-year data retention

SOFTWARE FEATURES

- Support Common Flash Interface (CFI)
 - Flash device parameters stored on the device and provide the host system to access.
- Program Suspend/Program Resume
 - Suspend program operation to read other sectors
- Erase Suspend/Erase Resume
 - Suspends sector erase operation to read or program other sectors
- Status Reply
 - Data# polling & Toggle bits provide detection of program and erase operation completion

HARDWARE FEATURES

- Ready/Busy (RY/BY#) Output
 - Provides a hardware method of detecting program and erase operation completion
- Hardware Reset (RESET#) Input
 - Provides a hardware method to reset the internal state machine to read mode
- ACC input
 - ACC (high voltage) accelerates programming time for higher throughput during system

PACKAGE

- 40-pin TSOP
- **All Pb-free devices are RoHS Compliant**

programmers.

The standard MX29LV033M offers access time as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the MX29LV033M has separate chip enable (CE#) and

output enable (OE#) controls.

MXIC's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The MX29LV033M uses a command register to manage this functionality.

MXIC Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The MXIC cell is designed to optimize the erase and program mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The MX29LV033M uses a 2.7V to 3.6V VCC supply to perform the High Reliability Erase and auto Program/Erase algorithms.

The highest degree of latch-up protection is achieved with MXIC's proprietary non-epi process. Latch-up protection is proved for stresses up to 100 milliamperes on address and data pin from -1V to VCC + 1V.

AUTOMATIC PROGRAMMING

The MX29LV033M is byte/page programmable using the Automatic Programming algorithm. The Automatic Programming algorithm makes the external system do not need to have time out sequence nor to verify the data programmed.

AUTOMATIC PROGRAMMING ALGORITHM

MXIC's Automatic Programming algorithm require the user to only write program set-up commands (including 2 unlock write cycle and A0H) and a program command (program data and address). The device automatically times the programming pulse width, provides the program verification, and counts the number of sequences. A status bit similar to DATA# polling and a status bit toggling between consecutive read cycles, provide feedback to the user as to the status of the programming operation.

AUTOMATIC CHIP ERASE

The entire chip is bulk erased using 50 ms erase pulses according to MXIC's Automatic Chip Erase algorithm. The Automatic Erase algorithm automatically programs the entire array prior to electrical erase. The timing and veri-

fication of electrical erase are controlled internally within the device.

AUTOMATIC SECTOR ERASE

The MX29LV033M is sector(s) erasable using MXIC's Auto Sector Erase algorithm. Sector erase modes allow sectors of the array to be erased in one erase cycle. The Automatic Sector Erase algorithm automatically programs the specified sector(s) prior to electrical erase. The timing and verification of electrical erase are controlled internally within the device.

AUTOMATIC ERASE ALGORITHM

MXIC's Automatic Erase algorithm requires the user to write commands to the command register using standard microprocessor write timings. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verification, and counts the number of sequences. A status bit toggling between consecutive read cycles provides feedback to the user as to the status of the programming operation.

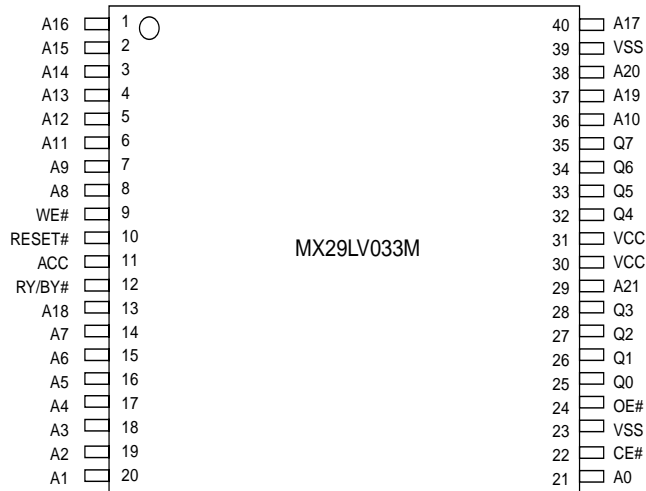
Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. During a system write cycle, addresses are latched on the falling edge, and data are latched on the rising edge of WE#.

MXIC's Flash technology combines years of EPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The MX29LV033M electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed by using the EPROM programming mechanism of hot electron injection.

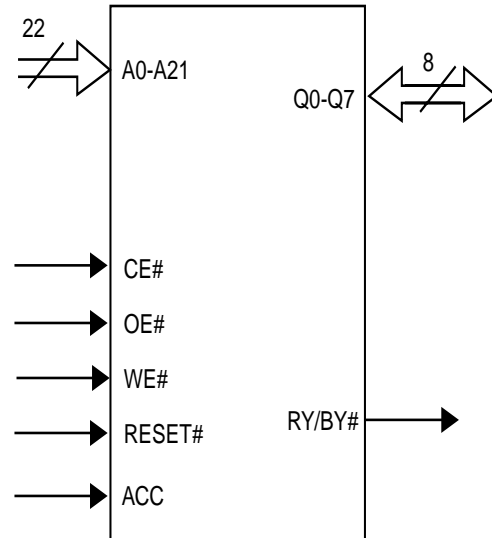
During a program cycle, the state-machine will control the program sequences and command register will not respond to any command set. During a Sector Erase cycle, the command register will only respond to Erase Suspend command. After Erase Suspend is completed, the device stays in read mode. After the state machine has completed its task, it will allow the command register to respond to its full command set.

PIN CONFIGURATION

40TSOP

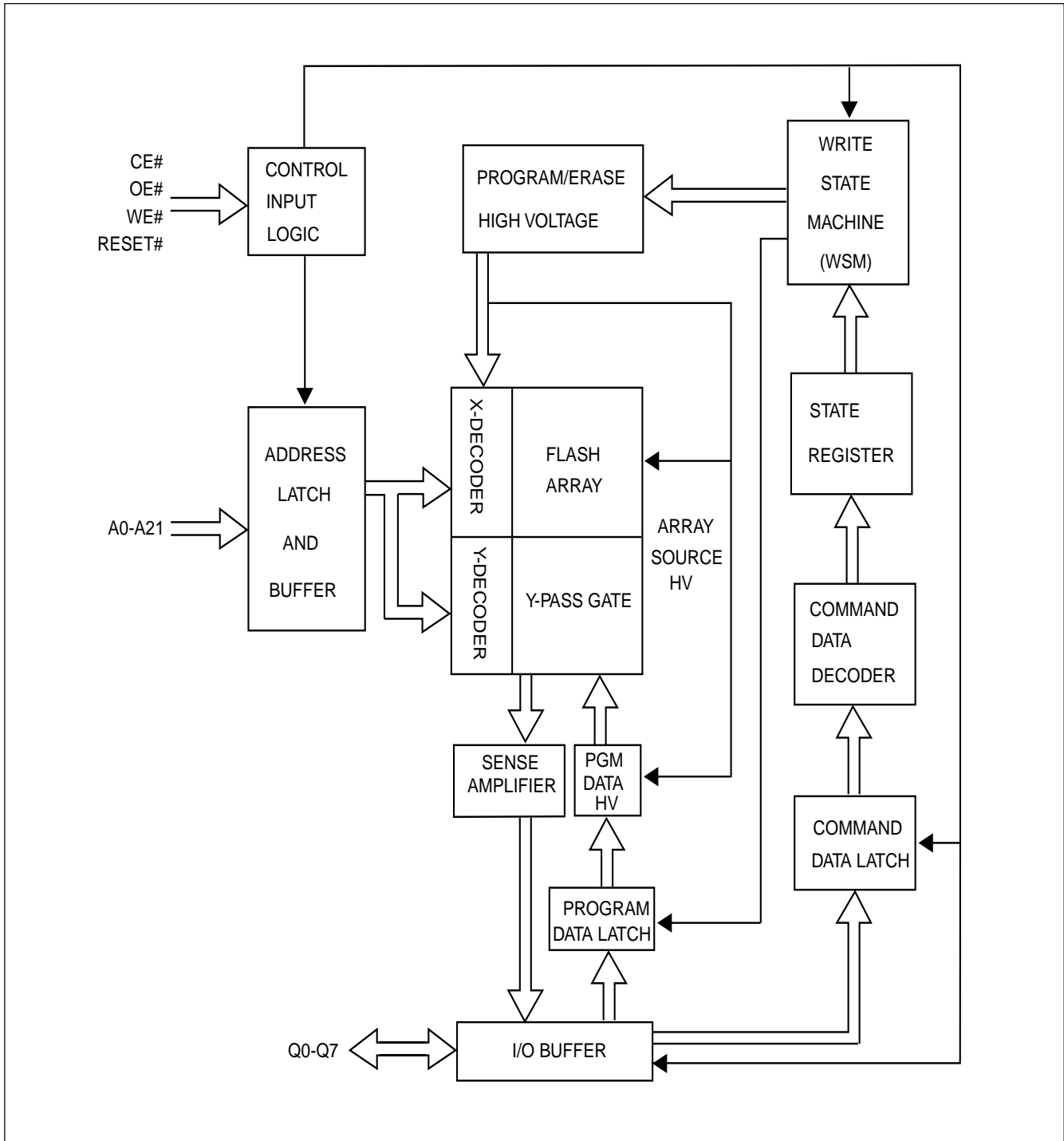


LOGIC SYMBOL



PIN DESCRIPTION

SYMBOL	PIN NAME
A0~A21	Address Input
Q0~Q7	8 Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
RESET#	Hardware Reset Pin, Active Low
RY/BY#	Read/Busy Output
VCC	+3.3V single power supply
ACC	Hardware Acceleration Pin
VSS	Device Ground
NC	Pin Not Connected Internally

BLOCK DIAGRAM


SECTOR (GROUP) STRUCTURE

Sector	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA0	0	0	0	0	0	0	000000-00FFFF
SA1	0	0	0	0	0	1	010000-01FFFF
SA2	0	0	0	0	1	0	020000-02FFFF
SA3	0	0	0	0	1	1	030000-03FFFF
SA4	0	0	0	1	0	0	040000-04FFFF
SA5	0	0	0	1	0	1	050000-05FFFF
SA6	0	0	0	1	1	0	060000-06FFFF
SA7	0	0	0	1	1	1	070000-07FFFF
SA8	0	0	1	0	0	0	080000-08FFFF
SA9	0	0	1	0	0	1	090000-09FFFF
SA10	0	0	1	0	1	0	0A0000-0AFFFF
SA11	0	0	1	0	1	1	0B0000-0BFFFF
SA12	0	0	1	1	0	0	0C0000-0CFFFF
SA13	0	0	1	1	0	1	0D0000-0DFFFF
SA14	0	0	1	1	1	0	0E0000-0EFFFF
SA15	0	0	1	1	1	1	0F0000-0FFFFF
SA16	0	1	0	0	0	0	100000-10FFFF
SA17	0	1	0	0	0	1	110000-11FFFF
SA18	0	1	0	0	1	0	120000-12FFFF
SA19	0	1	0	0	1	1	130000-13FFFF
SA20	0	1	0	1	0	0	140000-14FFFF
SA21	0	1	0	1	0	1	150000-15FFFF
SA22	0	1	0	1	1	0	160000-16FFFF
SA23	0	1	0	1	1	1	170000-17FFFF
SA24	0	1	1	0	0	0	180000-18FFFF
SA25	0	1	1	0	0	1	190000-19FFFF
SA26	0	1	1	0	1	0	1A0000-1AFFFF
SA27	0	1	1	0	1	1	1B0000-1BFFFF
SA28	0	1	1	1	0	0	1C0000-1CFFFF
SA29	0	1	1	1	0	1	1D0000-1DFFFF
SA30	0	1	1	1	1	0	1E0000-1EFFFF
SA31	0	1	1	1	1	1	1F0000-1FFFFF
SA32	1	0	0	0	0	0	200000-20FFFF
SA33	1	0	0	0	0	1	210000-21FFFF
SA34	1	0	0	0	1	0	220000-22FFFF
SA35	1	0	0	0	1	1	230000-23FFFF
SA36	1	0	0	1	0	0	240000-24FFFF
SA37	1	0	0	1	0	1	250000-25FFFF



MX29LV033M

Sector	A21	A20	A19	A18	A17	A16	8-bit Address Range (in hexadecimal)
SA38	1	0	0	1	1	0	260000-26FFFF
SA39	1	0	0	1	1	1	270000-27FFFF
SA40	1	0	1	0	0	0	280000-28FFFF
SA41	1	0	1	0	0	1	290000-29FFFF
SA42	1	0	1	0	1	0	2A0000-2AFFFF
SA43	1	0	1	0	1	1	2B0000-2BFFFF
SA44	1	0	1	1	0	0	2C0000-2CFFFF
SA45	1	0	1	1	0	1	2D0000-2DFFFF
SA46	1	0	1	1	1	0	2E0000-2EFFFF
SA47	1	0	1	1	1	1	2F0000-2FFFFF
SA48	1	1	0	0	0	0	300000-30FFFF
SA49	1	1	0	0	0	1	310000-31FFFF
SA50	1	1	0	0	1	0	320000-32FFFF
SA51	1	1	0	0	1	1	330000-33FFFF
SA52	1	1	0	1	0	0	340000-34FFFF
SA53	1	1	0	1	0	1	350000-35FFFF
SA54	1	1	0	1	1	0	360000-36FFFF
SA55	1	1	0	1	1	1	370000-37FFFF
SA56	1	1	1	0	0	0	380000-38FFFF
SA57	1	1	1	0	0	1	390000-39FFFF
SA58	1	1	1	0	1	0	3A0000-3AFFFF
SA59	1	1	1	0	1	1	3B0000-3BFFFF
SA60	1	1	1	1	0	0	3C0000-3CFFFF
SA61	1	1	1	1	0	1	3D0000-3DFFFF
SA62	1	1	1	1	1	0	3E0000-3EFFFF
SA63	1	1	1	1	1	1	3F0000-3FFFFF



MX29LV033M Sector Group Protection Address Table

Sector Group	A21-A17
SA0-SA3	00000
SA4-SA7	00001
SA8-SA11	00010
SA12-SA15	00011
SA16-SA19	00100
SA20-SA23	00101
SA24-SA27	00110
SA28-SA31	00111
SA32-SA35	01000
SA36-SA39	01001
SA40-SA43	01010
SA44-SA47	01011
SA48-SA51	01100
SA52-SA55	01101
SA56-SA59	01110
SA60-SA63	01111

Table 1. BUS OPERATION (1)

Operation	CE#	OE#	WE#	RESET#	ACC	Address	Q0~Q7
Read	L	L	H	H	X	A _{IN}	D _{OUT}
Write (Program/Erase)	L	H	L	H	X	A _{IN}	(Note 3)
Accelerated Program	L	H	L	H	V _{HH}	A _{IN}	(Note 3)
Standby	VCC±0.3V	X	X	VCC±0.3V	H	X	High-Z
Output Disable	L	H	H	H	X	X	High-Z
Reset	X	X	X	L	X	X	High-Z
Sector Group Protect (Note 2)	L	H	L	V _{ID}	X	Sector Addresses, A6=L,A3=L, A2=L, A1=H,A0=L	(Note 3)
Chip unprotect (Note 2)	L	H	L	V _{ID}	X	Sector Addresses, A6=H, A3=L, A2=L, A1=H, A0=L	(Note 3)
Temporary Sector Group Unprotect	X	X	X	V _{ID}	X	A _{IN}	(Note 3)

Legend:

L=Logic LOW=V_{IL}, H=Logic High=V_{IH}, V_{ID}=12.0 ±0.5V, V_{HH}=12.0 ±0.5V, X=Don't Care, A_{IN}=Address IN, D_{IN}=Data IN, D_{OUT}=Data OUT

Notes:

1. Address are A21:A0. Sector addresses are A21:A16.
2. The sector group protect and chip unprotect functions may also be implemented via programming equipment. See the "Sector Group Protection and Chip Unprotect" section.
3. D_{IN} or D_{OUT} as required by command sequence, Data# polling or sector protect algorithm (see Figure 15).

Table 2. AUTOSELECT CODES (High Voltage Method)

Description		CE#	OE#	WE#	A21 to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	Q7 to Q0
Manufacturer ID		L	L	H	X	X	VID	X	L	X	L	L	L	C2h
29LV033M	Cycle 1	L	L	H	X	X	VID	X	L	X	L	L	H	7Eh
	Cycle 2										H	H	L	1Ch
	Cycle 3										H	H	H	00h
Sector Protection Verification		L	L	H	SA	X	VID	X	L	X	L	H	L	01h (protected), 00h (unprotected)
Secured Silicon Sector Indicator Bit (Q7)		L	L	H	X	X	VID	X	L	X	L	H	H	90h (factory locked), 10h (not factory locked)

Legend: L = Logic Low = VIL, H = Logic High = VIH, SA = Sector Address, X = Don't care.

REQUIREMENTS FOR READING ARRAY DATA

To read array data from the outputs, the system must drive the CE# and OE# pins to VIL. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at VIH.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid address on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

PAGE MODE READ

The MX29LV033M offers "fast page mode read" function. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 bytes. The appropriate page is selected by the higher address bits A-1~A1. This is an asynchronous operation; the microprocessor supplies the specific word location.

The system performance could be enhanced by initiating 1 normal read and 7 fast page read. When CE# is deasserted and reasserted for a subsequent access, the access time is tACC or tCE. Fast page mode accesses are obtained by keeping the "read-page addresses" constant and changing the "intra-read page" addresses.

WRITING COMMANDS/COMMAND SEQUENCES

To program data to the device or erase sectors of memory, the system must drive WE# and CE# to VIL, and OE# to VIH.

An erase operation can erase one sector, multiple sectors, or the entire device. Table indicates the address space that each sector occupies. A "sector address" consists of the address bits required to uniquely select a sector. The "Writing specific address and data commands

or sequences into the command register initiates device operations. Table 1 defines the valid register command sequences. Writing incorrect address and data values or writing them in the improper sequence resets the device to reading array data. Section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

After the system writes the Automatic Select command sequence, the device enters the Automatic Select mode. The system can then read Automatic Select codes from the internal register (which is separate from the memory array) on Q7-Q0. Standard read cycle timings apply in this mode. Refer to the Automatic Select Mode and Automatic Select Command Sequence section for more information.

ICC2 in the DC Characteristics table represents the active current specification for the write mode. The "AC Characteristics" section contains timing specification table and timing diagrams for write operations.

WRITE BUFFER

Write Buffer Programming allows the system to write a maximum of 32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See "Write Buffer" for more information.

ACCELERATED PROGRAM OPERATION

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts VHH on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing VHH from the ACC pin must not be at VHH for operations other than accelerated programming, or device damage may result.

STANDBY MODE

When using both pins of CE# and RESET#, the device enter CMOS Standby with both pins held at $V_{CC} \pm 0.3V$. If CE# and RESET# are held at V_{IH} , but not within the range of $V_{CC} \pm 0.3V$, the device will still be in the standby mode, but the standby current will be larger. During Auto Algorithm operation, V_{CC} active current ($ICC2$) is required even CE# = "H" until the operation is completed. The device can be read with standard access time (t_{CE}) from either of these standby modes, before it is ready to read data.

AUTOMATIC SLEEP MODE

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when address remain stable for $t_{ACC} + 30ns$. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. $ICC4$ in the DC Characteristics table represents the automatic sleep mode current specification.

OUTPUT DISABLE

With the OE# input at a logic high level (V_{IH}), output from the devices are disabled. This will cause the output pins to be in a high impedance state.

RESET# OPERATION

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP} , the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3V$, the device draws CMOS standby current ($ICC4$). If RESET# is held at V_{IL}

but not within $V_{SS} \pm 0.3V$, the standby current will be greater.

The RESET# pin may be tied to system reset circuitry. A system reset would that also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a "0" (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH} .

Refer to the AC Characteristics tables for RESET# parameters and to Figure 3 for the timing diagram.

SECTOR GROUP PROTECT OPERATION

The MX29LV033M features hardware sector group protection. This feature will disable both program and erase operations for these sector group protected. In this device, a sector group consists of four adjacent sectors which are protected or unprotected at the same time. To activate this mode, the programming equipment must force VID on address pin A9 and control pin OE#, (suggest VID = 12V) A6 = V_{IL} and CE# = V_{IL} . (see Table 2) Programming of the protection circuitry begins on the falling edge of the WE# pulse and is terminated on the rising edge. Please refer to sector group protect algorithm and waveform.

MX29LV033M also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

To verify programming of the protection circuitry, the programming equipment must force VID on address pin A9 (with CE# and OE# at V_{IL} and WE# at V_{IH}). When A1=1, it will produce a logical "1" code at device output Q0 for a protected sector. Otherwise the device will produce 00H for the unprotected sector. In this mode, the addresses, except for A1, are don't care. Address locations with A1 = V_{IL} are reserved to read manufacturer and device codes. (Read Silicon ID)

It is also possible to determine if the group is protected in the system by writing a Read Silicon ID command. Performing a read operation with A1=VIH, it will produce a logical "1" at Q0 for the protected sector.

CHIP UNPROTECT OPERATION

The MX29LV033M also features the chip unprotect mode, so that all sectors are unprotected after chip unprotect is completed to incorporate any changes in the code. It is recommended to protect all sectors before activating chip unprotect mode.

To activate this mode, the programming equipment must force VID on control pin OE# and address pin A9. The CE# pins must be set at VIL. Pins A6 must be set to VIH. (see Table 2) Refer to chip unprotect algorithm and waveform for the chip unprotect algorithm. The unprotect mechanism begins on the falling edge of the WE# pulse and is terminated on the rising edge.

MX29LV033M also provides another method. Which requires VID on the RESET# only. This method can be implemented either in-system or via programming equipment. This method uses standard microprocessor bus cycle timing.

It is also possible to determine if the chip is unprotect in the system by writing the Read Silicon ID command. Performing a read operation with A1=VIH, it will produce 00H at data outputs (Q0-Q7) for an unprotect sector. It is noted that all sectors are unprotected after the chip unprotect algorithm is completed.

TEMPORARY SECTOR GROUP UNPROTECT OPERATION

This feature allows temporary unprotect of previously protected sector to change data in-system. The Temporary Sector Unprotect mode is activated by setting the RESET# pin to VID(11.5V-12.5V). During this mode, formerly protected sectors can be programmed or erased as unprotect sector. Once VID is remove from the RESET# pin, all the previously protected sectors are protected again.

SILICON ID READ OPERATION

Flash memories are intended for use in applications where

the local CPU alters memory contents. As such, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not generally desired system design practice.

MX29LV033M provides hardware method to access the silicon ID read operation. Which method requires VID on A9 pin, VIL on CE#, OE#, A6, and A1 pins. Which apply VIL on A0 pin, the device will output MXIC's manufacture code. Which apply VIH on A0 pin, the device will output MX29LV033M device code.

VERIFY SECTOR GROUP PROTECT STATUS OPERATION

MX29LV033M provides hardware method for sector group protect status verify. Which method requires VID on A9 pin, VIH on WE# and A1 pins, VIL on CE#, OE#, A6, and A0 pins, and sector address on A16 to A21 pins. Which the identified sector is protected, the device will output 01H. Which the identified sector is not protect, the device will output 00H.

DATA PROTECTION

The MX29LV033M is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transition. During power up the device automatically resets the state machine in the Read mode. In addition, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences. The device also incorporates several features to prevent inadvertent write cycles resulting from VCC power-up and power-down transition or system noise.

SECURED SILICON SECTOR

The MX29LV033M features a OTP memory region where the system may access through a command sequence to create a permanent part identification as so called Electronic Serial Number (ESN) in the device. Once this region is programmed, any further modification on the region is impossible. The secured silicon sector is a 256 bytes in length, and uses a Secured Silicon Sector Indi-

cator Bit (Q7) to indicate whether or not the Secured Silicon Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevent duplication of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The MX29LV033M offers the device with Secured Silicon Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory , and has the Secured Silicon Sector Indicator Bit permanently set to a "1". The customer-lockable version is shipped with the Secured Silicon Sector unprotected, allowing customers to utilize that sector in any form they prefer. The customer-lockable version has the secured sector Indicator Bit permanently set to a "0". Therefore, the Secured Silicon Sector Indicator Bit prevents customer, lockable device from being used to replace devices that are factory locked.

The system access the Secured Silicon Sector through a command sequence (refer to "Enter Secured Silicon/ Exit Secured Silicon Sector command Sequence). After the system has written the Enter Secured Silicon Sector command sequence, it may read the Secured Silicon Sector by using the address normally occupied by the first sector SA0. Once entry the Secured Silicon Sector the operation of boot sectors is disabled but the operation of main sectors is as normally. This mode of operation continues until the system issues the Exit Secured Silicon Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending command to sector SA0.

Secured Silicon Sector address range	ESN factory locked	Customer lockable
000000h-00000Fh	ESN	Determined by
000010h-0000FFh	Unavailable	Customer

FACTORY LOCKED:Secured Silicon Sector Programmed and Protected At the Factory

In device with an ESN, the Secured Silicon Sector is protected when the device is shipped from the factory. The Secured Silicon Sector cannot be modified in any

way. A factory locked device has an 16-byte random ESN at address 000000h-00000Fh.

CUSTOMER LOCKABLE:Secured Silicon Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 256 bytes Secured Silicon Sector. Programming and protecting the Secured Silicon Sector must be used with caution since, once protected, there is no procedure available for unprotected the Secured Silicon Sector area and none of the bits in the Secured Silicon Sector memory space can be modified in any way.

The Secured Silicon Sector area can be protected using one of the following procedures:

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 15, except that RESET# may be at either VIH or VID. This allows in-system protection of the Secured Silicon Sector without raising any device pin to a high voltage. Note that method is only applicable to the Secured Silicon Sector.

Write the three-cycle Enter Secured Silicon Sector Region command sequence, and then alternate method of sector protection described in the :Sector Group Protection and Unprotect" section.

Once the Secured Silicon Sector is programmed, locked and verified, the system must write the Exit Secured Silicon Sector Region command sequence to return to reading and writing the remainder of the array.

LOW VCC WRITE INHIBIT

When VCC is less than VLKO the device does not accept any write cycles. This protects data during VCC power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets. Subsequent writes are ignored until VCC is greater than VLKO. The system must provide the proper signals to the control pins to prevent unintentional write when VCC is greater than VLKO.

WRITE PULSE "GLITCH" PROTECTION

Noise pulses of less than 5ns (typical) on CE# or WE# will not initiate a write cycle.

LOGICAL INHIBIT

Writing is inhibited by holding any one of OE# = VIL, CE# = VIH or WE# = VIH. To initiate a write cycle CE# and WE# must be a logical zero while OE# is a logical one.

POWER-UP SEQUENCE

The MX29LV033M powers up in the Read only mode. In addition, the memory contents may only be altered after successful completion of the predefined command sequences.

POWER-UP WRITE INHIBIT

If WE#=CE#=VIL and OE#=VIH during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

POWER SUPPLY DE COUPLING

In order to reduce power switching effect, each device should have a 0.1uF ceramic capacitor connected between its VCC and GND.

SOFTWARE COMMAND DEFINITIONS

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode. Table 3 defines the valid register command sequences. Note that the Erase Suspend (B0H) and

Erase Resume (30H) commands are valid only while the Sector Erase operation is in progress. Either of the two reset command sequences will reset the device (when applicable).

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data are latched on rising edge of WE# or CE#, whichever happens first.

TABLE 3. MX29LV033M COMMAND DEFINITIONS

Command	Bus Cycles	First Bus Cycle		Second Bus Cycle		Third Bus Cycle		Fourth Bus Cycle		Fifth Bus Cycle		Sixth Bus Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)	1	RA	RD										
Reset (Note 6)	1	XXX	F0										
Automatic Select (Note 7)													
Manufacturer ID	4	XXX	AA	XXX	55	XXX	90	X00	C2H				
Device ID (Note 8)	4	XXX	AA	XXX	55	XXX	90	X01	7E	X0E	1Ch	X0F	00
Secured Sector Factory Protect	4	XXX	AA	XXX	55	XXX	90	X03					
Sector Group Protect Verify (Note 9)	4	XXX	AA	XXX	55	XXX	90	(SA)X02	00/01				
Enter Secured Silicon Sector	3	XXX	AA	XXX	55	XXX	88						
Exit Secured Silicon Sector	4	XXX	AA	XXX	55	XXX	90	XXX	00				
Program	4	XXX	AA	XXX	55	XXX	A0	PA	PD				
Write to Buffer (Note 10)	6	XXX	AA	XXX	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash	1	SA	29										
Write to Buffer Abort	3	XXX	AA	XXX	55	XXX	F0						
Reset (Note 11)													
Chip Erase	6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	XXX	10
Sector Erase	6	XXX	AA	XXX	55	XXX	80	XXX	AA	XXX	55	SA	30
Program/Erase Suspend (Note 12)	1	XXX	B0										
Program/Erase Resume (Note 13)	1	XXX	30										
CFI Query (Note 14)	1	AA	98										

Legend:

X=Don't care

RA=Address of the memory location to be read.

RD=Data read from location RA during read operation.

PA=Address of the memory location to be programmed.

Addresses are latched on the falling edge of the WE# or CE# pulse, whichever happen later.

DDI=Data of device identifier

C2H for manufacture code

PD=Data to be programmed at location PA. Data is latched on the rising edge of WE# or CE# pulse.

SA=Address of the sector to be erase or verified (in autoselect mode).

Address bits A21-A12 uniquely select any sector.

WBL=Write Buffer Location. Address must be within the same write buffer page as PA.

BC=Byte Count. Number of write buffer locations to load minus 1.

Notes:

1. See Table 1 for descriptions of bus operations.
2. All values are in hexadecimal.
3. Except when reading array or automatic select data, all bus cycles are write operation.
4. Address bits are don't care for unlock and command cycles, except when PA or SA is required.
5. No unlock or command cycles required when device is in read mode.
6. The Reset command is required to return to the read mode when the device is in the automatic select mode or if Q5 goes high.
7. The fourth cycle of the automatic select command sequence is a read cycle.
8. The device ID must be read in three cycles.
9. The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.
10. The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.
11. Command sequence resets device for next command after aborted write-to-buffer operation.
12. The system may read and program functions in non-erasing sectors, or enter the automatic select mode, when in the erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.
13. The Erase Resume command is valid only during the Erase Suspend mode.
14. Command is valid when device is ready to read array data or when device is in automatic select mode.

READING ARRAY DATA

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is also ready to read array data after completing an Automatic Program or Automatic Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the Erase Suspend mode. The system can read array data using the standard read timings, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See Erase Suspend/Erase Resume Commands for more information on this mode. The system must issue the reset command to re-enable the device for reading array data if Q5 goes high, or while in the automatic select mode. See the "Reset Command" section, next.

RESET COMMAND

Writing the reset command to the device resets the device to reading array data. Address bits are don't care for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to reading array data. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to reading array data (also applies to programming in Erase Suspend mode). Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an SILICON ID READ command sequence. Once in the SILICON ID READ mode, the reset command must be written to return to reading array data (also applies to SILICON ID READ during Erase Suspend).

If Q5 goes high during a program or erase operation, writing the reset command returns the device to reading

array data (also applies during Erase Suspend).

SILICON ID READ COMMAND SEQUENCE

The SILICON ID READ command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. Table 2 shows the address and data requirements. This method is an alternative to that shown in Table 1, which is intended for PROM programmers and requires VID on address bit A9.

The SILICON ID READ command sequence is initiated by writing two unlock cycles, followed by the SILICON ID READ command. The device then enters the SILICON ID READ mode, and the system may read at any address any number of times, without initiating another command sequence. A read cycle at address XX00h retrieves the manufacturer code. A read cycle at address XX01h returns the device code. A read cycle containing a sector address (SA) and the address 02h returns 01h if that sector is protected, or 00h if it is unprotected. Refer to Table for valid sector addresses.

The system must write the reset command to exit the automatic select mode and return to reading array data.

BYTE PROGRAM COMMAND SEQUENCE

The command sequence requires four bus cycles, and is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically generates the program pulses and verifies the programmed cell margin. Table 3 shows the address and data requirements for the byte program command sequence.

When the Embedded Program algorithm is complete, the device then returns to reading array data and addresses are no longer latched. The system can determine the status of the program operation by using Q7, Q6, or RY/BY#. See "Write Operation Status" for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a hardware reset immediately terminates the programming op-

eration. The Byte Program command sequence should be reinitiated once the device has reset to reading array data, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. A bit cannot be programmed from a "0" back to a "1". Attempting to do so may halt the operation and set Q5 to "1", or cause the Data# Polling algorithm to indicate the operation was successful. However, a succeeding read will show that the data is still "0". Only erase operations can convert a "0" to a "1".

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 32 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits $A_{MAX}-4$. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be

decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. Q7, Q6, Q5, and Q1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by Q1 = 1, Q7 = DATA# (for the last address location loaded), Q6 = toggle, and Q5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any

non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15us maximum (5 us typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the Secured Silicon Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. See Write Operation Status for more information.

SETUP AUTOMATIC CHIP/SECTOR ERASE

Chip erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command 80H. Two more "unlock" write cycles are then followed by the chip erase command 10H, or the sector erase command 30H.

The MX29LV033M contains a Silicon-ID-Read operation to supplement traditional PROM programming methodology. The operation is initiated by writing the read silicon ID command sequence into the command register. Following the command write, a read cycle with A1=VIL,A0=VIL retrieves the manufacturer code. A read cycle with A1=VIL,A0=VIH retrieves the device code.

AUTOMATIC CHIP/SECTOR ERASE COMMAND

The device does not require the system to preprogram prior to erase. The Automatic Erase algorithm automatically pre-program and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 3 shows the address and data requirements for the chip erase command sequence.

Any commands written to the chip during the Automatic Erase algorithm are ignored. Note that a hardware reset during the chip erase operation immediately terminates the operation. The Chip Erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

The system can determine the status of the erase operation by using Q7, Q6, Q2, or RY/BY#. See "Write Operation Status" for information on these status bits. When the Automatic Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched.

Figure 10 illustrates the algorithm for the erase operation. See the Erase/Program Operations tables in "AC Characteristics" for parameters, and to Figure 9 for timing diagrams.

SECTOR ERASE COMMANDS

The Automatic Sector Erase does not require the device to be entirely pre-programmed prior to executing the Automatic Set-up Sector Erase command and Automatic Sector Erase command. Upon executing the Automatic Sector Erase command, the device will automatically program and verify the sector(s) memory for an all-zero data pattern. The system is not required to provide any control or timing during these operations.

When the sector(s) is automatically verified to contain an all-zero pattern, a self-timed sector erase and verify begin. The erase and verify operations are complete when the data on Q7 is "1" and the data on Q6 stops toggling for two consecutive read cycles, at which time the device returns to the Read mode. The system is not required to provide any control or timing during these operations.

When using the Automatic Sector Erase algorithm, note that the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verification command is required). Sector erase is a six-bus cycle operation. There are two "unlock" write cycles. These are followed by writing the set-up command 80H. Two more "unlock" write cycles are then followed by the sector erase command 30H. The sector address is latched on the falling edge of WE# or CE#, whichever happens later, while the command (data) is latched on the rising edge of WE# or CE#, whichever happens first. Sector addresses selected are loaded into internal register on the sixth falling edge of WE# or CE#, whichever happens later. Each successive sector load cycle started by the falling edge of WE# or CE#, whichever happens later must begin within 50us from the rising edge of the preceding WE# or CE#, whichever happens first. Otherwise, the loading period ends and internal auto sector erase cycle starts. (Monitor Q3 to determine if the sector erase timer window is still open, see section Q3, Sector Erase Timer.) Any command other than Sector Erase(30H) or Erase Suspend(B0H) during the time-out period resets the device to read mode.

ERASE SUSPEND

This command only has meaning while the state machine is executing Automatic Sector Erase operation, and therefore will only be responded during Automatic Sector Erase operation. When the Erase Suspend command is issued during the sector erase operation, the

device requires a maximum 20us to suspend the sector erase operation. However, When the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. After this command has been executed, the command register will initiate erase suspend mode. The state machine will return to read mode automatically after suspend is ready. At this time, state machine only allows the command register to respond to the Erase Resume, program data to, or read data from any sector not selected for erasure.

The system can determine the status of the program operation using the Q7 or Q6 status bits, just as in the standard program operation. After an erase-suspend program operation is complete, the system can once again read array data within non-suspended blocks.

ERASE RESUME

This command will cause the command register to clear the suspend state and return back to Sector Erase mode but only if an Erase Suspend command was previously issued. Erase Resume will not have any effect in all other conditions. Another Erase Suspend command can be written after the chip has resumed erasing.

QUERY COMMAND AND COMMON FLASH INTERFACE (CFI) MODE

MX29LV033M is capable of operating in the CFI mode. This mode all the host system to determine the manufacturer of the device such as operating parameters and configuration. Two commands are required in CFI mode. Query command of CFI mode is placed first, then the Reset command exits CFI mode. These are described in Table 4.

The single cycle Query command is valid only when the device is in the Read mode, including Erase Suspend, Standby mode, and Read ID mode; however, it is ignored otherwise.

The Reset command exits from the CFI mode to the Read mode, or Erase Suspend mode, or read ID mode. The command is valid only when the device is in the CFI mode.

Table 4-1. CFI mode: Identification Data Values

(All values in these tables are in hexadecimal)

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "QRY"	10	20	51
	11	22	52
	12	24	59
Primary vendor command set and control interface ID code	13	26	02
	14	28	00
Address for primary algorithm extended query table	15	2A	40
	16	2C	00
Alternate vendor command set and control interface ID code (none)	17	2E	00
	18	30	00
Address for secondary algorithm extended query table (none)	19	32	00
	1A	34	00

Table 4-2. CFI Mode: System Interface Data Values

Description	Address h (x16)	Address h (x8)	Data h
VCC supply, minimum (2.7V)	1B	36	27
VCC supply, maximum (3.6V)	1C	38	36
VPP supply, minimum (none)	1D	3A	00
VPP supply, maximum (none)	1E	3C	00
Typical timeout for single word/byte write (2^N us)	1F	3E	07
Typical timeout for maximum size buffer write (2^N us)	20	40	07
Typical timeout for individual block erase (2^N ms)	21	42	0A
Typical timeout for full chip erase (2^N ms)	22	44	00
Maximum timeout for single word/byte write times (2^N X Typ)	23	46	01
Maximum timeout for maximum size buffer write times (2^N X Typ)	24	48	05
Maximum timeout for individual block erase times (2^N X Typ)	25	4A	04
Maximum timeout for full chip erase times (not supported)	26	4C	00

Table 4-3. CFI Mode: Device Geometry Data Values

Description	Address h (x16)	Address h (x8)	Data h
Device size (2 ⁿ bytes)	27	4E	16
Flash device interface code	28	50	00
	29	52	00
Maximum number of bytes in multi-byte write = 2 ⁿ	2A	54	05
	2B	56	00
Number of erase block regions	2C	58	01
Erase block region 1 information	2D	5A	3F
[2E, 2D] = # of blocks in region -1	2E	5C	00
[30, 2F] = size in multiples of 256-bytes	2F	5E	00
	30	60	01
Erase Block Region 2 Information (refer to CFI publication 100)	31	62	00
	32	64	00
	33	66	00
	34	68	00
Erase Block Region 3 Information (refer to CFI publication 100)	35	6A	00
	36	6C	00
	37	6E	00
	38	70	00
Erase Block Region 4 Information (refer to CFI publication 100)	39	72	00
	3A	74	00
	3B	76	00
	3C	78	00

Table 4-4. CFI Mode: Primary Vendor-Specific Extended Query Data Values

Description	Address h (x16)	Address h (x8)	Data h
Query-unique ASCII string "PRI"	40	80	50
	41	82	52
	42	84	49
Major version number, ASCII	43	86	31
Minor version number, ASCII	44	88	33
Address sensitive unlock (0=required, 1= not required)	45	8A	01
Erase suspend (2= to read and write)	46	8C	02
Sector protect (N= # of sectors/group)	47	8E	04
Temporary sector unprotect (1=supported)	48	90	01
Sector protect/unprotect scheme	49	92	04
Simultaneous R/W operation (0=not supported)	4A	94	00
Burst mode type (0=not supported)	4B	96	00
Page mode type (1= 8 byte page)	4C	98	01
ACC (Acceleration) Supply Minimum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4D	9A	B5
ACC (Acceleration) Supply Maximum 00h=Not Supported, D7-D4: Volt, D3-D0:100mV	4E	9C	C5
Top/Bottom Boot Sector Flag 00h=Uniform Device without WP# support 02h=Bottom Boot Device, 03h=Top Boot Device 04h=uniform sectors bottom WP# protect, 05h=uniform sectors top WP# protect	4F	9E	00
Program Suspend 00h=Not Supported, 01h=Supported	50	A0	01

WRITE OPERATION STATUS

The device provides several bits to determine the status of a write operation: Q2, Q3, Q5, Q6, Q7, and RY/BY#. Table 5 and the following subsections describe the functions of these bits. Q7, RY/BY#, and Q6 each offer a method for determining whether a program or erase operation is complete or in progress. These three bits are discussed first.

Table 5. Write Operation Status

Status		Q7	Q6	Q5	Q3	Q2	Q1	RY/BY#
Byte Program in Auto Program Algorithm		Q7#	Toggle	0	N/A	No Toggle	0	0
Auto Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Erase Suspended Mode	Erase Suspend Read (Erase Suspended Sector)	1	No Toggle	0	N/A	Toggle	N/A	1
	Erase Suspend Read (Non-Erase Suspended Sector)	Data	Data	Data	Data	Data	Data	1
	Erase Suspend Program	Q7#	Toggle	0	N/A	N/A	N/A	0
Program Suspend	Program-Suspended Read (Program-Suspended Sector)	Invalid (not allowed)						1
	Program-Suspended Read (Non-Program-Suspended Sector)	Data						1
Write-to-Buffer	Busy	Q7#	Toggle	0	N/A	N/A	0	0
	Abort	Q7#	Toggle	0	N/A	N/A	1	0

Notes:

1. Q5 switches to "1" when an Byte Program, Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on Q5 for more information.
2. Q7 and Q2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
3. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
4. Q1 switches to "1" when the device has aborted the write-to-buffer operation.

Q7: Data# Polling

The Data# Polling bit, Q7, indicates to the host system whether an Automatic Algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the program or erase command sequence.

During the Automatic Program algorithm, the device outputs on Q7 the complement of the datum programmed to Q7. This Q7 status also applies to programming during Erase Suspend. When the Automatic Program algorithm is complete, the device outputs the datum programmed to Q7. The system must provide the program address to read valid status information on Q7. If a program address falls within a protected sector, Data# Polling on Q7 is active for approximately 1 us, then the device returns to reading array data.

During the Automatic Erase algorithm, Data# Polling produces a "0" on Q7. When the Automatic Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a "1" on Q7. This is analogous to the complement/true datum output described for the Automatic Program algorithm: the erase function changes all the bits in a sector to "1" prior to this, the device outputs the "complement," or "0". The system must provide an address within any of the sectors selected for erasure to read valid status information on Q7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on Q7 is active for approximately 100 us, then the device returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

When the system detects Q7 has changed from the complement to true data, it can read valid data at Q7-Q0 on the following read cycles. This is because Q7 may change asynchronously with Q0-Q6 while Output Enable (OE#) is asserted low.

Q6:Toggle Bit I

Toggle Bit I on Q6 indicates whether an Automatic Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# or CE#, whichever

happens first pulse in the command sequence (prior to the program or erase operation), and during the sector time-out.

During an Automatic Program or Erase algorithm operation, successive read cycles to any address cause Q6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, Q6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, Q6 toggles for 100us and returns to reading array data. If not all selected sectors are protected, the Automatic Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use Q6 and Q2 together to determine whether a sector is actively erasing or is erase suspended. When the device is actively erasing (that is, the Automatic Erase algorithm is in progress), Q6 toggling. When the device enters the Erase Suspend mode, Q6 stops toggling. However, the system must also use Q2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use Q7.

If a program address falls within a protected sector, Q6 toggles for approximately 2us after the program command sequence is written, then returns to reading array data.

Q6 also toggles during the erase-suspend-program mode, and stops toggling once the Automatic Program algorithm is complete.

Table 5 shows the outputs for Toggle Bit I on Q6.

Q2:Toggle Bit II

The "Toggle Bit II" on Q2, when used with Q6, indicates whether a particular sector is actively erasing (that is, the Automatic Erase algorithm is in process), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# or CE#, whichever happens first pulse in the command sequence.

Q2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But Q2 cannot distinguish whether the sector is actively erasing or is erase-suspended. Q6, by com-

parison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sectors and mode information. Refer to Table 5 to compare outputs for Q2 and Q6.

Reading Toggle Bits Q6/ Q2

Whenever the system initially begins reading toggle bit status, it must read Q7-Q0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on Q7-Q0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of Q5 is high (see the section on Q5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as Q5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not complete the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that system initially determines that the toggle bit is toggling and Q5 has not gone high. The system may continue to monitor the toggle bit and Q5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation.

Q5:Program/Erase Timing

Q5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions Q5 will produce a "1". This time-out condition indicates that the program or erase cycle was not successfully completed. Data# Polling and Toggle Bit are the only operating functions of the device under this condition.

If this time-out condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this time-out condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this time-out condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The time-out condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Automatic Algorithm operation. Hence, the system never reads a valid data on Q7 bit and Q6 never stops toggling. Once the Device has exceeded timing limits, the Q5 bit will indicate a "1". Please note that this is not a device failure condition since the device was incorrectly used.

The Q5 failure condition may appear if the system tries to program a to a "1" location that is previously programmed to "0". Only an erase operation can change a "0" back to a "1". Under this condition, the device halts the operation, and when the operation has exceeded the timing limits, Q5 produces a "1".

Q3:Sector Erase Timer

After the completion of the initial sector erase command sequence, the sector erase time-out will begin. Q3 will remain low until the time-out is complete. Data# Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data# Polling or the Toggle Bit indicates the device has been written with a valid erase command, Q3 may be used to determine if the sector erase timer window is still open. If Q3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data# Polling or Toggle Bit. If Q3 is low ("0"), the device will accept addi-

tional sector erase commands. To insure the command has been accepted, the system software should check the status of Q3 prior to and following each subsequent sector erase command. If Q3 were high on the second status check, the command may not have been accepted.

If the time between additional erase commands from the system can be less than 50us, the system need not to monitor Q3.

Q1: Write-to-Buffer Abort

Q1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions Q1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer section for more details.

RY/BY#:READY/BUSY OUTPUT

The RY/BY# is a dedicated, open-drain output pin that indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to VCC .

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is ready to read array data (including during the Erase Suspend mode), or is in the standby mode.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature

Plastic Packages -65°C to +150°C

Ambient Temperature

with Power Applied. -65°C to +125°C

Voltage with Respect to Ground

VCC (Note 1) -0.5 V to +4.0 V
A9, OE#, and

RESET# (Note 2) -0.5 V to +12.5 V

All other pins (Note 1) -0.5 V to VCC +0.5 V

Output Short Circuit Current (Note 3) 200 mA

Notes:

1. Minimum DC voltage on input or I/O pins is -0.5 V.
During voltage transitions, input or I/O pins may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is VCC +0.5 V.
During voltage transitions, input or I/O pins may overshoot to VCC +2.0 V for periods up to 20ns.
2. Minimum DC input voltage on pins A9, OE#, and RESET# is -0.5 V. During voltage transitions, A9, OE#, and RESET# may overshoot VSS to -2.0 V for periods of up to 20 ns. Maximum DC input voltage on pin A9 is +12.5 V which may overshoot to 14.0 V for periods up to 20 ns.
3. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RATINGS**Commercial (C) Devices**

Ambient Temperature (T_A) 0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) -40°C to +85°C

V_{CC} Supply Voltages

VCC for full voltage range. +2.7 V to 3.6 V

VCC for regulated voltage range. +3.0 V to 3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

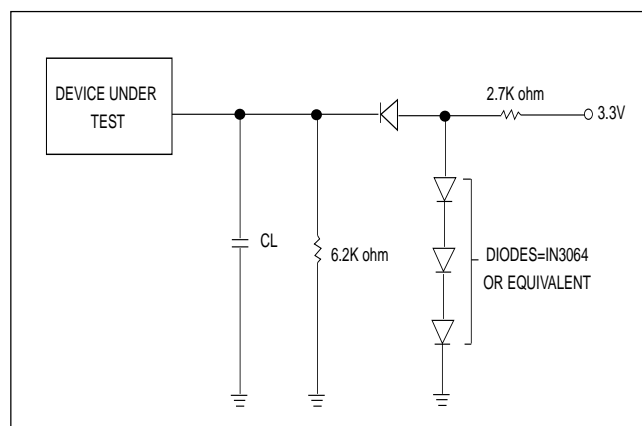
DC CHARACTERISTICS

TA=-40° C to 85° C, VCC=2.7V~3.6V (TA= 0° C to 70° C, VCC=3.0V~3.6V for 70R)

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Unit
I LI	Input Load Current (Note 1)	VIN = VSS to VCC , VCC = VCC max				±1.0	uA
I LIT	A9 Input Leakage Current	VCC=VCC max; A9 = 12.5V				35	uA
I LO	Output Leakage Current	VOUT = VSS to VCC , VCC= VCC max				±1.0	uA
ICC1	VCC Active Read Current (Notes 2,3)	CE#= VIL, OE# = VIH	10 MHz		35	50	mA
			5 MHz		18	25	mA
			1 MHz		5	20	mA
ICC2	VCC Intra-Page Read Current (Notes 2,3)	CE#= VIL , OE# = VIH	10 MHz		5	20	mA
			40 MHz		10	40	mA
ICC3	VCC Active Write Current (Notes 2,3)	CE#= VIL , OE# = VIH WE#=VIL			50	60	mA
ICC4	VCC Standby Current (Note 2)	CE#,RESET#=VCC±0.3V			20	50	uA
ICC5	VCC Reset Current (Note 2)	RESET#=VSS±0.3V			20	50	uA
ICC6	Automatic Sleep Mode (Notes 2,4)	VIL = V SS ± 0.3 V, VIH = VCC ± 0.3 V,			20	50	uA
VIL	Input Low Voltage			-0.5		0.8	V
VIH	Input High Voltage			0.7xVCC		VCC+0.5	V
VHH	Voltage for ACC Program Acceleration	VCC = 2.7V ~ 3.6V		11.5	12.0	12.5	V
VID	Voltage for Autoselect and Temporary Sector Unprotect	VCC = 3.0 V ± 10%		11.5	12.0	12.5	V
VOL	Output Low Voltage	IOL= 4.0mA,VCC=VCC min				0.45	V
VOH1	Output High Voltage	IOH=-2.0mA,VCC=VCC min		0.85VCC			V
VOH2		IOH=-100uA,VCC=VCC min		VCC-0.4			V
VLKO	Low VCC Lock-Out Voltage (Note 5)			2.3		2.5	V






Notes:

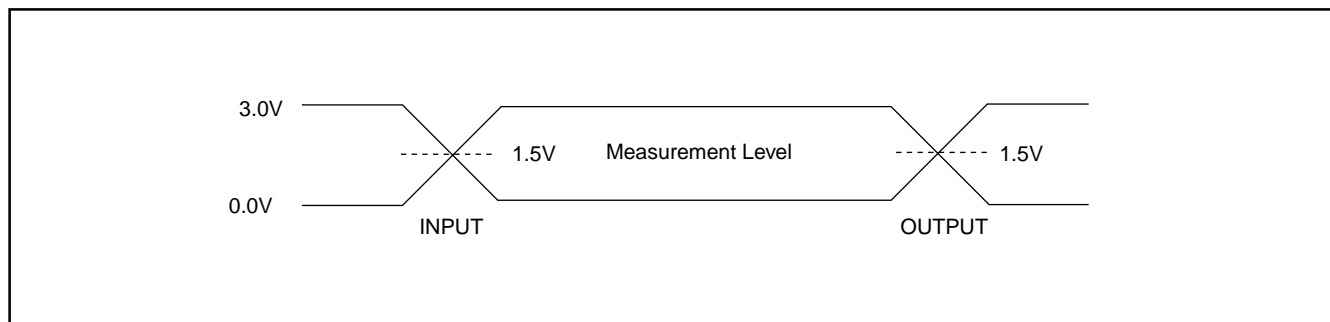
1. The ICC current listed is typically is less than 2 mA/MHz, with OE# at VIH. Typical specifications are for VCC = 3.0V.
2. Maximum ICC specifications are tested with VCC = VCC max.
3. ICC active while Embedded Erase or Embedded Program is in progress.
4. Automatic sleep mode enables the low power mode when addresses remain stable for t ACC + 30 ns.
5. Not 100% tested.
6. A9=12.5V when TA=0° C to 85° C, A9=12V when when TA=-40° C to 0° C.

SWITCHING TEST CIRCUITS

TEST SPECIFICATIONS

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, CL (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0-3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State(High Z)

SWITCHING TEST WAVEFORMS


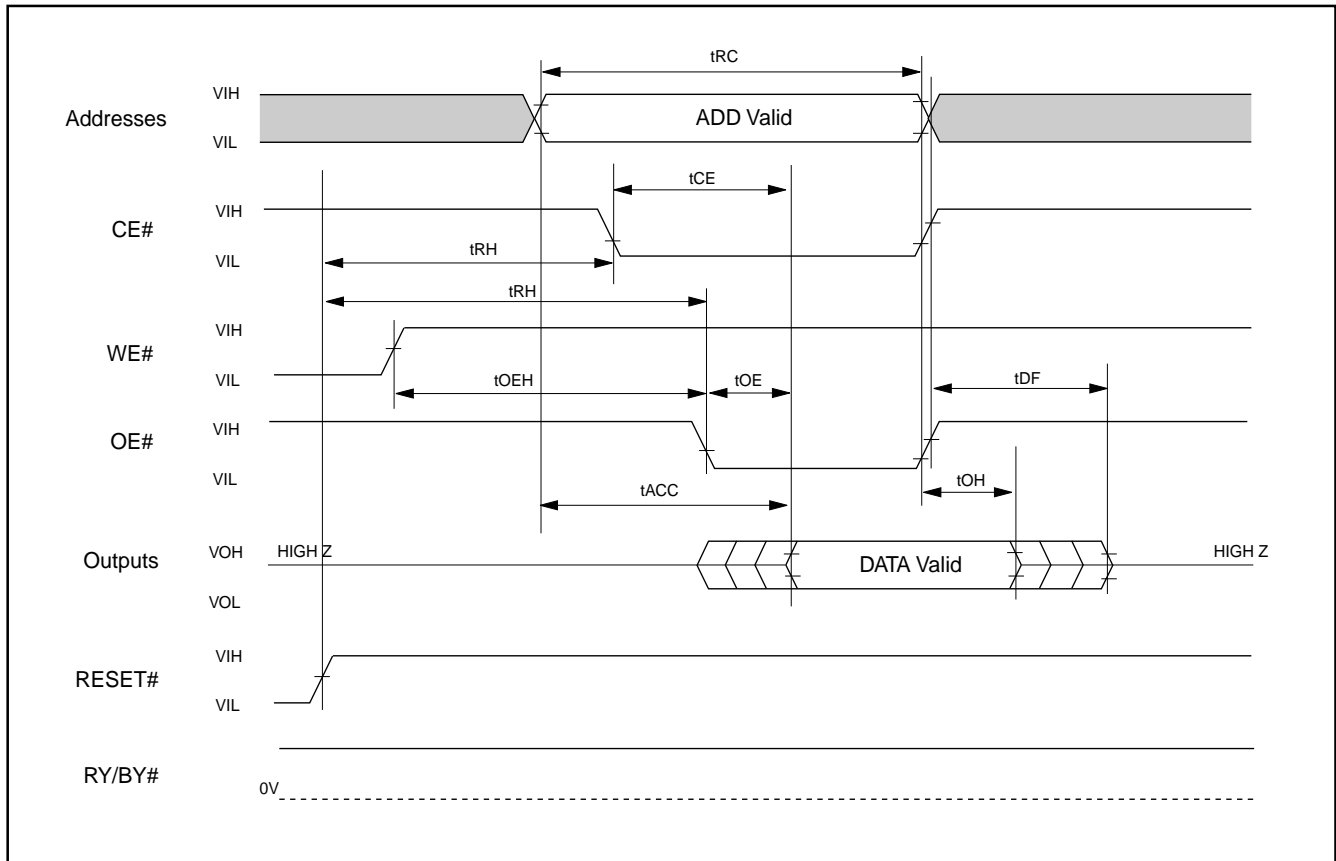
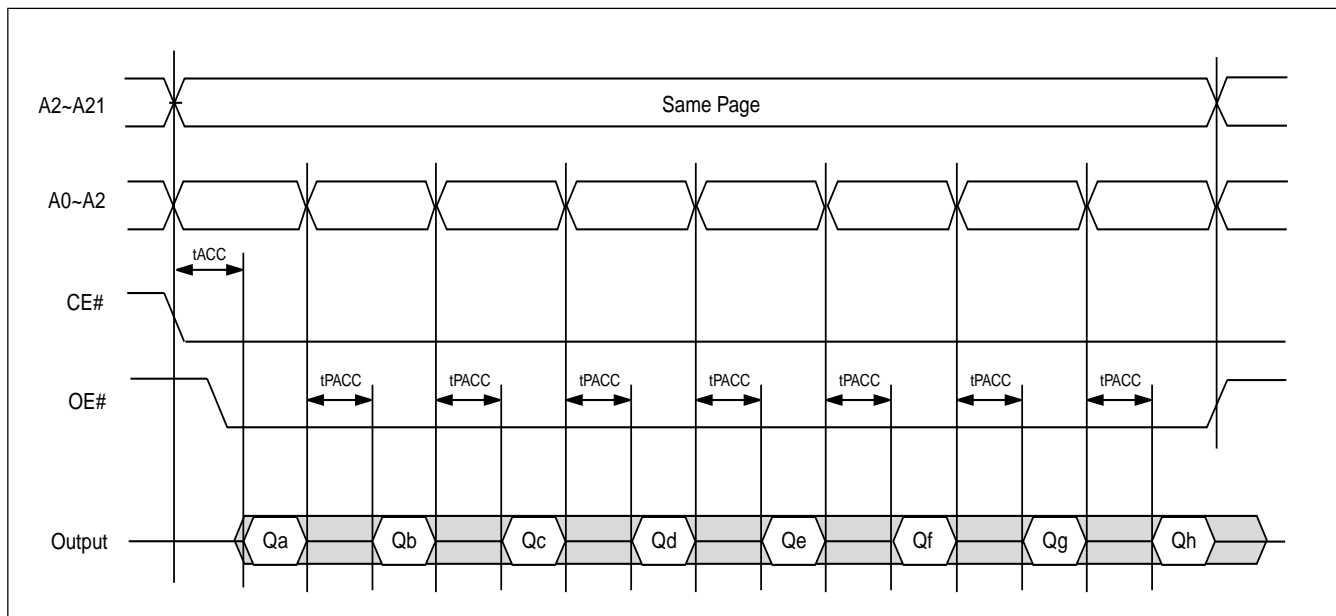
AC CHARACTERISTICS**Read-Only Operations****TA=-40° C to 85° C, VCC=2.7V~3.6V (TA= 0° C to 70° C, VCC=3.0V~3.6V for 70R)**

Parameter Std.	Description	Test Setup		Speed Options		Unit
				70R	90	
tRC	Read Cycle Time (Note 1)		Min	70	90	ns
tACC	Address to Output Delay	CE#, OE#=VIL	Max	70	90	ns
tCE	Chip Enable to Output Delay	OE#=VIL	Max	70	90	ns
tPACC	Page Access Time		Max	25	25	ns
tOE	Output Enable to Output Delay		Max	35	35	ns
tDF	Chip Enable to Output High Z (Note 1)		Max	16		ns
tDF	Output Enable to Output High Z (Note 1)		Max	16		ns
tOH	Output Hold Time From Address, CE# or OE#, whichever Occurs First		Min	0		ns
tOEH	Output Enable Hold Time (Note 1)	Read	Min	35		ns
		Toggle and Data# Polling	Min	10		ns

Notes:

1. Not 100% tested.

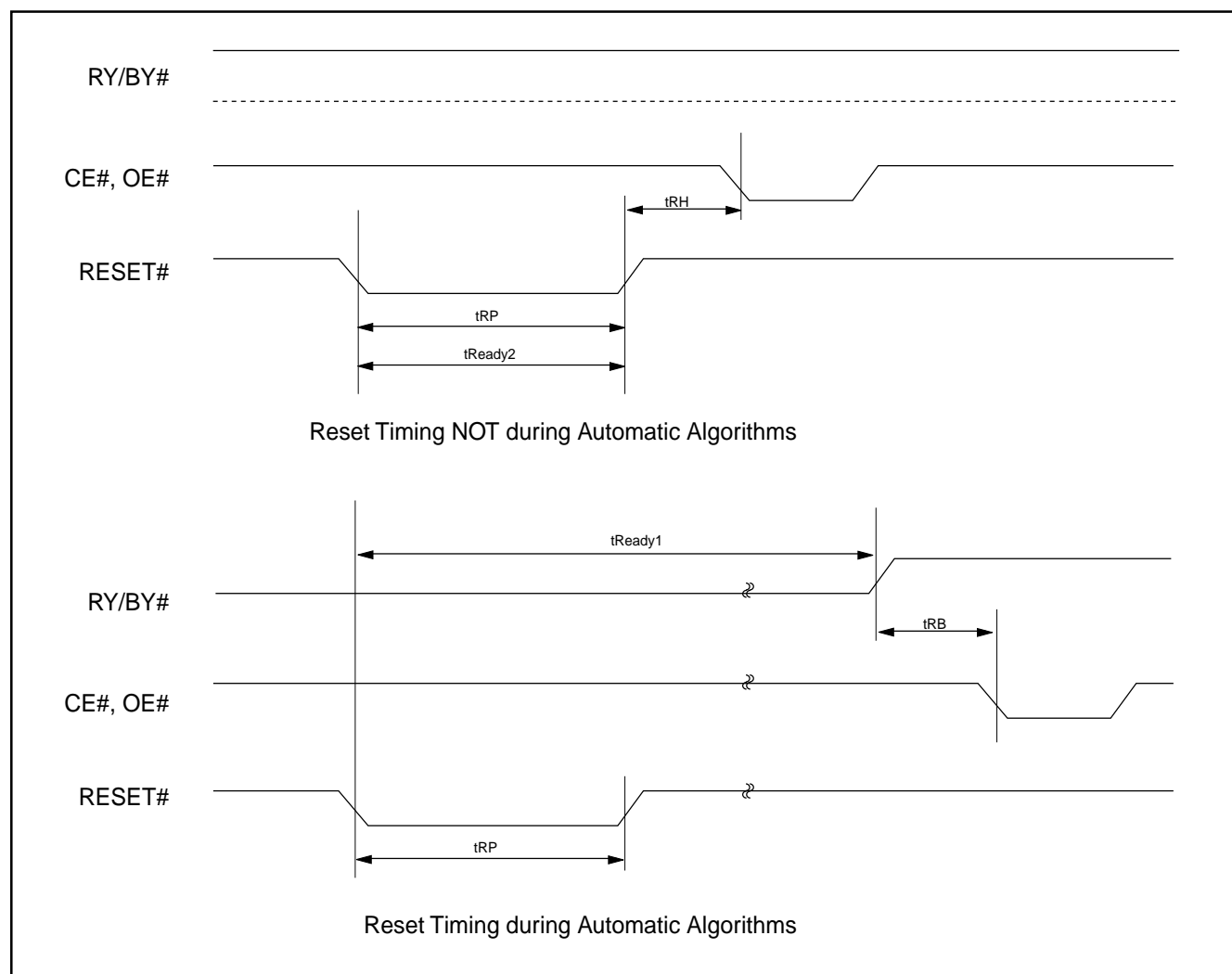
2. See SWITCHING TEST CIRCUITS and TEST SPECIFICATIONS TABLE for test specifications.

Figure 1. READ TIMING WAVEFORMS

Figure 2. PAGE READ TIMING WAVEFORMS


AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tREADY1	RESET# PIN Low (During Automatic Algorithms) to Read or Write (See Note)	MAX	20	us
tREADY2	RESET# PIN Low (NOT During Automatic Algorithms) to Read or Write (See Note)	MAX	500	ns
tRP	RESET# Pulse Width (NOT During Automatic Algorithms)	MIN	500	ns
tRH	RESET# High Time Before Read (See Note)	MIN	50	ns
tRB	RY/BY# Recovery Time(to CE#, OE# go low)	MIN	0	ns
tRPD	RESET# Low to Standby Mode	MIN	20	us

Note:Not 100% tested

Figure 3. RESET# TIMING WAVEFORM


AC CHARACTERISTICS

Erase and Program Operations

TA=-40° C to 85° C, VCC=2.7V~3.6V (TA= 0° C to 70° C, VCC=3.0V~3.6V for 70R)

Parameter Std.	Description		Speed Options		Unit
			70R	90	
tWC	Write Cycle Time (Note 1)	Min	70	90	ns
tAS	Address Setup Time	Min	0		ns
tASO	Address Setup Time to OE# low during toggle bit polling	Min	15		ns
tAH	Address Hold Time	Min	45		ns
tAHT	Address Hold Time From CE# or OE# high during toggle bit polling	Min	0		ns
tDS	Data Setup Time	Min	35		ns
tDH	Data Hold Time	Min	0		ns
tCEPH	CE# High During Toggle Bit Polling	Min	20		ns
tOEPH	Output Enable High during toggle bit polling	Min	20		ns
tGHWL	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
tGHEL	Read Recovery Time Before Write	Min	0		ns
tCS	CE# Setup Time	Min	0		ns
tCH	CE# Hold Time	Min	0		ns
tWP	Write Pulse Width	Min	35		ns
tWPH	Write Pulse Width High	Min	30		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)	Typ	240		us
	Single Word/Byte Program Operation (Notes 2,5)	Typ	60		us
	Accelerated Single Word/Byte Programming Operation (Notes 2,5)	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)	Typ	0.5		sec
tVCS	VCC Setup Time (Note 1)	Min	50		us
tRB	Write Recovery Time from RY/BY#	Min	0		ns
tBUSY	Program/Erase Valid to RY/BY# Delay	Min	70	90	ns
tVHH	VHH Rise and Fall Time (Note 1)	Min	250		ns
tPOLL	Program Valid Before Status Polling (Note 6)	Max	4		us

Notes:

1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-16 words/1-32 bytes programmed.
4. Effective write buffer specification is based upon a 16-word/32-byte write buffer operation.
5. Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

ERASE/PROGRAM OPERATION

Figure 4. AUTOMATIC PROGRAM TIMING WAVEFORMS

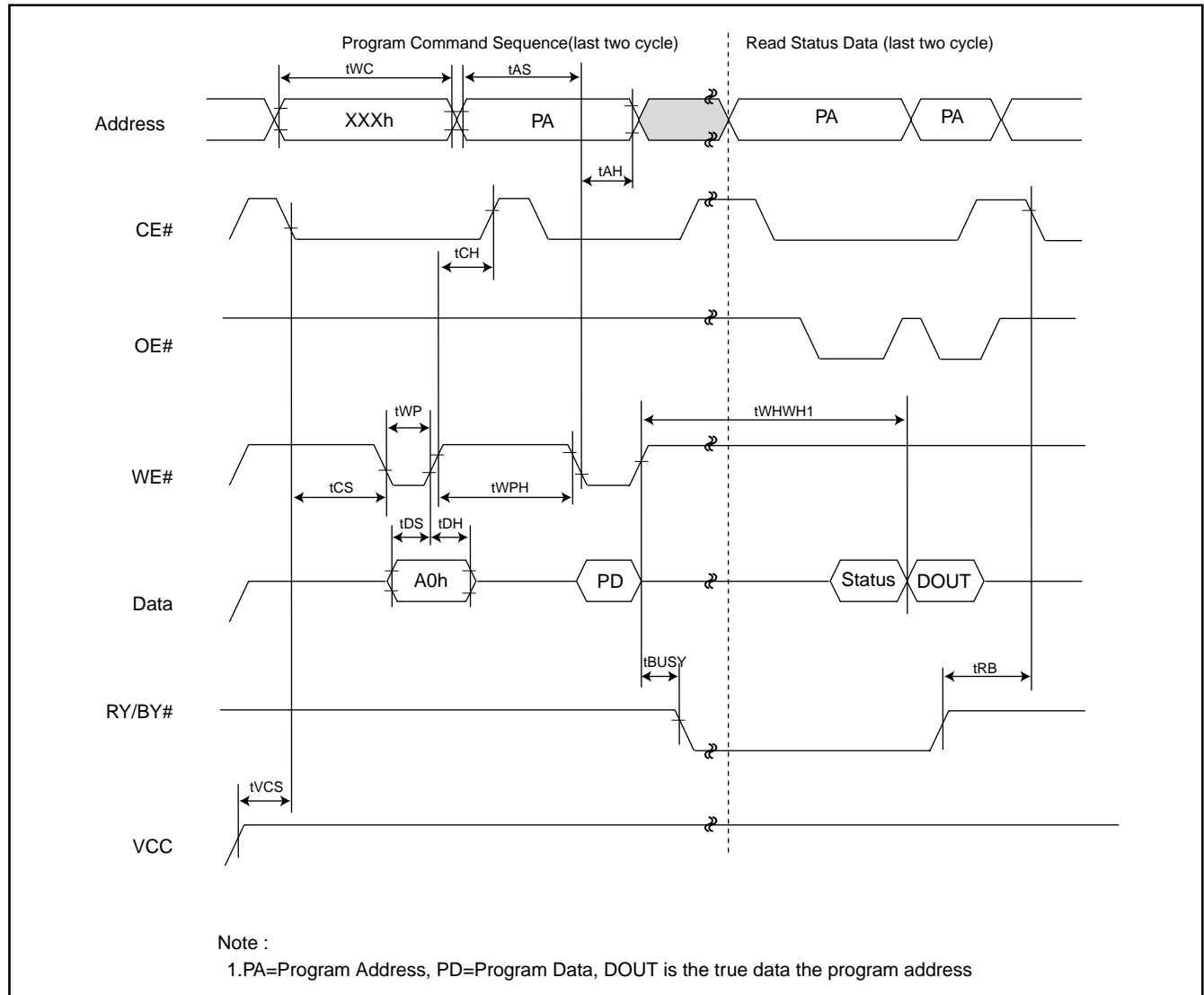


Figure 5. ACCELERATED PROGRAM TIMING DIAGRAM

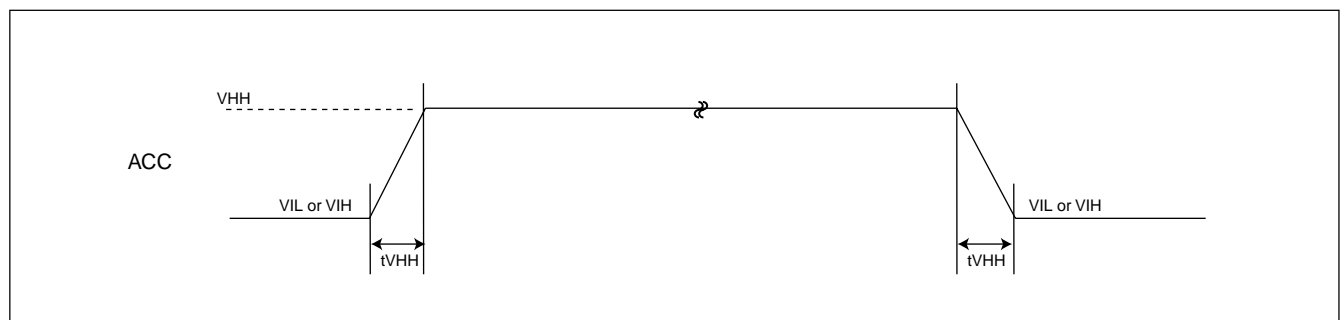


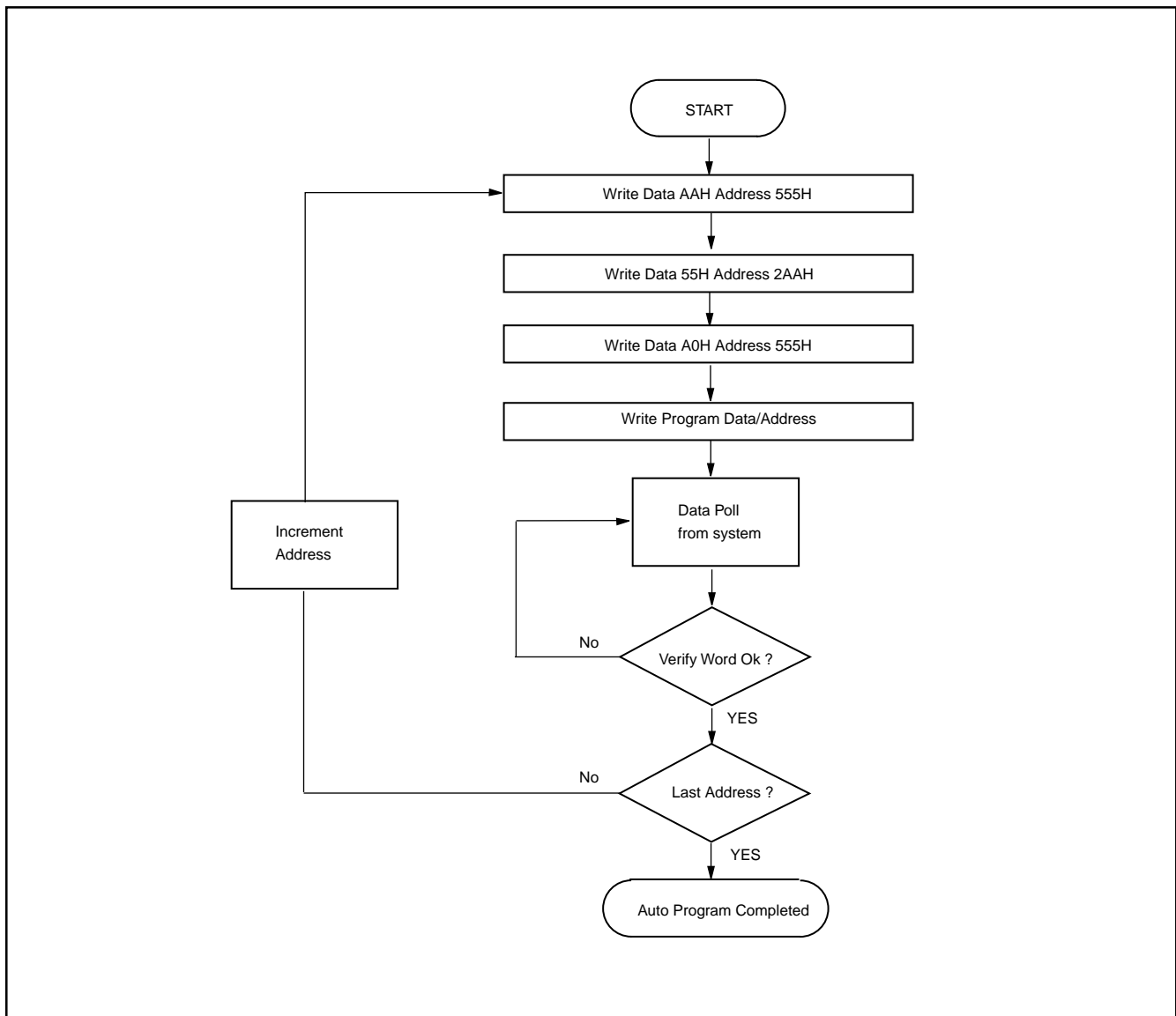
Figure 6. AUTOMATIC PROGRAMMING ALGORITHM FLOWCHART


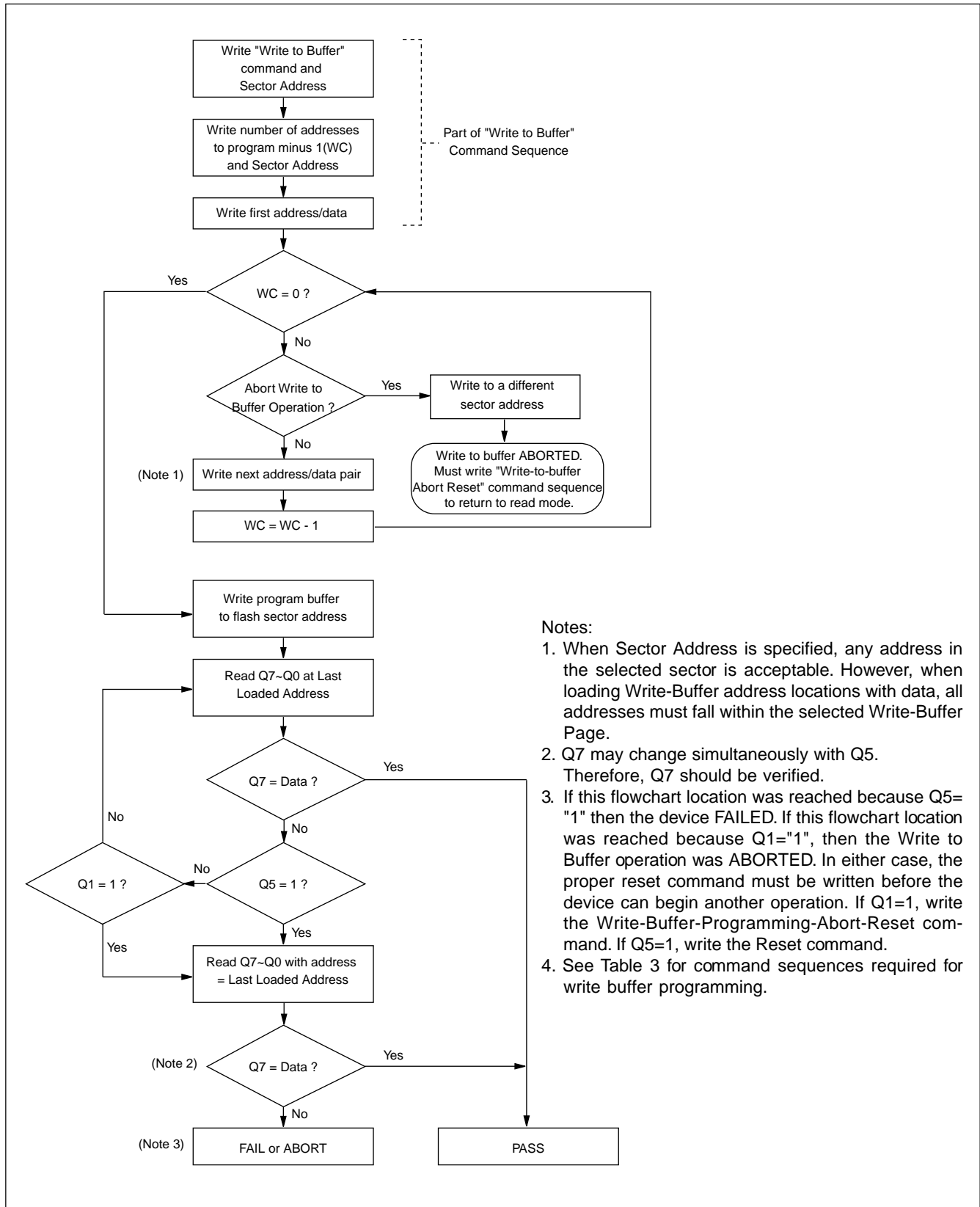
Figure 7. WRITE BUFFER PROGRAMMING ALGORITHM FLOWCHART


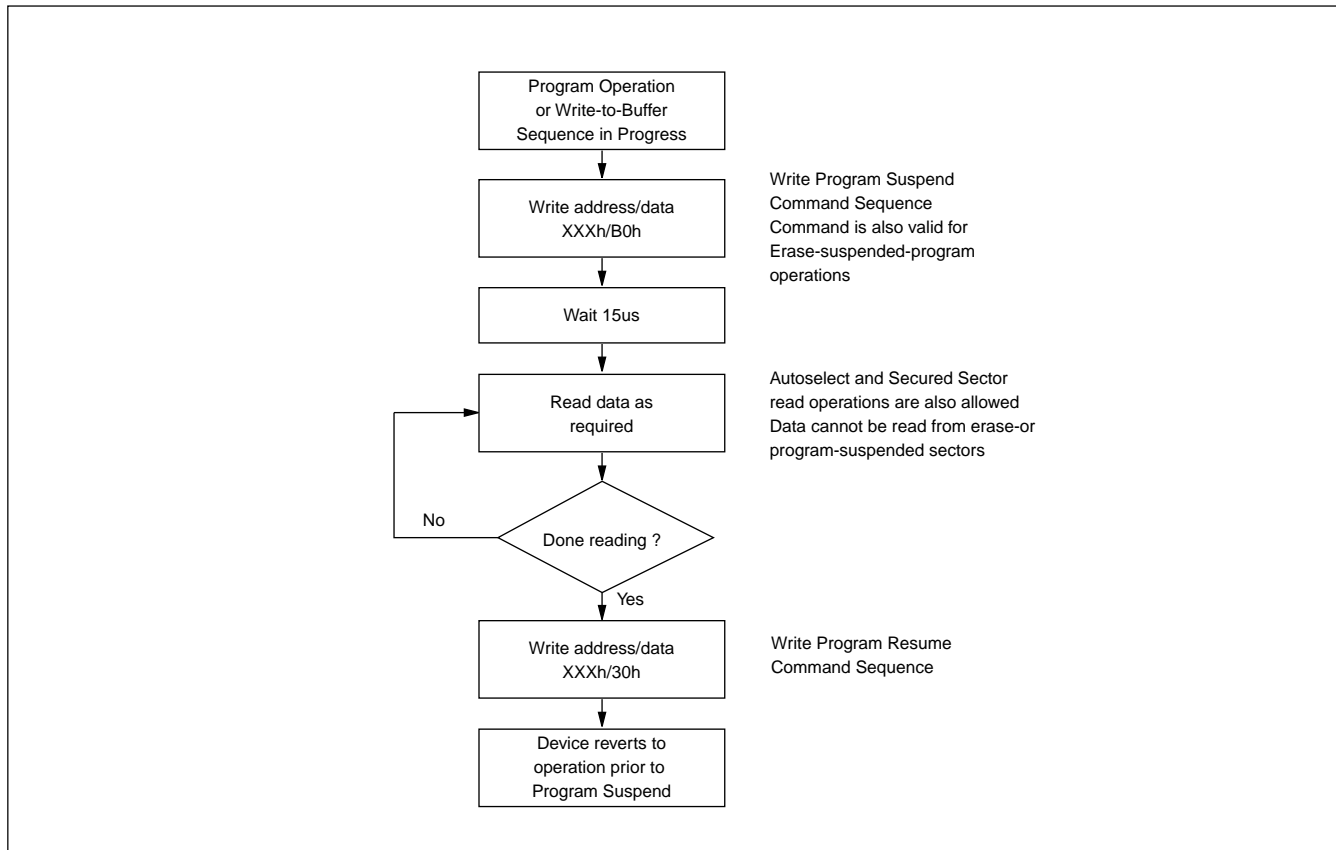
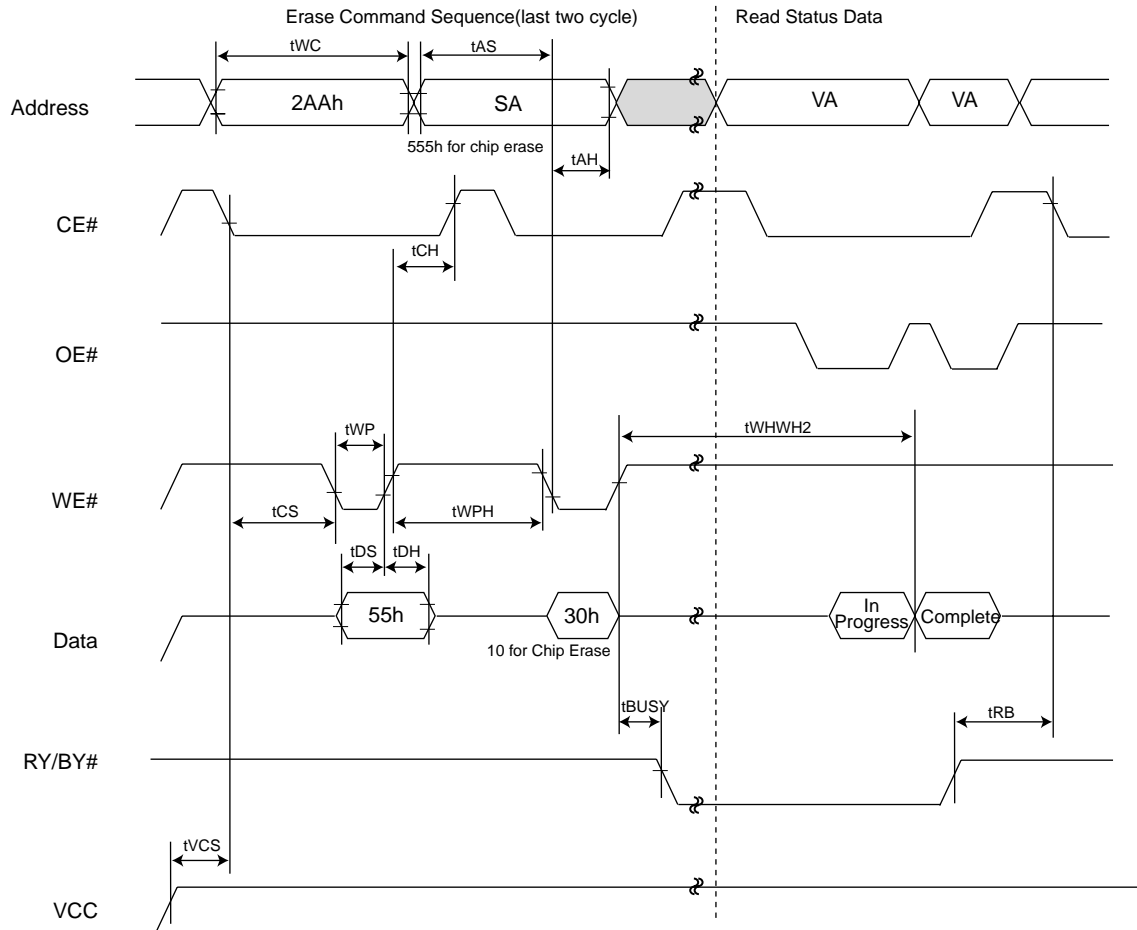
Figure 8. PROGRAM SUSPEND/RESUME FLOWCHART


Figure 9. AUTOMATIC CHIP/SECTOR ERASE TIMING WAVEFORM


Note :

1.SA=sector address(for Sector Erase), VA=Valid Address for reading status data(see "Write Operation Status").

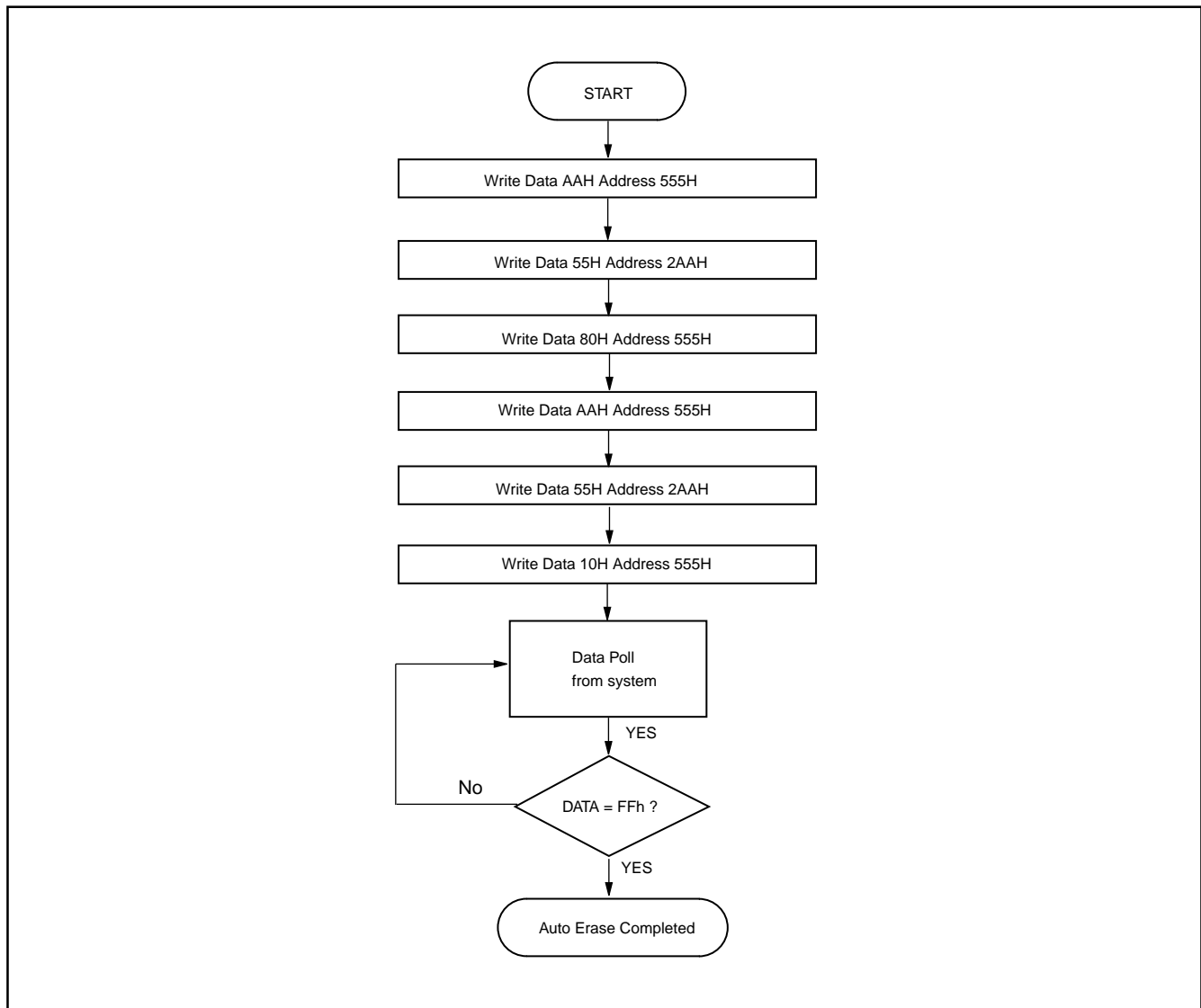
Figure 10. AUTOMATIC CHIP ERASE ALGORITHM FLOWCHART

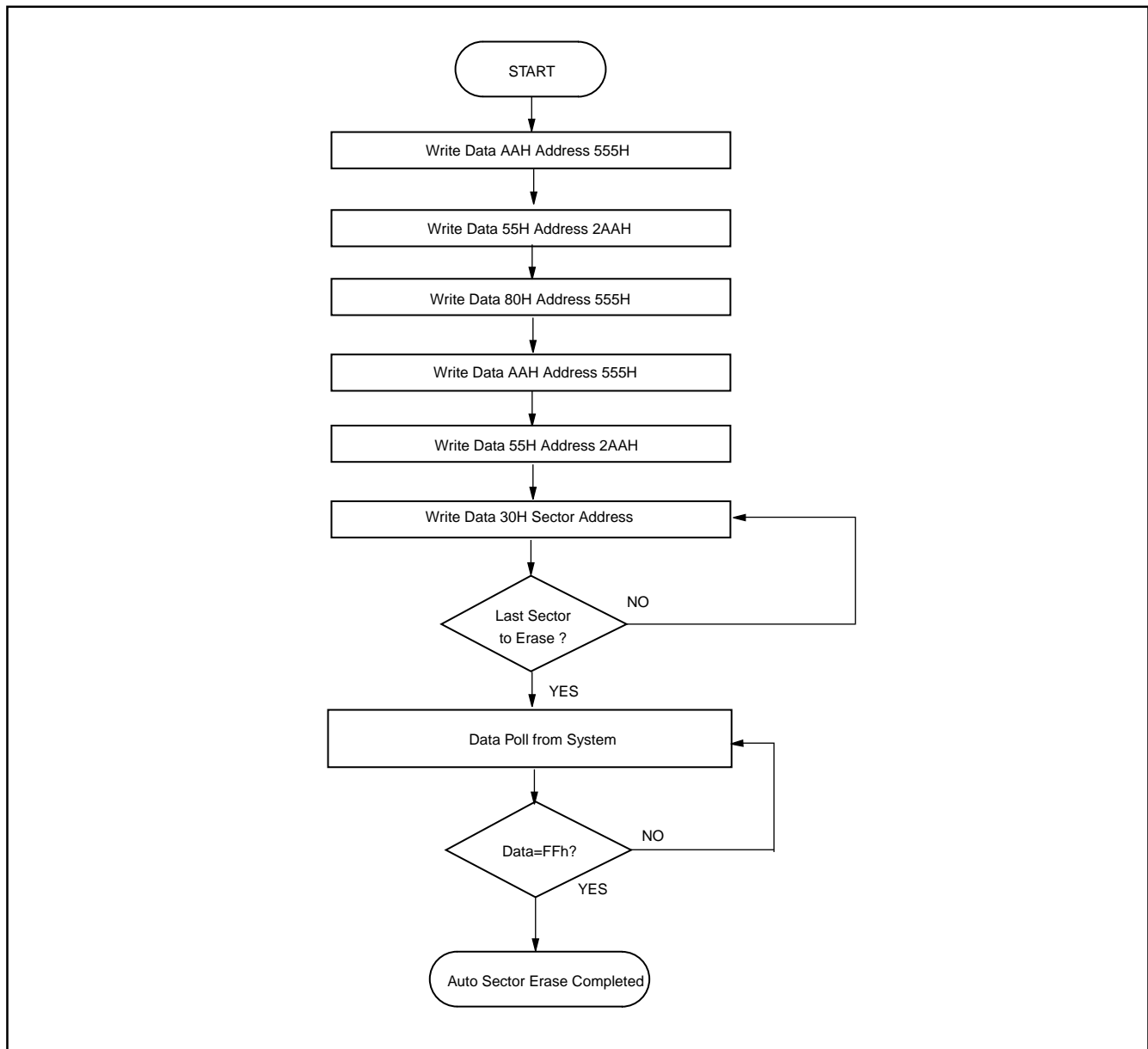
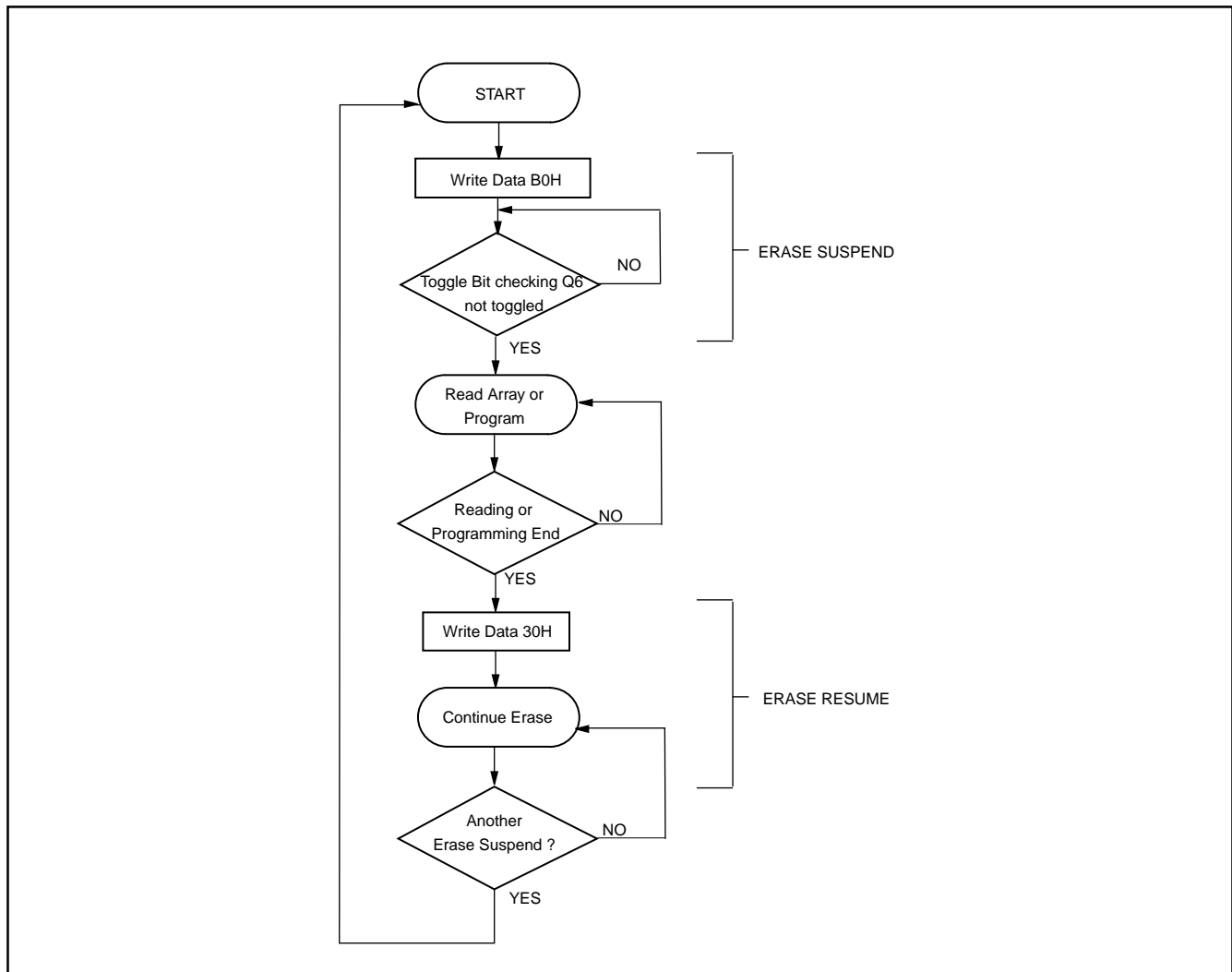
Figure 11. AUTOMATIC SECTOR ERASE ALGORITHM FLOWCHART


Figure 12. ERASE SUSPEND/RESUME FLOWCHART


AC CHARACTERISTICS

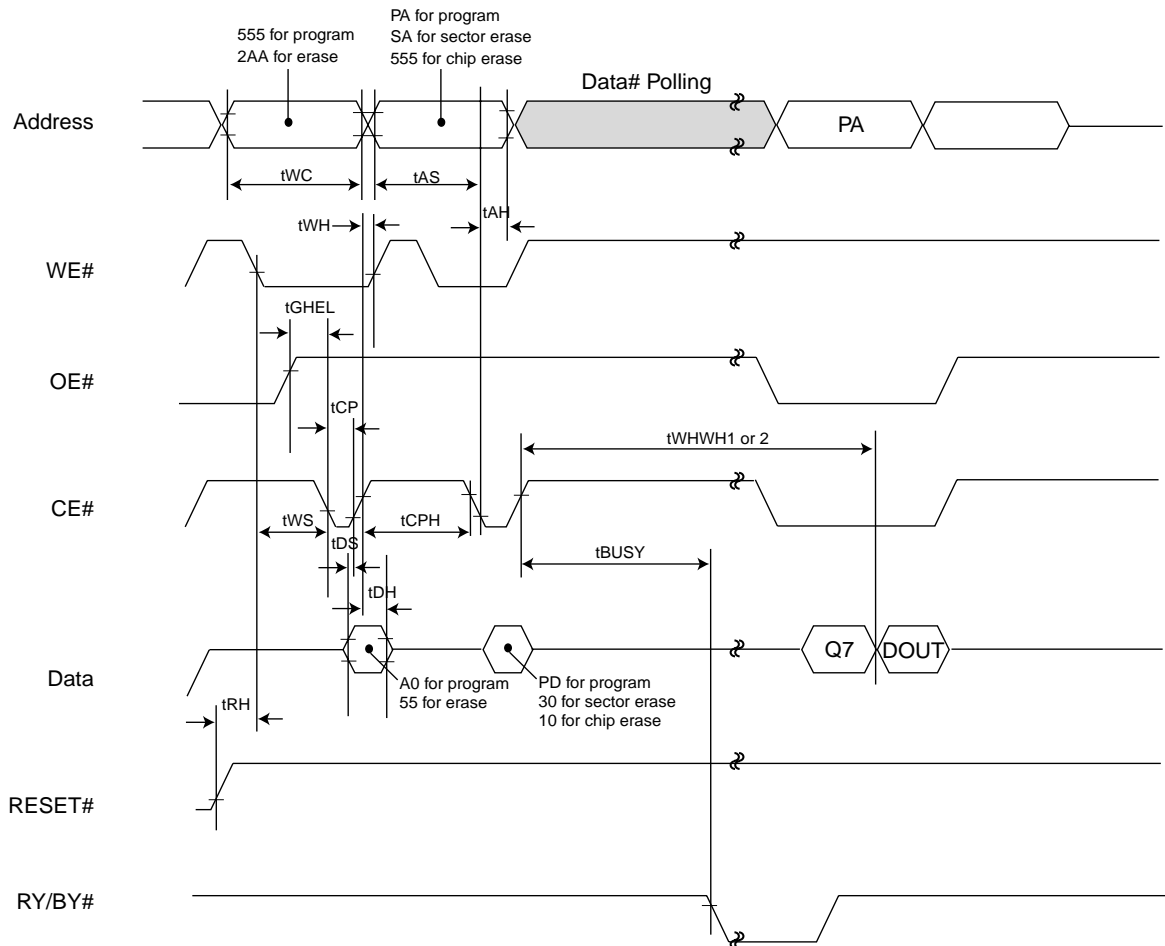
Alternate CE# Controlled Erase and Program Operations

TA=-40° C to 85° C, VCC=2.7V~3.6V (TA= 0° C to 70° C, VCC=3.0V~3.6V for 70R)

Parameter Std.	Description		Speed Options		Unit
			70R	90	
tWC	Write Cycle Time (Note 1)	Min	70	90	ns
tAS	Address Setup Time	Min	0		ns
tAH	Address Hold Time	Min	45		ns
tDS	Data Setup Time	Min	35		ns
tDH	Data Hold Time	Min	0		ns
tGHEL	Read Recovery Time Before Write (OE# High to WE# Low)	Min	0		ns
tWS	WE# Setup Time	Min	0		ns
tWH	WE# Hold Time	Min	0		ns
tCP	CE# Pulse Width	Min	35		ns
tCPH	CE# Pulse Width High	Min	25		ns
tWHWH1	Write Buffer Program Operation (Notes 2,3)	Typ	240		us
	Single Byte Program Operation (Notes 2,5)	Typ	60		us
	Accelerated Single Byte Programming Operation (Notes 2,5)	Typ	54		us
tWHWH2	Sector Erase Operation (Note 2)	Typ	0.5		sec
tRH	RESET HIGH Time Before Write (Note 1)	Min	50		ns
tPOLL	Program Valid Before Status Polling (Note 6)	Max	4		us

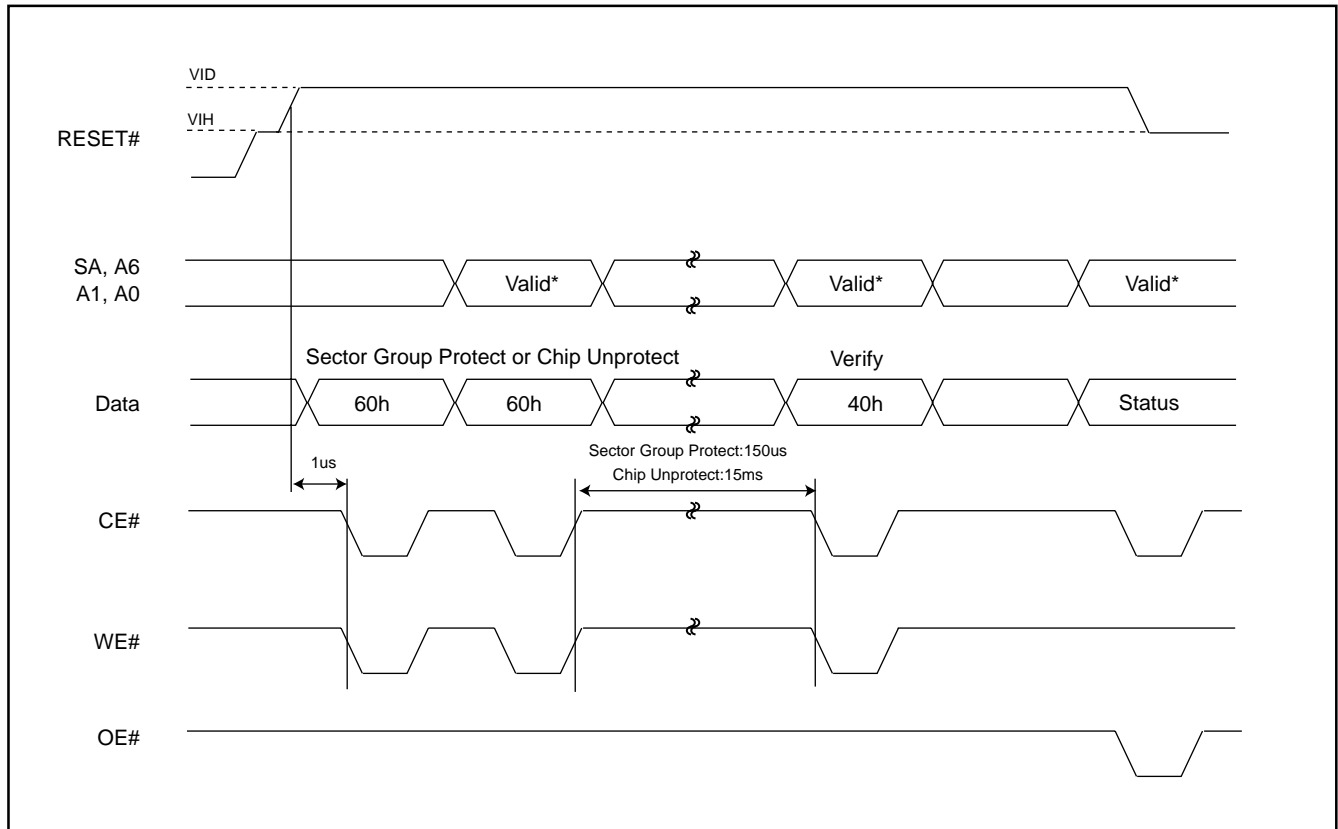
Notes:

1. Not 100% tested.
2. See the "Erase And Programming Performance" section for more information.
3. For 1-32 bytes programmed.
4. Effective write buffer specification is based upon a 32-byte write buffer operation.
5. Byte programming specification is based upon a single byte programming operation not utilizing the write buffer.
6. When using the program suspend/resume feature, if the suspend command is issued within tPOLL, tPOLL must be fully re-applied upon resuming the programming operation. If the suspend command is issued after tPOLL, tPOLL is not required again prior to reading the status bits upon resuming.

Figure 13. CE# CONTROLLED PROGRAM TIMING WAVEFORM


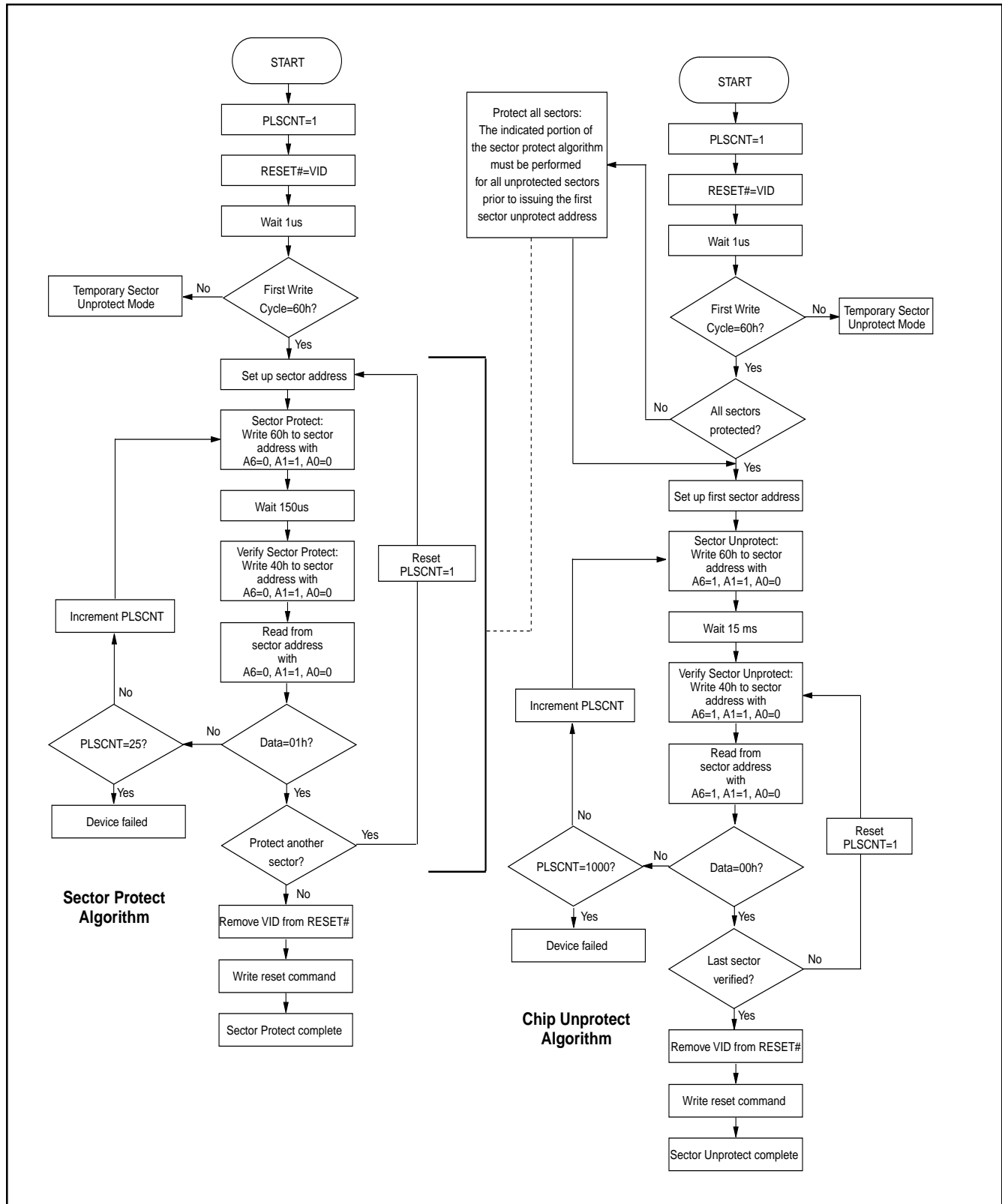
SECTOR GROUP PROTECT/CHIP UNPROTECT

Figure 14. Sector Group Protect / Chip Unprotect Waveform (RESET# Control)



Note: For sector group protect A6=0, A1=1, A0=0. For chip unprotect A6=1, A1=1, A0=0

Figure 15. IN-SYSTEM SECTOR GROUP PROTECT/CHIP UNPROTECT ALGORITHMS WITH RESET#=VID



AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVLHT	Voltage transition time	Min.	4	us
tWPP1	Write pulse width for sector group protect	Min.	100	ns
tOESP	OE# setup time to WE# active	Min.	4	us

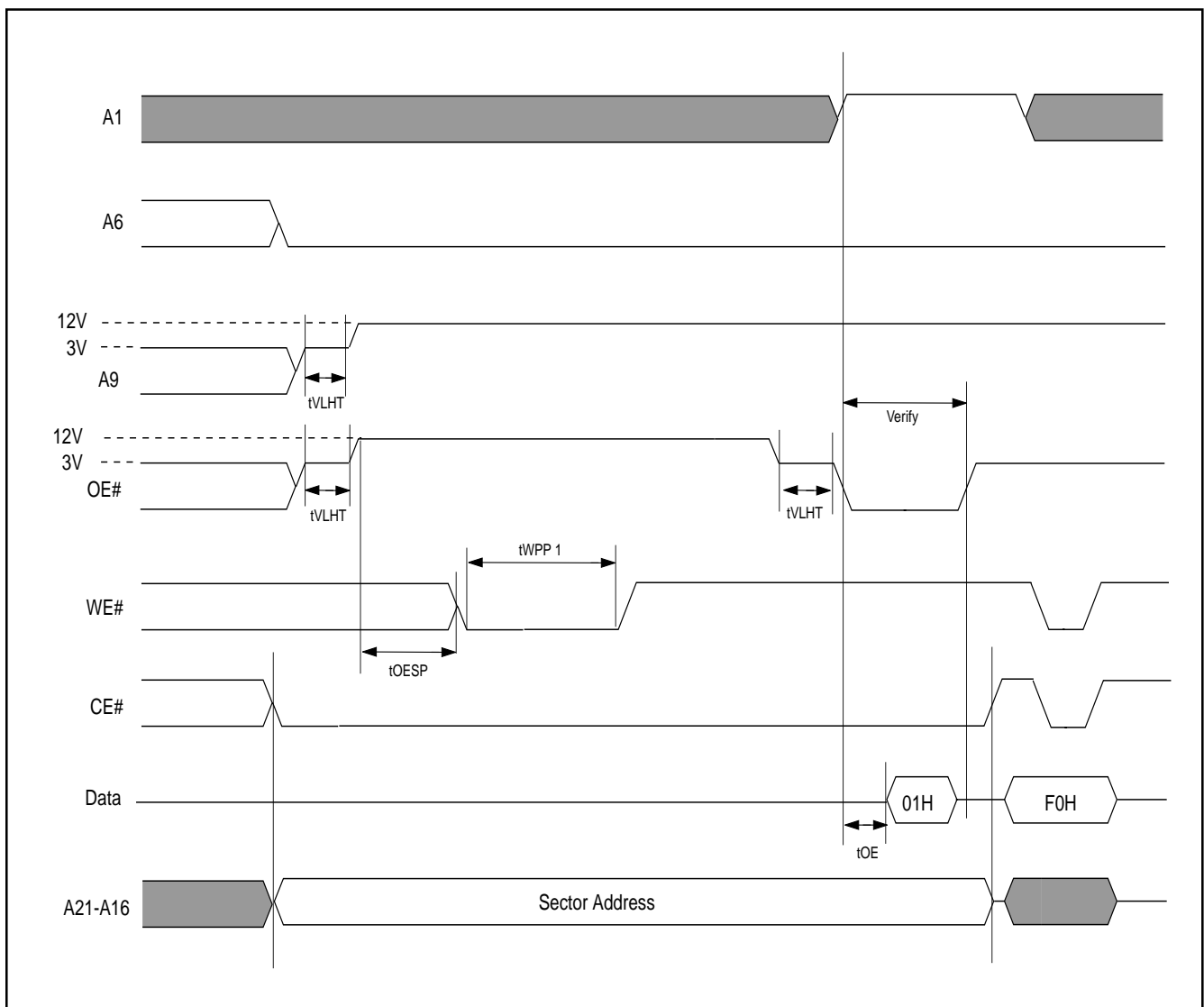
Figure 16. SECTOR GROUP PROTECT TIMING WAVEFORM (A9, OE# Control)


Figure 17. SECTOR GROUP PROTECTION ALGORITHM (A9, OE# Control)

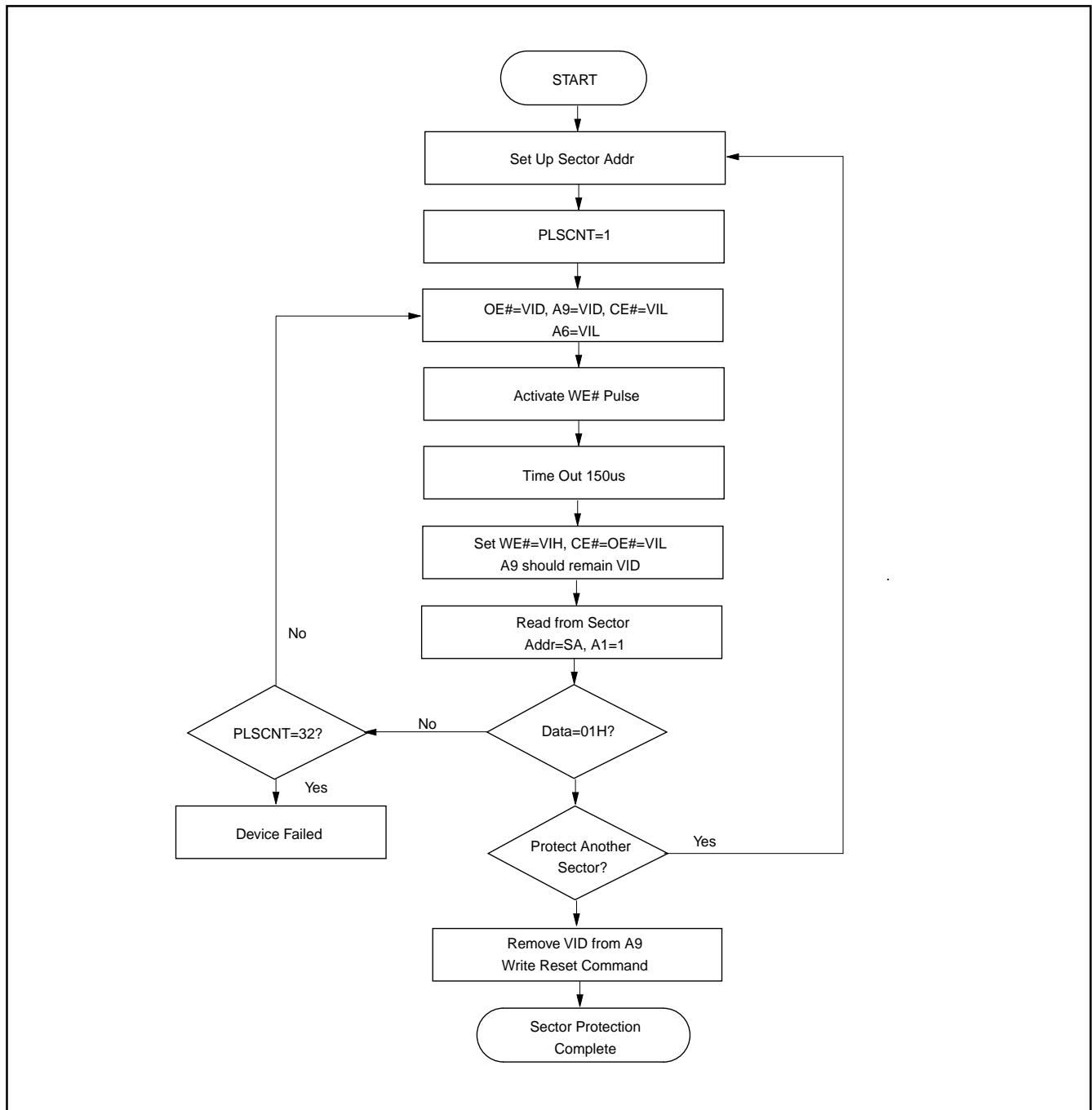


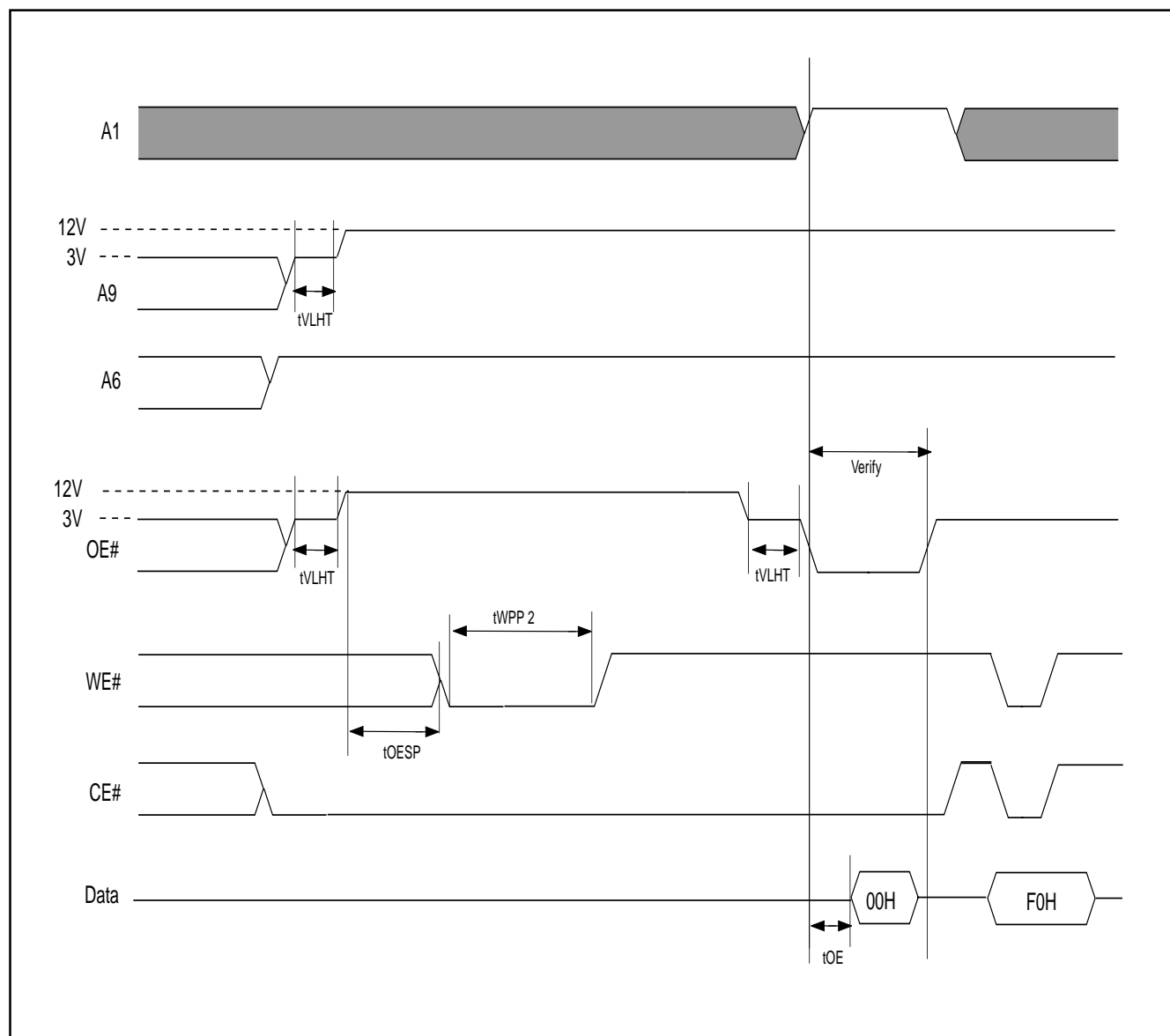
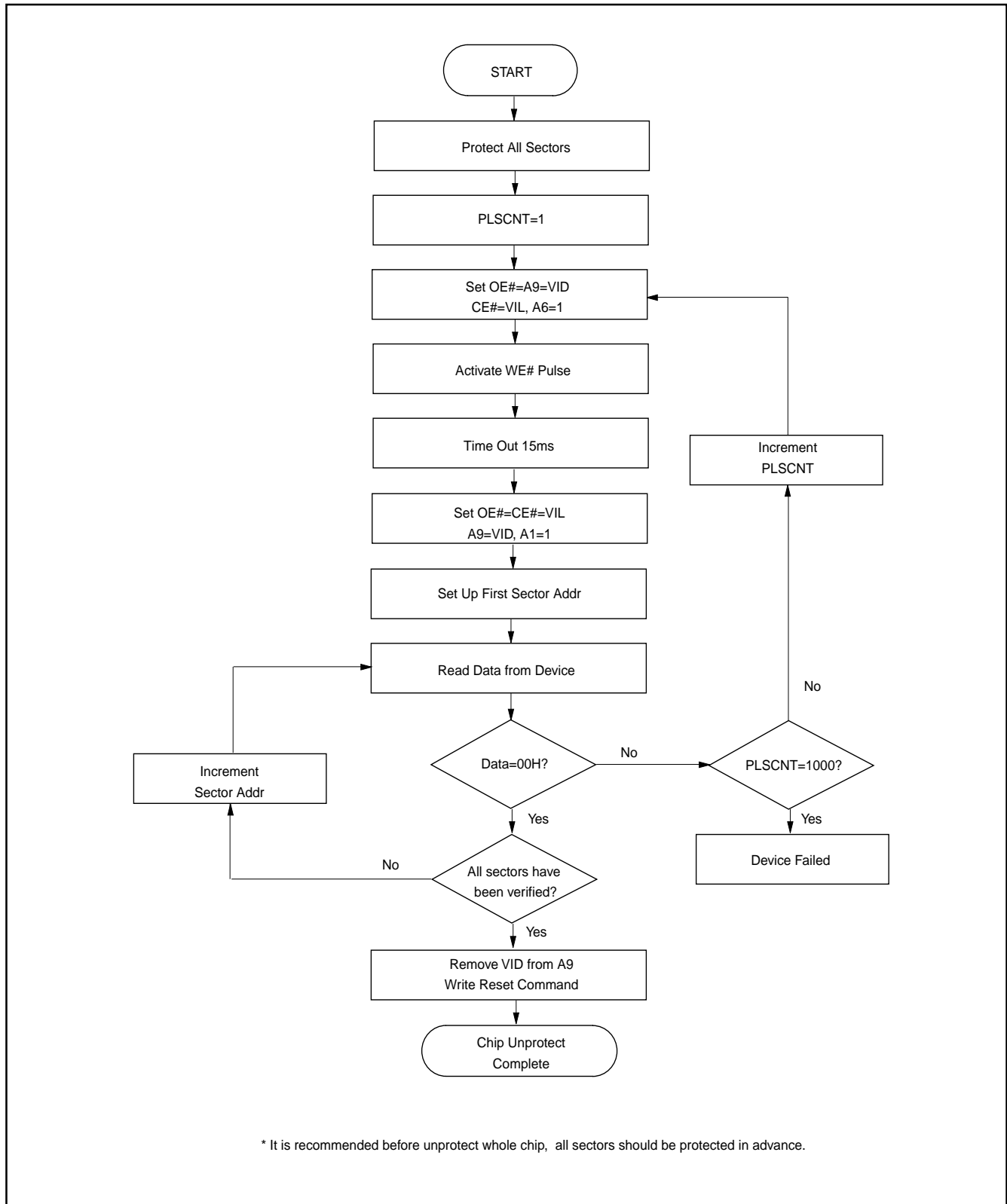
Figure 18. CHIP UNPROTECT TIMING WAVEFORM (A9, OE# Control)


Figure 19. CHIP UNPROTECT FLOWCHART (A9, OE# Control)


AC CHARACTERISTICS

Parameter	Description	Test Setup	All Speed Options	Unit
tVIDR	VID Rise and Fall Time (see Note)	Min	500	ns
tRSP	RESET# Setup Time for Temporary Sector Unprotect	Min	4	us
tRRB	RESET# Hold Time from RY/BY# High for Temporary Sector Group Unprotect	Min	4	us

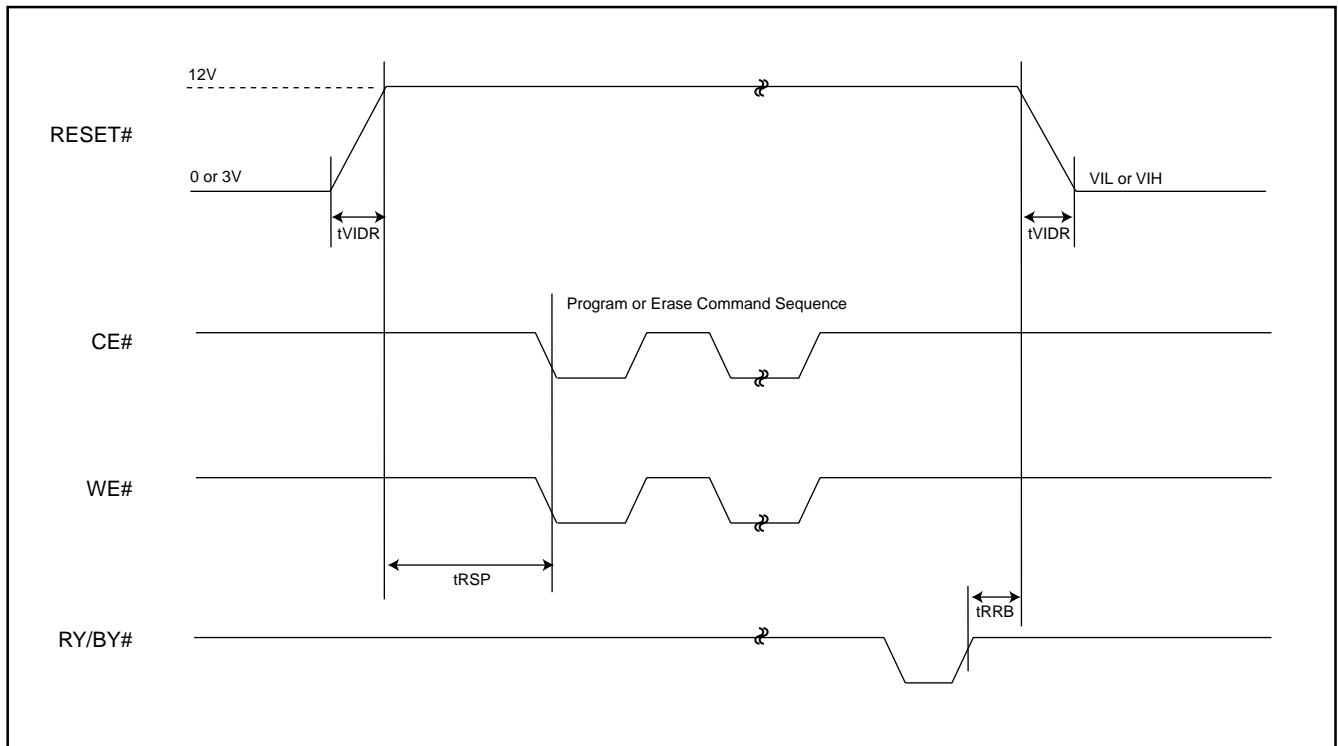
Figure 20. TEMPORARY SECTOR GROUP UNPROTECT WAVEFORMS


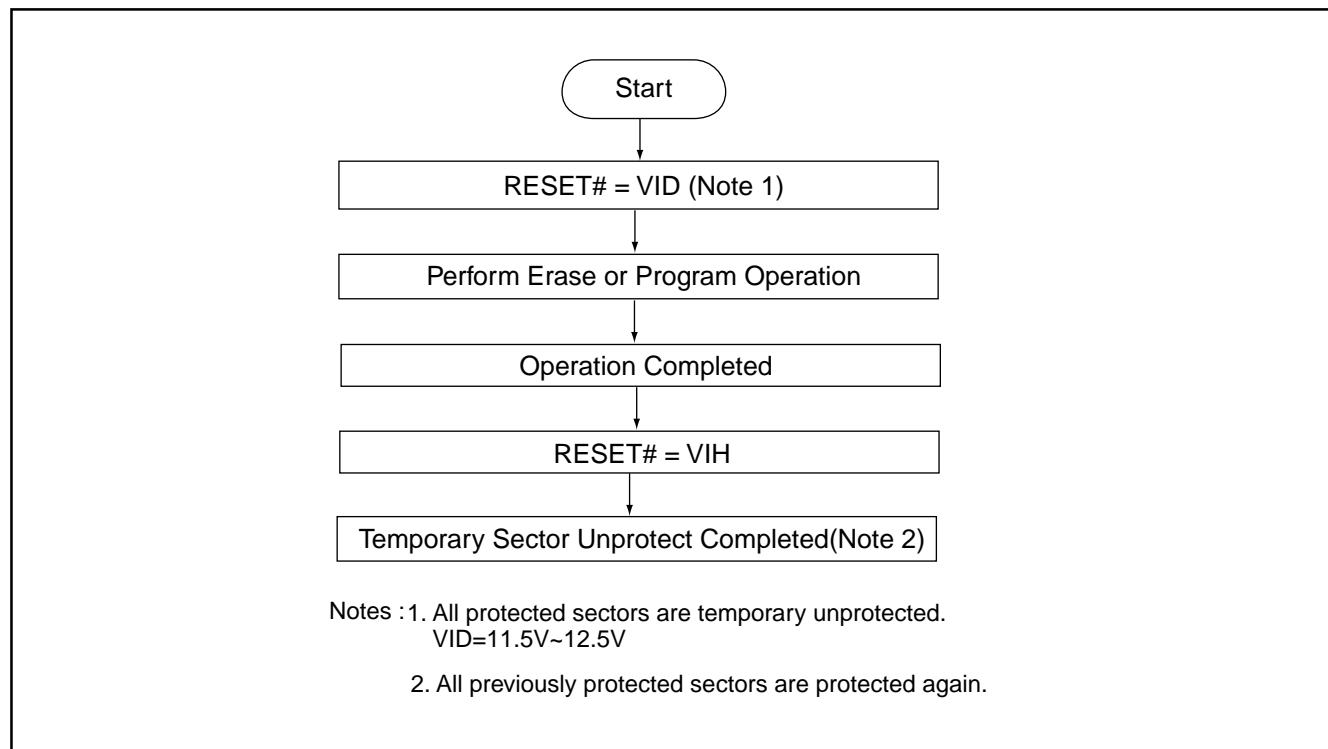
Figure 21. TEMPORARY SECTOR GROUP UNPROTECT FLOWCHART

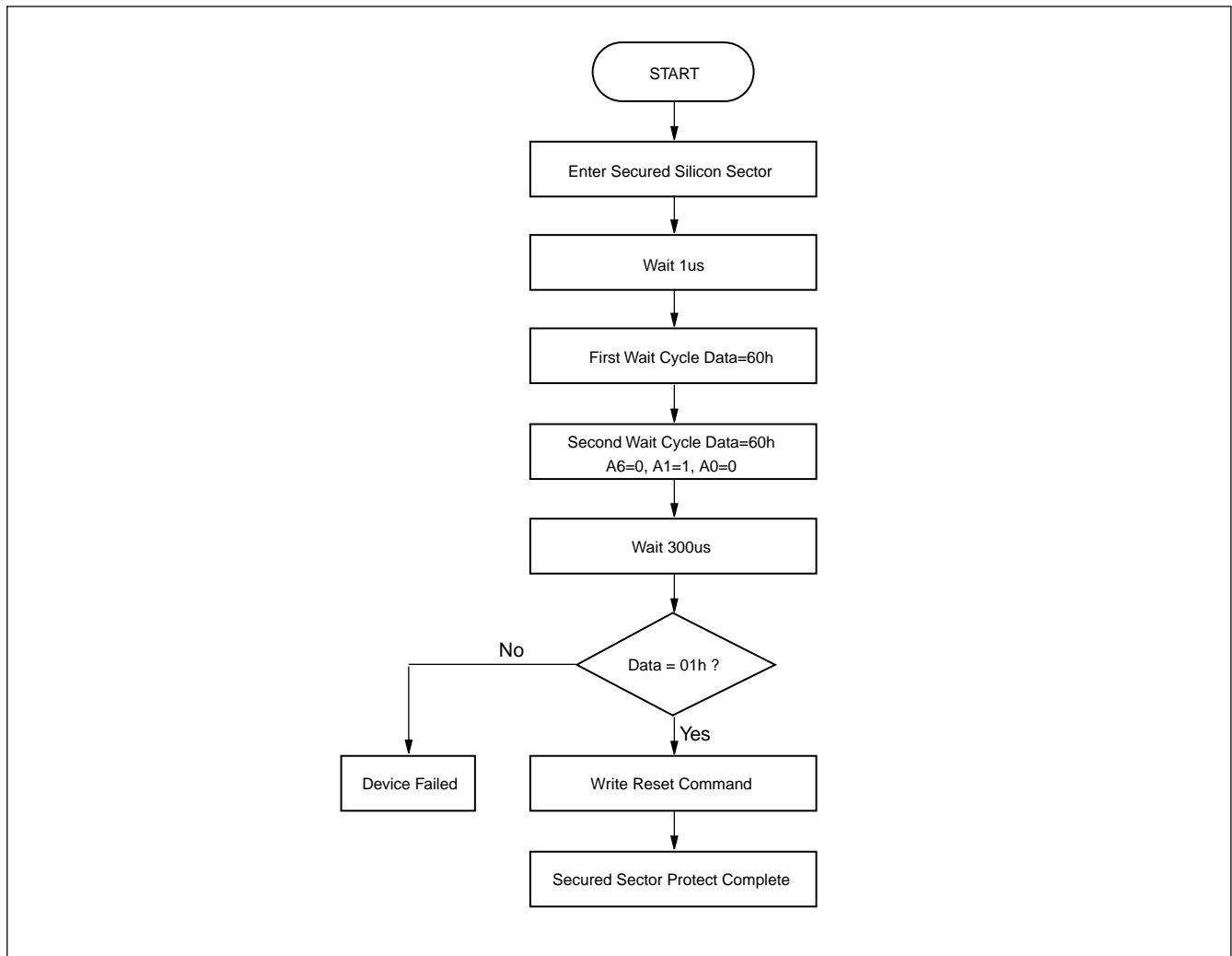
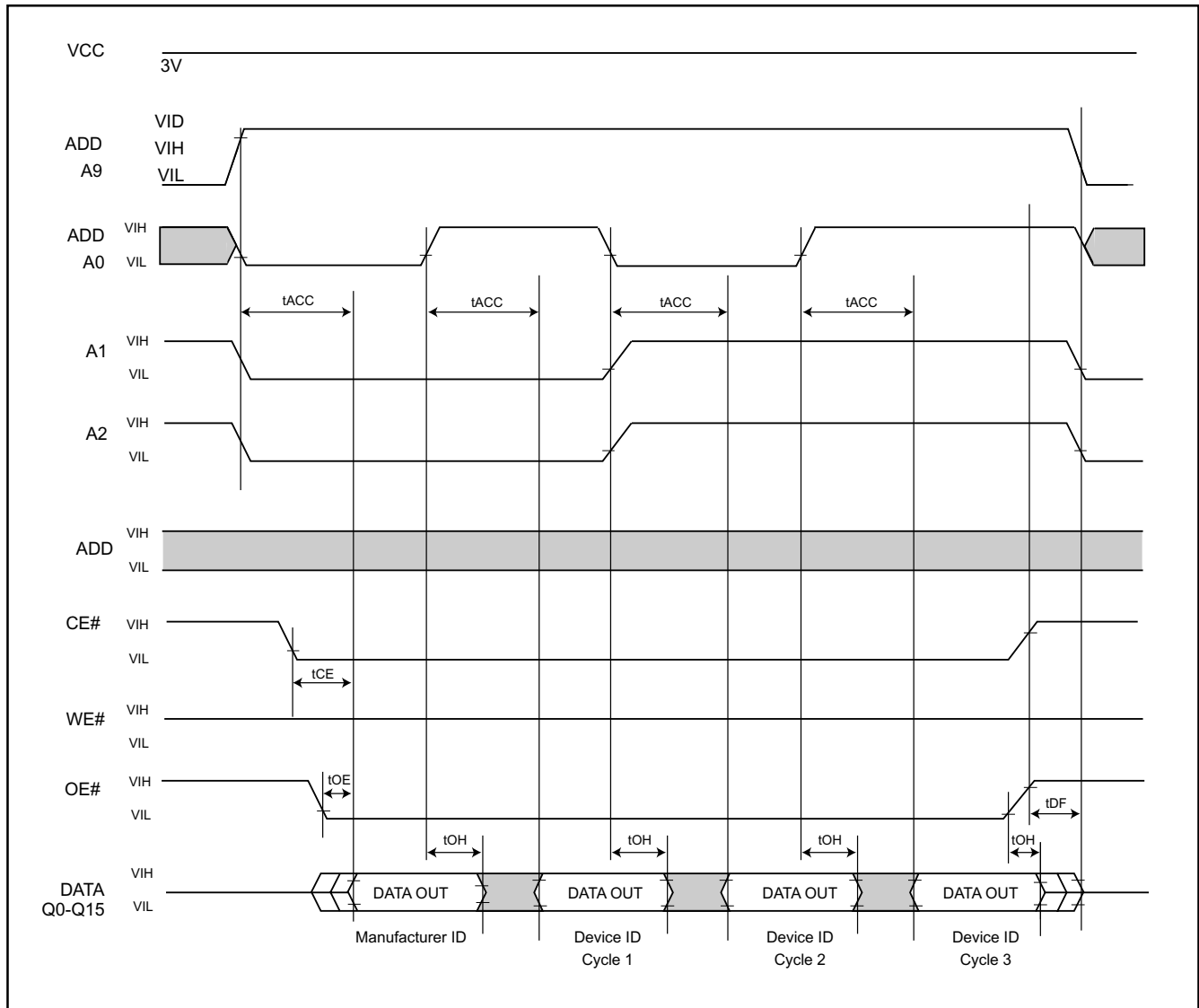
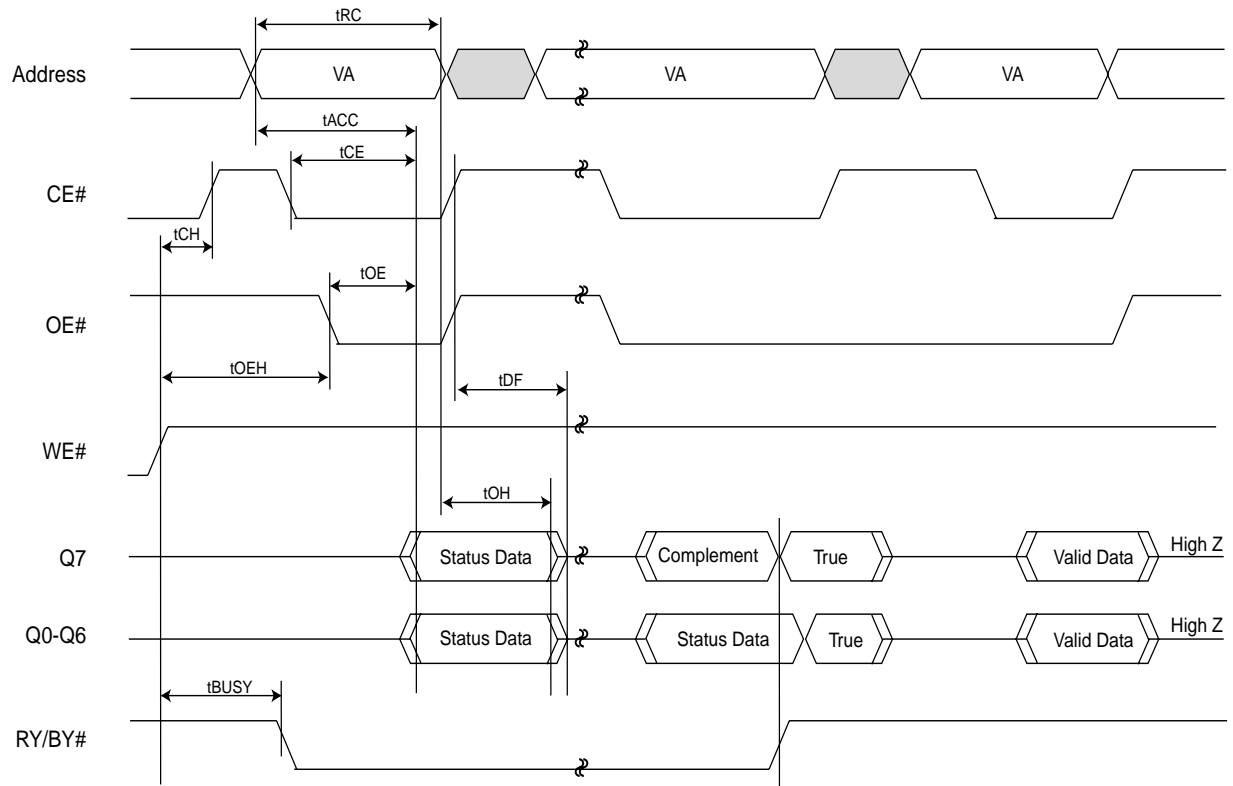
Figure 22. SECURED SILICON SECTOR PROTECTED ALGORITHMS FLOWCHART

Figure 23. SILICON ID READ TIMING WAVEFORM


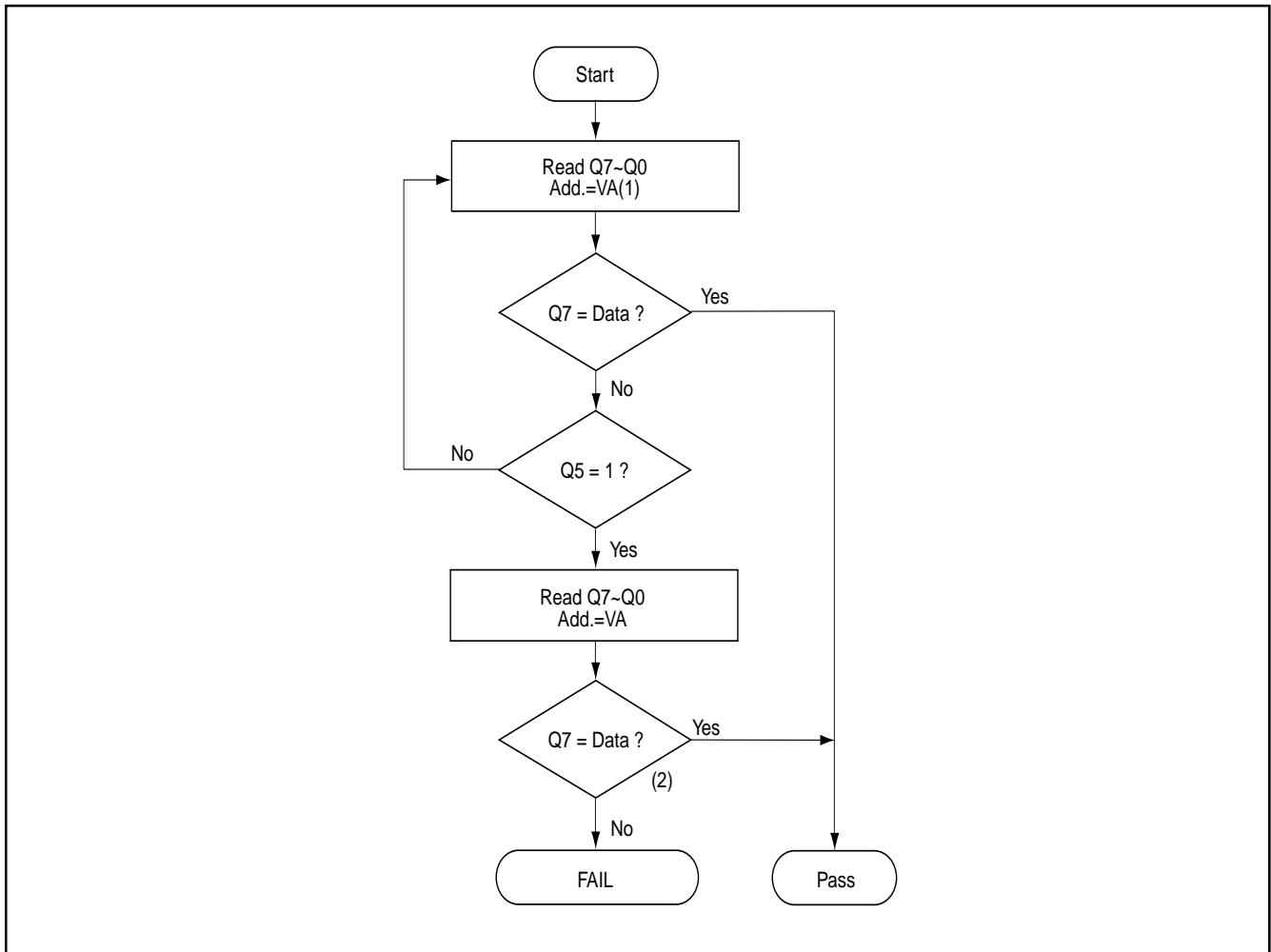
WRITE OPERATION STATUS

Figure 24. DATA# POLLING TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)



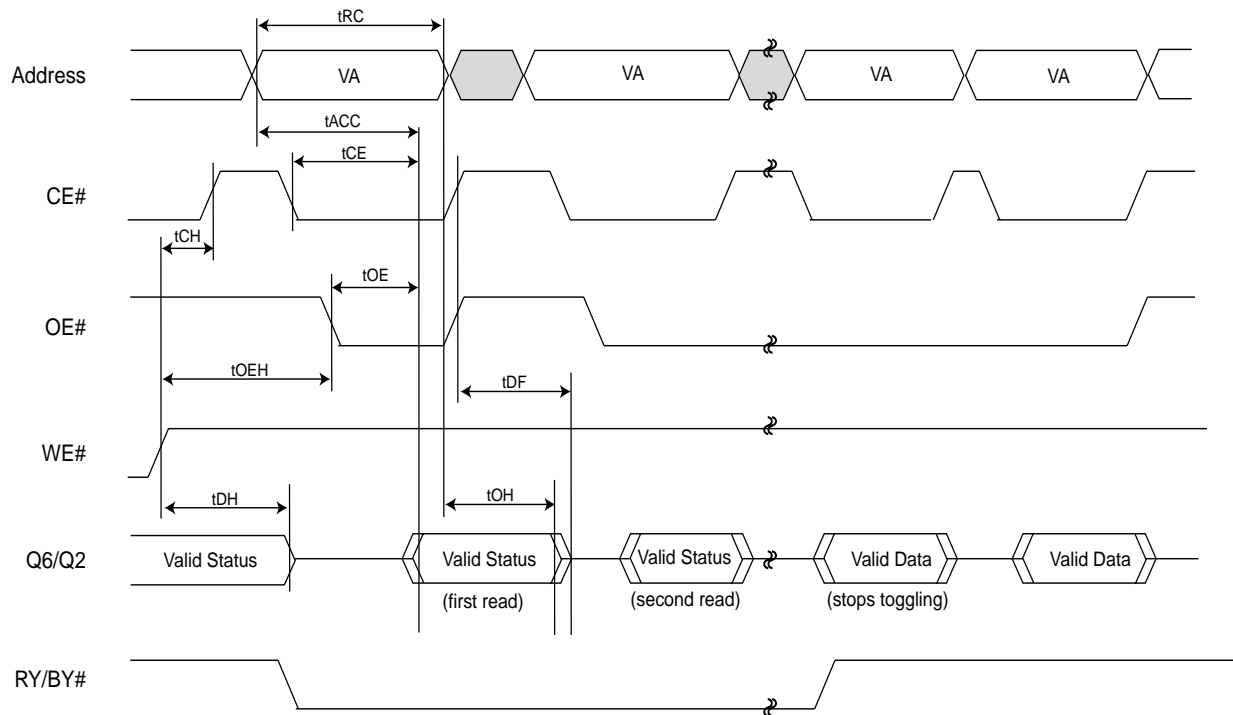
Note :

VA=Valid address. Figure shows are first status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 25. DATA# POLLING ALGORITHM

Notes:

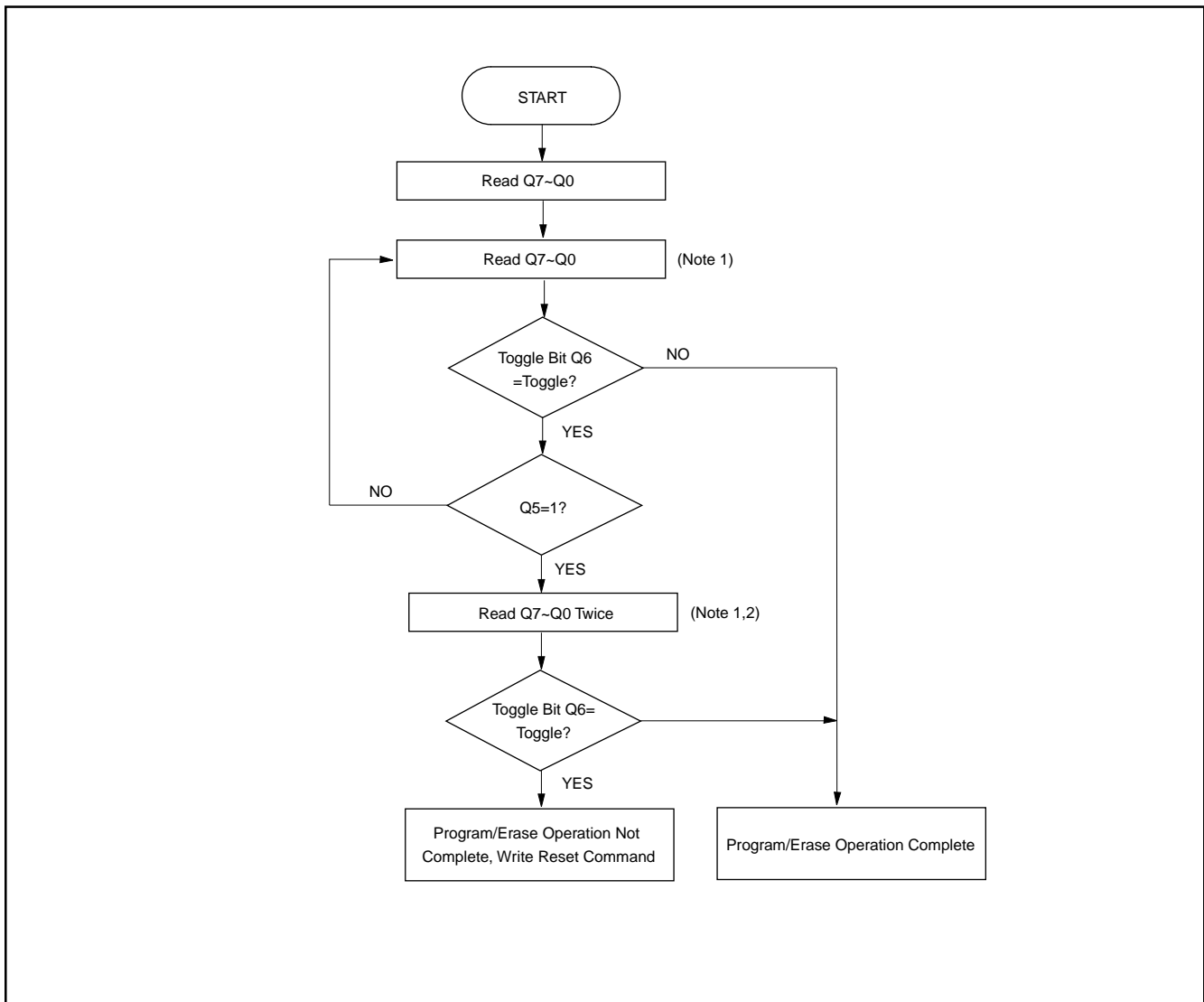
1. VA=valid address for programming.

2. Q7 should be rechecked even Q5="1" because Q7 may change simultaneously with Q5.

Figure 26. TOGGLE BIT TIMING WAVEFORMS (DURING AUTOMATIC ALGORITHMS)


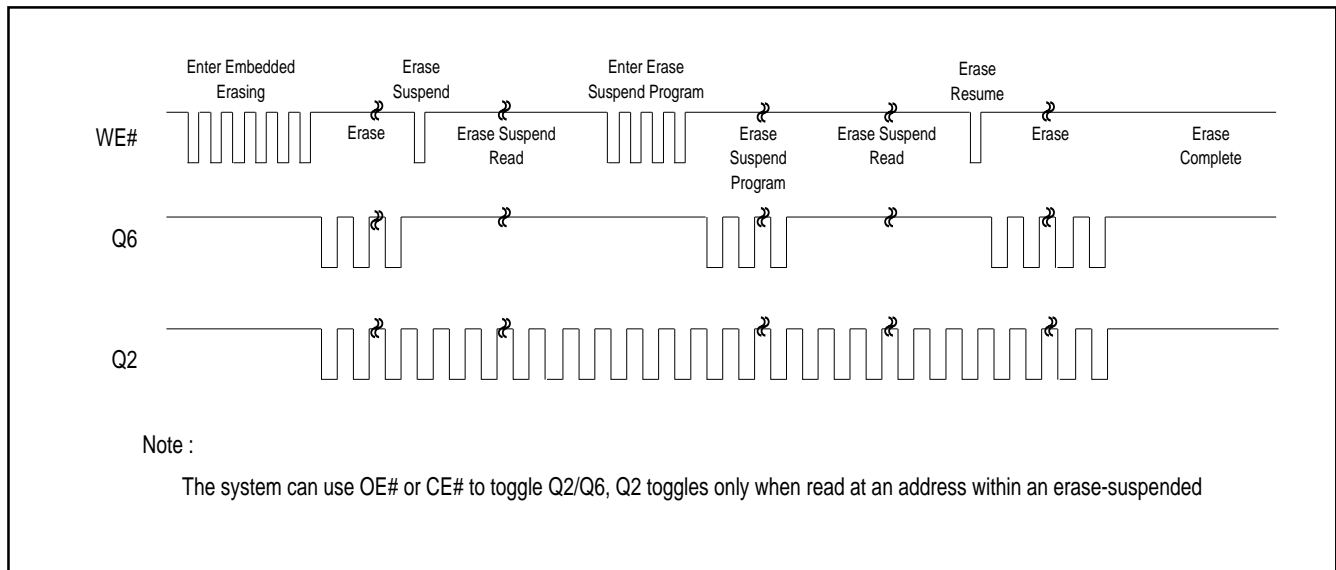
Note :

VA=Valid address; not required for Q6. Figure shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

Figure 27. TOGGLE BIT ALGORITHM


Notes :

1. Read toggle bit twice to determine whether or not it is toggling.
2. Recheck toggle bit because it may stop toggling as Q5 changes to "1".

Figure 28. Q6 versus Q2


ERASE AND PROGRAMMING PERFORMANCE (1)

PARAMETER	Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time	0.5	3.5	sec	Excludes 00h programming prior to erasure Note 6
Chip Erase Time	32	64	sec	
Total Write Buffer Program Time (Note 4)	240		us	Excludes system level overhead Note 7
Total Accelerated Effective Write Buffer Program Time (Note 4)	200		us	
Chip Program Time	31.5		sec	

Notes:

1. Typical program and erase times assume the following conditions: 25° C, 3.0 V VCC. Programming specifications assume checkerboard data pattern.
2. Maximum values are measured at VCC = 3.0 V, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.
3. Byte programming specification is based upon a single byte programming operation not utilizing the write buffer.
4. For 1-32 bytes programmed in a single write buffer programming operation.
5. Effective write buffer specification is calculated on a per-byte basis for a 32-byte write buffer operation.
6. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
7. System-level overhead is the time required to execute the command sequence(s) for the program command. See Tables 3 for further information on command definitions.
8. The device has a minimum erase and program cycle endurance of 100,000 cycles.

LATCH-UP CHARACTERISTICS

	MIN.	MAX.
Input Voltage with respect to GND on all pins except I/O pins	-1.0V	13.5V
Input Voltage with respect to GND on all I/O pins	-1.0V	VCC + 1.0V
Current	-100mA	+100mA
Includes all pins except VCC. Test conditions: VCC = 3.0V, one pin at a time.		

DATA RETENTION

Parameter	Min	Unit
Minimum Pattern Data Retention Time	20	Years

TSOP PIN AND BGA PACKAGE CAPACITANCE

Parameter Symbol	Parameter Description	Test Set		TYP	MAX	UNIT
CIN	Input Capacitance	VIN=0	TSOP	6	7.5	pF
			CSP	4.2	5.0	pF
COUT	Output Capacitance	VOUT=0	TSOP	8.5	12	pF
			CSP	5.4	6.5	pF
CIN2	Control Pin Capacitance	VIN=0	TSOP	7.5	9	pF
			CSP	3.9	4.7	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions TA=25°C, f=1.0MHz

**ORDERING INFORMATION**

PART NO.	ACCESS TIME (ns)	Ball Pitch/ Ball size	PACKAGE	Remark
MX29LV033MTC-70R	70		40 Pin TSOP	
MX29LV033MTI-70R	70		40 Pin TSOP	
MX29LV033MTC-90	90		40 Pin TSOP	
MX29LV033MTI-90	90		40 Pin TSOP	
MX29LV033MTC-90G	90		40 Pin TSOP	Pb-free
MX29LV033MTI-90G	90		40 Pin TSOP	Pb-free

PART NAME DESCRIPTION

MX 29 LV 640 M T T C - 90 G

OPTION:

G: Lead-free package

R: Restricted VCC (3.0V~3.6V)

Q: Restricted VCC (3.0V~3.6V) with Lead-free package

blank: normal

SPEED:

70: 70ns

90: 90ns

10:100ns

TEMPERATURE RANGE:

C: Commercial (0°C to 70°C)

I: Industrial (-40°C to 85°C)

PACKAGE:

M: SOP

T: TSOP

X: FBGA (CSP)

XB - 0.3mm Ball

XE - 0.4mm Ball

XC - 1.0mm Ball

BOOT BLOCK TYPE:

T: Top Boot

B: Bottom Boot

H: Uniform with Highest Sector H/W Protect

L: Uniform with Lowest Sector H/W Protect

U: Uniform Sector

REVISION:

M: NBit Technology

DENSITY & MODE:

033/320/321: 32Mb, Page Mode Flash Device

065/640/641: 64Mb, Page Mode Flash Device

128/129: 128Mb, Page Mode Flash Device

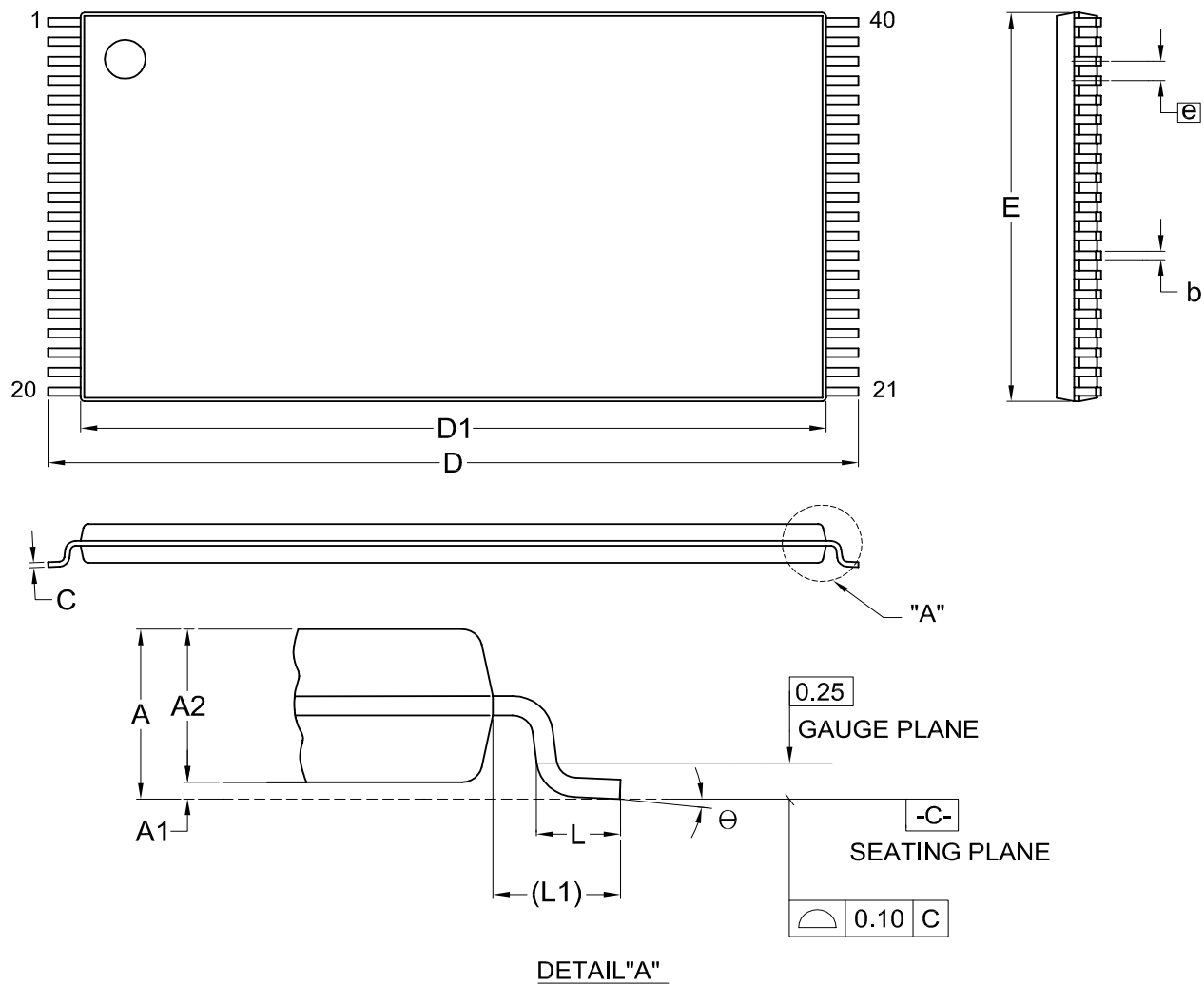
TYPE:

LV/GL: 3V standard

LA: 3V Security

DEVICE:

29:Flash

PACKAGE INFORMATION
Title: Package Outline for TSOP(I) 40L (10X20mm)


Dimensions (inch dimensions are derived from the original mm dimensions)

SYMBOL		A	A1	A2	b	C	D	D1	E	e	L	L1	Θ
mm	Min.	—	0.05	0.95	0.17	0.10	19.80	18.30	9.90		0.50	0.70	0
	Nom.	—	0.10	1.00	0.20	0.13	20.00	18.40	10.00	0.50	0.60	0.80	5
	Max.	1.20	0.15	1.05	0.27	0.21	20.20	18.50	10.10		0.70	0.90	8
Inch	Min.	—	0.002	0.037	0.007	0.004	0.780	0.720	0.390		0.020	0.028	0
	Nom.	---	0.004	0.039	0.008	0.005	0.787	0.724	0.394	0.020	0.024	0.031	5
	Max.	0.047	0.006	0.041	0.011	0.008	0.795	0.728	0.398		0.028	0.035	8

DWG.NO.	REVISION	REFERENCE			ISSUE DATE
		JEDEC	EIAJ		
6110-1606	6	MO-142			12-01-'03

REVISION HISTORY

Revision No.	Description	Page	Date
1.0	1. Removed "Preliminary" wording	P1	AUG/10/2005
	2. Added description about Pb-free device is RoHS compliant	P1	
	2. Added note 6 for ILIT parameter in DC Characteristics table	P29	
	3. Added comments into performance table	P60	
	4. Added Part Name Description	P63	



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