MX3000DS
MaxxBass ASIC for Psycho-Acoustic Bass Extension

MX3000DS Features

- Second Generation ASIC for patented MaxxBass® algorithm
- Proven to extend perceived bass frequency response by up to $1^1/_2$ octaves
- Analog stereo input and output with minimal external components
- Supports I^2C host and stand-alone (no microcontroller host) applications
- Software commands for

- Intensity	- Clock Divider
- Bypass	- Subwoofer Low Pass Filter
- Powerdown	- Power-on Output Delay
- Snap reduction	- Noise Gate

- Improved SNR with higher 2.0Vpp input dynamic range and noise gate
- Controls for setting MaxxBass Intensity without a microcontroller host
- Reset pin voltage monitor for robust reset behavior
- Low cost 16-pin 150mil SOIC RoHS compliant green packaging
- Low power consumption with 3.3 volt operation

MX3000DS Description

MaxxBass is a bass frequency extension technology that extends the perceived bass frequency response below the physical low frequency cut off in an audio system. It is based upon psycho-acoustic effects, which Waves has patented in the USA and other countries worldwide.

MaxxBass utilizes the principle of the missing fundamental, which creates the sensation of low frequencies by generating a carefully calculated series of harmonics designed to simulate the auditory experience caused by the missing fundamental pitch. These harmonics extend the virtual frequency response up to two-third or $1^1/_2$ octaves below the physical speaker cutoff frequency without perceived distortion or increased power consumption.

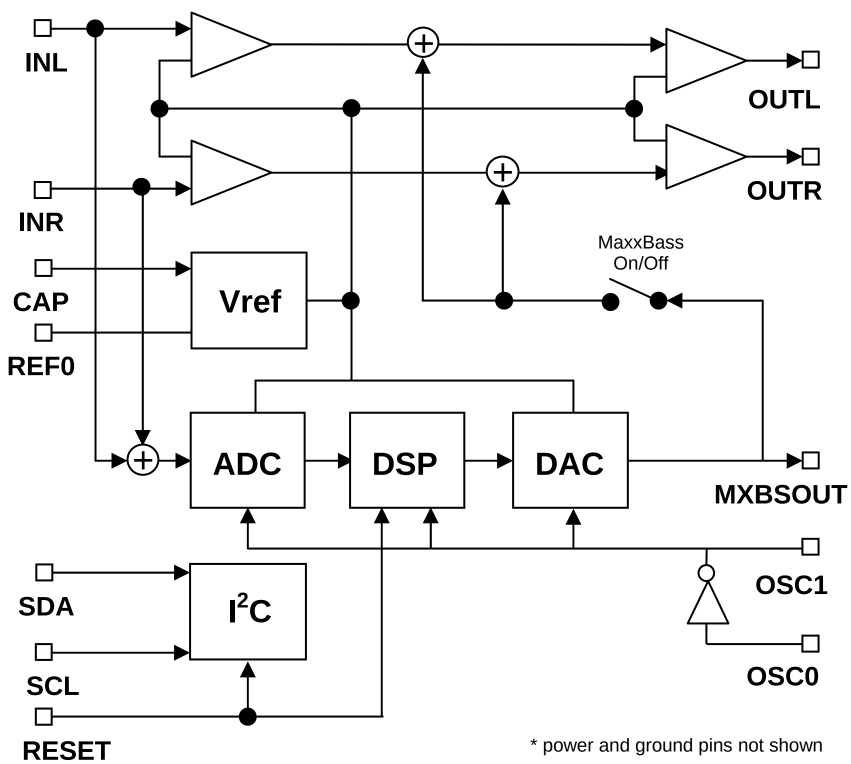
The MX3000DS is the second generation, mixed-signal ASIC (Application Specific Integrated Circuit) that includes a MaxxBass optimized DSP, sigma delta ADC, DAC and high quality analog circuits. It provides a low cost, stand-alone solution for implementing MaxxBass. It is ideal for extending bass frequency response in consumer products such as portable loudspeakers, LCD TVs, mini-compo, car audio, subwoofers and other audio products where size and cost constraints limit the available bass frequency response.

1.0 MX3000DS OPERATION

1.1 Principle of Operation

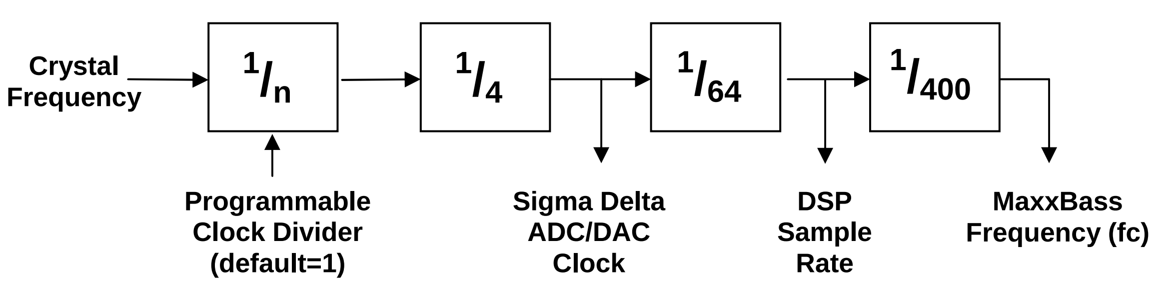
The MaxxBass algorithm is implemented digitally on a mono L+R signal. The MaxxBass harmonics are generated in a custom DSP and added back into the original left/right signals as shown in Figure 1.

Figure 1: MX3000DS Functional Diagram



All internal clocks are established from a crystal oscillator, ceramic resonator or other clock source. The relationship between the clock frequency input, sigma delta ADC/DAC converter clock, DSP sample rate and MaxxBass Frequency is shown in Figure 2.

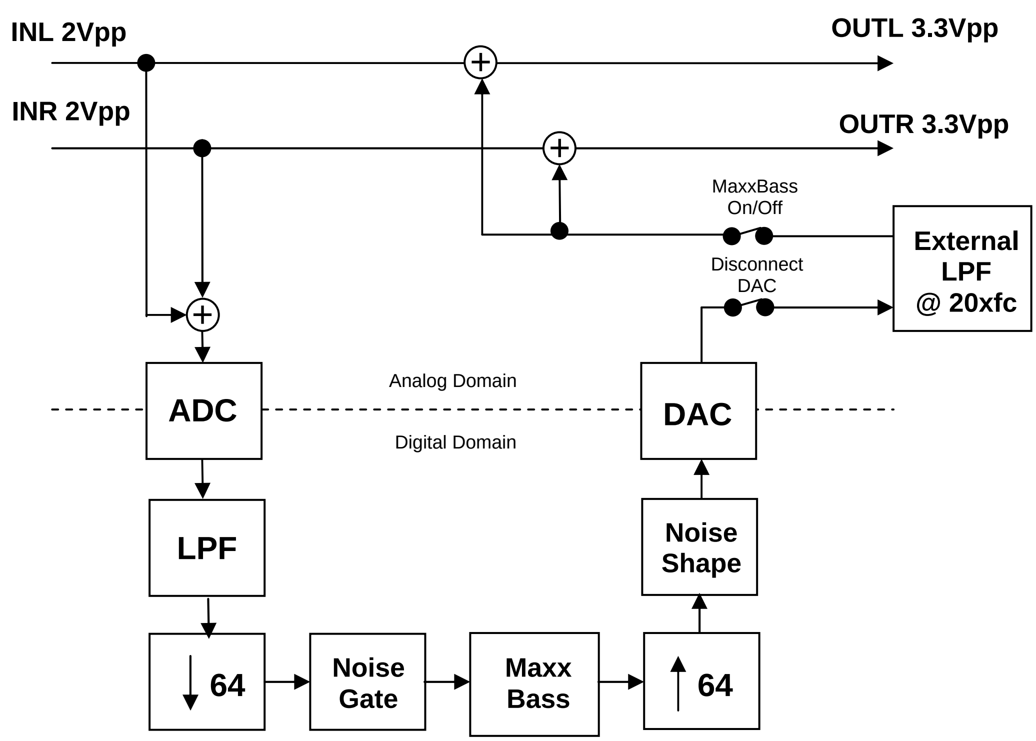
Figure 2: Clock and Sample Rate Generation



The MaxxBass signal flow is shown in Figure 3. The digital domain contains two signal paths, one for MaxxBass harmonic generation at the DSP sample rate and another at the ADC sample rate (not shown). The MaxxBass signal path is first low pass filtered at the MaxxBass Frequency and then decimated by 64. The MaxxBass harmonics is then generated and the resulting signal is interpolated. The latency of the MaxxBass harmonics signal path is 3 samples at the DSP sample rate. The MaxxBass harmonics latency will vary between 10 and 50 microseconds based on the clock frequency, which is unperceivable to the listener.

The ADC rate digital signal path is provided (not shown), which implements a high pass filter at the MaxxBass Frequency when added back into the original signal. This path also implements the subwoofer low pass filter at 2 * MaxxBass Frequency, which is enabled by a software command. The latency of this signal path is only a few samples at the much higher sigma delta sample rate.

Figure 3: MX3000DS Signal Flow Diagram



1.2 Operational States

1.2.1 Normal State

This state is automatically enabled after reset. The device is fully functional in this state.

When the device exits reset the SDA and SCL pins are read and this information is used to set the MaxxBass Intensity.

Table 1. MaxxBass Intensity Levels After Reset

SDA pin	SCL pin	Intensity % and level
‘1’	‘1’	100% - level 63
‘1’	‘0’	75% - level 47
‘0’	‘1’	50% - level 31
‘0’	‘0’	100% - level 63

When using the device with an I^2C host, SDA and SCL pins must stay at ‘1’ when exiting reset. This sets Intensity to 100% or level 63. The Intensity can then be changed by software commands.

1.2.2 Reset State

When the reset pin is pulled down, the device enters reset. During reset the analog passthrough functionality is not affected, but MaxxBass processing is OFF. All internal clocks are stopped.

When the reset pin reaches a high state, the device reads SDA and SCL pins and sets the MaxxBass Intensity according to Table 1.

The MX3000CS is equipped with a new analog voltage monitor at the reset pin, which ensures a robust behavior that is desirable during power on and off.

1.3 Setting MaxxBass Frequency and Clock Frequency

MaxxBass is a loudspeaker compensation algorithm that should be tuned to the target loudspeaker system. The most critical parameter for the MaxxBass algorithm is the MaxxBass Frequency.

The designer chooses a clock frequency to generate a particular MaxxBass Frequency according to the following equation:

$$\text{Clock} = \text{MaxxBass Frequency (fc)} \times \text{n} \times 256 \times 400$$

n is a programmable clock divider. It has a default setting equal to 1 and will always equal 1 in applications without an I^2C host.

The clock can be provided with a crystal oscillator, a ceramic resonator or an externally generated clock.

The MaxxBass Frequency should always be less than the loudspeaker roll-off frequency (-3dB point). The exact choice of MaxxBass Frequency should be decided by the designer based on listening tests with several common frequencies. A good starting point when selecting the MaxxBass Frequency is 25% less then the cutoff of the load speaker.

For example:

A loudspeaker with a roll-off frequency (f3) of 90Hz should start with a MaxxBass Frequency at about 70Hz (25% less then the speaker cutoff frequency)

The clock frequency that would be provided to the MX3000DS in this case should be:

$$Clock = Fc \times n \times 256 \times 400 = 70 \times 1 \times 102400 \approx 7.2Mhz$$

This result gives the designer a good starting point on for evaluating MaxxBass. It is recommended that the designer also evaluate performance with slightly and lower frequency clocks, maybe 6.0 to 8.0 MHz. The fine tuning to clock frequency is dependant on not only f3, but also the slope of the speaker roll-off and the type of subject bass sound desired. It is often desirable to set up a short evaluation test with several frequencies with not only engineering, but marketing input.

Table 1 provides suggested values for the required resonator/clock frequencies as a function of physical speaker cutoff (f3). A variety of MaxxBass cutoff frequencies are shown as well the perceived bass improvement (virtual cutoff frequency) up to 1.5 octaves below f3.

Table 1: Clock Frequency vs MaxxBass Frequency

Physical spkr cutoff	MaxxBass Cutoff	Clock Freq	Virtual Cutoff
60 Hz	42 – 54 Hz	4.3 – 5.5 MHz	20 Hz
80 Hz	56 – 72 Hz	5.7 – 7.4 MHz	27 Hz
100 Hz	70 – 90 Hz	7.2 – 9.2 MHz	33 Hz
120 Hz	84 – 108 Hz	8.6 – 11.0 MHz	40 Hz
145 Hz	101 – 120 Hz	10.3 – 12 MHz	48 Hz
170 Hz	119 – 130 Hz	12.2 – 13 MHz	57 Hz
200 Hz	135-150 Hz	13.8 – 15.4 MHz	65 Hz

1.4 External MXBSOUT Capacitor

An external capacitor, Crc, is placed on the output of the MXBSOUT pin. This capacitor should be set to 15nF regardless of MaxxBass Frequency and be placed close to the MXBSOUT pin as possible.

2 HARDWARE DESIGN

The MX3000DS is a mixed signal device with stereo analog input and output. It requires minimum external components to complete the design.

Since the MX3000DS combines both DSP, sigma delta ADC/DAC and high quality analog it is sensitive to PCB layout. It is strongly urged that designers read and follow detailed MaxxBass Development Recommendations and Reference Designs available at www.maxx.com to obtain the best possible performance.

Additionally Waves offers several reference designs which combine the MaxxBass ASIC with a suitable amplifier for low cost applications.

2.1 PCB Layout Recommendations

Since the MX3000DS is a mixed signal device with high speed digital clocks for the integrated sigma delta A/D, D/A and DSP, it is very important to have a noise free clock signal or the ASIC may become unpredictable due to parasitic oscillations. In practice this will keep the MaxxBass functionality implemented in digital portion of the ASIC from operating particularly during the boot or start-up process.

In order to eliminate this problem, these considerations must be taken in the PCB layout. The basic layout recommendations are listed below. When properly implemented a standard 2 layer PCB provides noise immunity to provide high quality results.

1) A massive ground plane should be provided and all empty spaces between traces on both sides of PCB to be filled by ground copper.

2) Wide traces (of at least 15-20 mils) should used on all lines across the board.

3) All parts related to MaxxBass ASIC should be placed as near as possible to the MX3000DS pins.

4) Decoupling caps have to be placed as near as possible to the MX3000DS power pins.

5) DC Blocking caps on the I/O must be placed near the input and output MX3000DS pins.

6) The 1uF capacitor connected to pin 16 should be placed as close as possible to the pin.

7) 10 kohm load should be applied after the DC blocking caps at the MX3000DS output pins.

Waves can provide a suggested PCB layout design and source files. It is suggested that these may be used as a starting point or reference for the customers' layout to reduce design effort and risk in the PCB design.

3.0 SOFTWARE COMMANDS

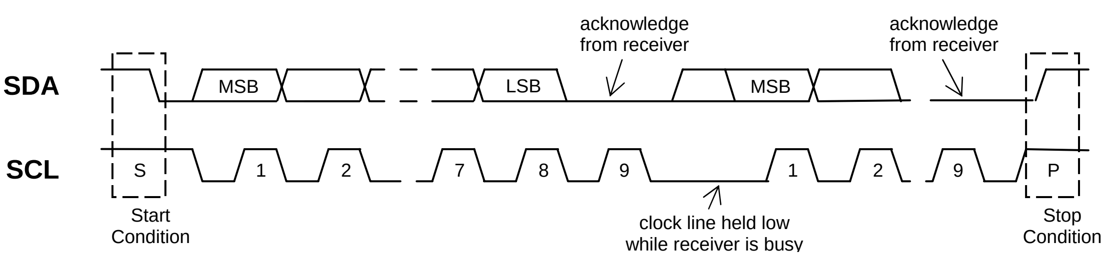
The MX3000DS is fully functional after reset and no software commands are required for proper use. For systems with I^2C hosts several software commands are available that provide additional features. These programmable features include clock divider, subwoofer low pass filter, intensity control, power-on output delay, noise gate and other features.

3.1 I^2C Command Format

The I^2C serial host interface operates as a simple I^2C slave unit. It is only able to receive bits and acknowledge the receipt. This is implemented with a serial data (SDA) pin and a serial clock (SCL) pin.

The I^2C protocol transfers a byte of data using a most significant bit (MSB) format. The transfer begins with a START-condition, ends by a STOP-condition and the slave (MX3000DS) genrates an acknowledge (ACK) signal after receiving all 8 bits. The host generates the clock on SCL line to transfer messages. Both SDA and SCL are of open collector type, so pull-up resistors are needed on the lines. The device only pulls the lines down if logic level zero is sent. The data transfer method is illustrated in Figure 4.

Figure 4: Data transfer on the I^2C Bus



The MX3000DS I^2C commands are always sent in three adjacent bytes – address, mode and data as shown in Figure 7.

Figure 7: MX3000DS Command Format

S	Slave Address 7-bits	R/W	A	Data 8-bits	A	Data 8-bits	A	P
	Byte 1 - Address			Byte 2 - Mode		Byte 3 - Data		

Shaded box: from master to slave
White box: from slave to master

A = acknowledge (SDA LOW), not acknowledge (SDA HIGH)
S = START
P = STOP condition

The first byte is a 7 bit slave address and the LSB is a R/_W bit. Since the MX3000DS can only read, the LSB bit of the slave address byte must be ‘0’. The address byte for the MX3000CS is “1110 0110” as shown in Table 3.

Table 3: Byte 1 - Address

Address Byte	Mode
"1110 0110"	Slave address for MX3000DS

If a valid slave address byte is received, then the second byte of the command controls the MX3000DS modes. Other bits labeled 'x' are ignored.

Table 4: Byte 2 - Mode

Mode Byte	Mode
"00xx xxxx"	Control for intensity level
"01xx xxxx"	Control for MaxxBass ON/OFF
"1111 0xxx"	Control for Output Delay ON/OFF
"1111 1xxx"	Control for Clock Divider and Noise Gate

If a valid mode-byte was received, then the third byte of the MX3000DS I^2C command will be considered valid data as shown in Table 5.

Table 5: Byte 3 - Data

Mode Byte	Data Byte	Description	After Reset
"00xx xxxx"	Bits (7:2)	MaxxBass intensity control (0 to 63)	"1111 11xx"
"01xx xxxx"	Bit 7	MaxxBass (ON-0 / OFF-1)	"0000 000x"
"01xx xxxx"	Bit 3	*Subwoofer LPF (ON-1 / OFF-0*)*	"0000 000x"
"1111 0xxx"	Bit 7	*Output Delay (OFF-1 / ON –0)**	"0xxx xxxx" *note
"1111 1xxx"	Bits (7:4)	*Clock Divider**	"0001 1111"
"1111 1xxx"	Bits (3:2)	*Noise Gate Threshold**	"0001 1111"
"1111 1xxx"	Bits (1:0)	*Noise Gate Gain**	"0001 1111"

* A power up voltage monitor detection circuit sets this bit to '0'. Normal reset does not affect this bit.

3.2 Command Functions

3.2.1 MaxxBass Intensity Level

Intensity controls the strength of the MaxxBass effect. Intensity level varies between 0 and 63, with 63 being maximum level (100%). The default value after reset is 63, but this can with the following software commands.

Commands	Address Byte	Mode Byte	Data Byte
Set Intensity = 47 (75%)	"1110 0110"	"0000 0000"	"1011 1100"
Set Intensity = 31 (50%)	"1110 0110"	"0000 0000"	"0111 1100"

3.2.2 Clock Divider*

A programmable clock divider has been added to the MX3000DS version. The following formula determines the MaxxBass Frequency (fc) based on clock input and clock divider value.

$$\text{MaxxBass Frequency (fc)} = \frac{\text{Clock Frequency}}{n \times 256 \times 400}$$

By using a software command the MX3000DS can set a clock divider value of n=1, 2, 3,…,10. The default value is 1.

Table 6 lists the effect of the clock divider value to MaxxBass Frequency (fc), when a 25.6MHz crystal is used.

Table 6 MaxxBass Frequencies using 25.6 MHz clock

Divider Value	Data Byte	MaxxBass Frequency (fc)
1	“0001 xxxx”	250 Hz
2	“0010 xxxx”	125 Hz
3	“0011 xxxx”	83 Hz
4	“0100 xxxx”	62.5 Hz
5	“0101 xxxx”	50 Hz
6	“0110 xxxx”	41.7 Hz
7	“0111 xxxx”	35.7 Hz
8	“1000 xxxx”	31.25 Hz
9	“1001 xxxx”	27 Hz
10*	“1010 xxxx”	25 Hz

* The MaxxBass frequency should not be set to a a frequency lower then 25Hz.

Commands	Address Byte	Mode Byte	Data Byte
Set MaxxBass Freq = 125Hz	“1110 0110”	“1111 1000”	“0010 1111”
Set MaxxBass Freq = 83Hz	“1110 0110”	“1111 1000”	“0011 1111”

Note:
When the MaxxBass Intensity command is used after the clock divider is changed to a non-default (divide by 1) state, the Intensity command does not correctly change the Intensity parameter of the algorithm.

This sensitive to command order only occurs between the Clock Divider command and the MaxxBass Intensity command. No other combination of commands is affected.

In order to avoid this problem the MaxxBass Intensity command must be issued before the Clock Divider command. If the application uses a non-default clock divider state (divide by 2, 3, 4 etc), then the clock divider needs to be set back to 1 prior to changing the MaxxBass Intensity.

The Clock Divider can then be changed as desired. The host controller should also mute the amplifier during this process.

Below is an example of how to dynamically change the MaxxBass Intensity Level when a non-default (not 1) clock divider is used.

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Commands	Address Byte	Mode Byte	Data Byte
Mute Amplifer	Not applicable		
Set Clock Divider to 1	E6	F8	1F
Set MaxxBass Intensity to 50%	E6	00	7B
Set Clock Divider to 2	E6	F8	2F
Unmute Amplifier	Not applicable		

3.2.2 Subwoofer Low Pass Filter

When enabled, the subwoofer low pass filter provides a 3rd order, -18dB/octve low pass filter with a corner frequency at 2 * MaxxBass Frequency.

Commands	Address Byte	Mode Byte	Data Byte
Set Subwoofer LPF ON	“1110 0110”	“0100 0000”	“x000 1000”

When working in subwoofer mode the designer should apply the input signal to <u>just to one input pin</u> (LIN) and use the opposite channel output (ROUT).

The unused input (RIN) should be grounded with capacitor and the unused output (LOUT) should be unconnected or left floating.

3.2.3 Output Buffer Delay

This function initiates only after power up by internal power up voltage monitors. It disables the audio output buffers and begins an internal counter. Once counter reaches a fixed value the audio output buffers are enabled. The delay is linearly dependent on the clock frequency as shown in the following equation and table.

Power Up Delay (s) = 4,194,304 / Clock Frequency (Hz)

Table 7 Power Up Delay

Delay	Clock Freq
280 msec	15 MHz
419 msec	10 MHz
524 msec	8 MHz
839 msec	5 MHz

During power up an offset voltage is created on the output lines which can create a power up "pop". The purpose of this delay is to allow the output lines to stabilize slowly and eliminate any pops or clicks.

The default setting for output buffer delay is ON, although this can be overridden by an I^2C command. This may be desirable in applications where separate power up or mute control of the power amplifier is available, so the power of sequence of the MaxxBass ASIC can occur before the power amplifier which would also eliminate power on pops without a delay.

Commands	Address Byte	Mode Byte	Data Byte
Set Output Delay OFF	"1110 0110"	"1111 0000"	"1000 0000"

3.2.4 Noise Gate

This function is used to lower the noise floor when no input signal is present. Without the noise gate, the MaxxBass algorithm includes compressors that provide maximum gain with no input signal is present. The noise gate operates prior to the compressor and is used to lower the noise floor when no input signal is provided.

The noise gate function has two adjustable parameters, Noise Gate Threshold and Noise Gate Gain.

The Noise Gate Threshold is set between –66dBu and –84dBu by setting bits (3:2) in the data byte as shown below. The default value after reset is –66 dBu or "11". If the signal level to the noise gate is above the threshold, the noise gate is inactive.

Table 8 Noise Gate Threshold

Data Byte	Threshold
"0001 <u>00</u>xx"	-84 dBu
"0001 <u>01</u>xx"	-78 dBu
"0001 <u>10</u>xx"	-72 dBu
"0001 <u>11</u>xx"	- 66 dBu

If the signal strength is below the Noise Gate Threshold, the noise gate lowers noise floor by attenuating the signal by Noise Gate Gain. The Noise Gate Gain is set between –12 dB and –30 dB using bits (1:0) as shown in Table 9. The default Noise Gate Gain is –30 dB or “11”.

Table 9 Noise Gate Gain

Data Byte	Gain
“0001 xx00”	-12 dB
“0001 xx01”	-18 dB
“0001 xx10”	-24 dB
“0001 xx11”	- 30 dB

Below is an example of an I^2C Command to change the Noise Gate parameters.

Commands	Address Byte	Mode Byte	Data Byte
Set NG Threshold = -78 dBu and Gain=-30db	“1110 0110”	“1111 1000”	“0001 0111”

4.0 ELECTRICAL SPECIFICATIONS

4.1 Absolute maximum ratings

Parameter	Min	Max	Units
Operating temperature. -All parameters inside limits -Functionality is guaranteed. Parameters may have some differences compared to specifications.	 0 -30	 +70 +85	 °C °C
Junction and storage temperature range	-65	+150	°C
Max power dissipation (Ta = +85°C)		200	mW
Current on any pin to avoid latch-up 1)	-100	+100	mA
ESD protection	2000		V
Supply voltage , analog (AVDD) 2)	-0.3	4.0	V
Supply voltage digital (DVDD) 2)	-0.3	4.0	V
Negative supply difference (DVSS to AVSS) 3)	-0.3	0.3	V
Input pin voltage, IO	-0.3	DVDD+0.3	V
Input pin voltage, analog	-0.3	AVDD+0.3	V

1) OUTL and OUTR pins only require a minimum of 300 ohms of resistance. Any common amplifier or op amp input resistance meets this requirement.
2) The damages are not caused even though other operating voltages are not at their operational limits. AVDD and DVDD must have approximately the same potential. Otherwise the power consumption may increase.
3) Due to p-type substrate all ground supplies must be in the same potential to avoid latch-up. Latch-up will destroy the chip without a current limiter.
4) Analog and digital grounds must have the same voltage level.

4.2 General ratings

Parameter	Min	Max	Units
PSRR (20Hz - 20kHz), AVDD = 3.30V ± 50mV	40		dB
Digital input pin capacitance		8	pF
Digital output load capacitance 1)		30	pF

1) AC timings are fulfilled with these loads

4.3 Operating voltages and currents

Parameter	Min	Typ	Max	Units
AVDD	3.15	3.3	3.45	V
DVDD	3.15	3.3	3.45	V
Power-down-idle state 2)		8.5	10.5	mA
Reset state		8.7	10.5	mA
ACTIVE 1)		12.7	20	mA

1) Outputs loaded with 10K Ohm, clock input = 10 MHz
2) Requires command through the I^2C interface

4.4 DC characteristics of digital signals

Parameter	Min	Typ	Max	Units
Input high voltage	0.7 x DVDD		DVDD+ 0.3	V
Input low voltage	-0.3		0.3 x DVDD	V
Input leakage Current	-5.0		5.0	µA
High-level output voltage IOH = -1mA	0.7 x DVDD		DVDD	V
Low-level output voltage IOL = 1mA	GND		0.3 x DVDD	V

4.5 AC characteristics of digital signals

4.5.1 Oscillator

Parameter	Symbol	Min	Typ	Max	Units
Oscillator clock cycle	tOSC	39		195	ns 1)
Clock duty cycle		45		55	%
Oscillator setup time	tSTABIL		4096		tOSC

1) MaxxBass cutoff frequency fc (25 Hz – 250 Hz) is adjusted by the clock frequency.

4.5.2 Reset timing

RESET is active low.

Parameter	Symbol	Min	Typ	Max	Units
RESET setup time	tXRS	100			ns
RESET hold time	tXRH	100			ns
RESET pulse width	tXRI	100			ns

4.6 Analog IO

4.6.1 Levels at inputs

Parameter	Min	Typ	Max	Units
INL 1)		2.0	AVDD	Vpp
INR 1)		2.0	AVDD	Vpp

1) ac-coupled, typical values guarantee non-distortion operation

4.6.2 Levels at outputs

Parameter	Min	Typ	Max	Units
OUTL, 10 kohm to AGND 1)		3.0	AVDD	Vpp
OUTR, 10 kohm to AGND 1)		3.0	AVDD	Vpp
MXBSOUT, to AGND	0	305	610	μA

1) ac-coupled, typical values correspond to typical inputs in active mode

4.6.3 Output loading

Parameter	Min	Typ	Max	Units
OUTL to AGND C R 1)	 10		 300	 pF kohm
OUTR to AGND C R 1)	 10		 300	 pF kohm
MXBSOUT to AGND C		 15		 nF

1) ac-coupled load,

4.6.4 Input impedance

Parameter	Min	Typ	Max	Units
INL		13		kohm
INR		13		kohm

4.6.5 Gain

Parameter	Min	Typ	Max	Units
INL to OUTL, Reset State	-0.5	0.0	+0.5	dB
INR to OUTR, Reset State	-0.5	0.0	+0.5	dB

4.6.6 Crosstalk

Parameter	Min	Typ	Max	Units
INL to OUTR, 20-20000 Hz, MaxxBass OFF		-78	-60	dB
INR to OUTL, 20-20000 Hz, MaxxBass OFF		-78	-60	dB

Since MaxxBass processing is implemented on the mono signal, crosstalk measurements with MaxxBass ON is not a relevant measurement for the same reason measuring crosstalk is not relevant for stereo and 3D enhancement algorithms. MaxxBass applies processing that is targeted towards psycho-acoustic perception, and crosstalk measurements by itself is not enough to predict the perceived result. This is because other effects such as the relative phase of the crosstalk signal affect perception. Please perform listening tests with the MaxxBass ASIC, we believe there is no noticeable degradation of the stereo imaging, rather maybe even improved stereo imaging!

(1Khz crosstalk with MaxxBass ON will be -18 to -22dB, but the output will be out of phase and uncorrelated to the other output. As result it will not degrade the stereo imaging.)

4.6.7 Distortion

Parameter	Min	Typ	Max	Units
INL=0.6 Vpp, 1000 Hz 1)		-77	-70	dB
INR=0.6 Vpp, 1000 Hz 1)		-77	-70	dB

1) Reset state (analog direct path), load is a AC-coupled 10K Ohms

4.6.8 Noise

Parameter	Min	Typ	Max	Units
INL to OUTL, A-weighted, MaxxBass OFF		10 -97		µVrms dB
INR to OUTR, A-weighted, MaxxBass OFF		10 -97		µVrms dB
INL to OUTL, A-weighted, Reset State		15 -94	25 -89	µVrms dB
INR to OUTR, A-weighted, Reset State		14 -94	25 -89	µVrms dB
INL to OUTL, A-weighted, MaxxBass ON		15 -94	50 -83	µVrms dB
INR to OUTR, A-weighted, MaxxBass ON		15 -94	50 -83	µVrms dB

Signal measure test conditions: INL and INR connected to 2Vpp sine wave at 1KHz. Noise measurement test conditions: INL and INR connected to AGND with 10µF capacitor, AC-coupled 10K Ohm output load on LOUT and ROUT, and 10 MHz clock input (MaxxBass Fc=98 Hz).

Maximum measurements are test limits from the production (noisy) test environment. Substantial improvement can be made in an end customer application with the MX3000CS directly soldered on a properly designed PCB. Typical values are the measured results from properly designed PCBs. More details of the testing and frequency plots can be found in the technical paper titled, “MaxxBass Noise and Distortion Measurements”. This paper can be found at www.maxx.com.

The spectrum of the MX3000DS added noise is largely concentrated at lower frequencies, the majority of it below the physical speaker cutoff frequency. The industry standard A-weighting considers human hearing sensitivity to the noise, but it does not consider the high pass filter effect of the loudspeaker. Considering that MaxxBass is a speaker compensation technology, it is appropriate also to include the speaker response weighting on the noise output. If one includes this effect the overall SNR weighting would improve by approximately 6 dB from the A-weighted results above.

5.0 RoHS COMPLIANT PACKAGE

The MX3000DS is provided in a 16-pin SOIC using only green environmentally-friendly materials.

Legislation such as the European Union's RoHS (Restriction on Hazardous Substances) Directive require suppliers to provide components manufactured without hazardous materials.

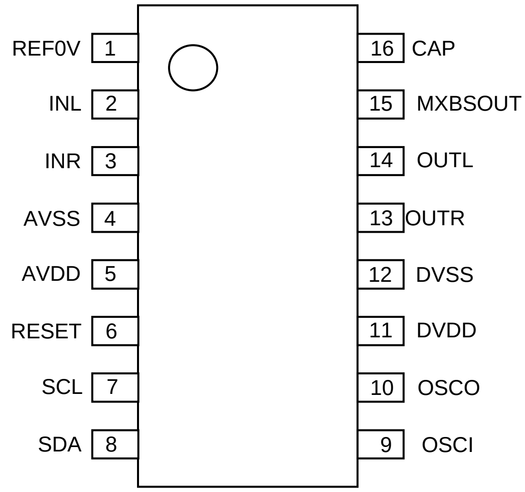
The MX3000DS was manufactured without the use of the following RoHS restricted materials.

- Heavy Metals
    - Cadmium and cadmium compounds
    - Lead and lead compounds
    - Mercury and mercury compounds
    - Hexavalent chromium compounds
- Brominated organic compounds
    - Polybrominated biphenyls (PBB)
    - Polybrominated diphenylethers (PBDE)

5.1 Pin description

Number	Name	Type	Description
1	REF0V	Power	Internal 0V reference.
2	INL	Analog Input	Left channel input
3	INR	Analog Input	Right channel input
4	AVSS	Power	Negative power supply for analog circuitry
5	AVDD	Power	Positive power supply for analog circuitry
6	RESET	Digital Input	Reset input, active low
7	SCL	Digital Input	Clock input of I^2C serial interface
8	SDA	Dig Input/Output	Data IO of I^2C serial interface, open drain
9	OSC1	Analog Output	Resonator output (2.56 – 25.6 MHz)
10	OSC0	Analog Input	Resonator input (2.56 – 25.6 MHz)
11	DVDD	Power	Positive power supply for digital circuitry
12	DVSS	Power	Negative power supply for digital circuitry
13	OUTR	Analog Output	Right channel output
14	OUTL	Analog Output	Left channel output
15	MXBSOUT	Analog Output	MaxxBass output. Connect to ext capacitor.
16	CAP	Analog Input	Bandgap reference. Connect to 1uF cap.

5.2 Pin Out Diagram



5.3 Order and Shipping Quantities

The MX3000DS is offered in two types of containers – tubes and tape-and-reel. The Quantity per Container is the minimum shipping increment.

Ordering Number	Device Container	Qty per Container*	Qty per Shipping Carton
MX3000DS	tube	48	9,600 (200 tubes)
MX3000DST	tape and reel	2,500	12,500 (5 reels)

5.4 Package Marking

Both MX3000DS and MX3000DST ordering part numbers are marked the same as shown below.

WAVES
MX3000DS
XXXXX YYWW

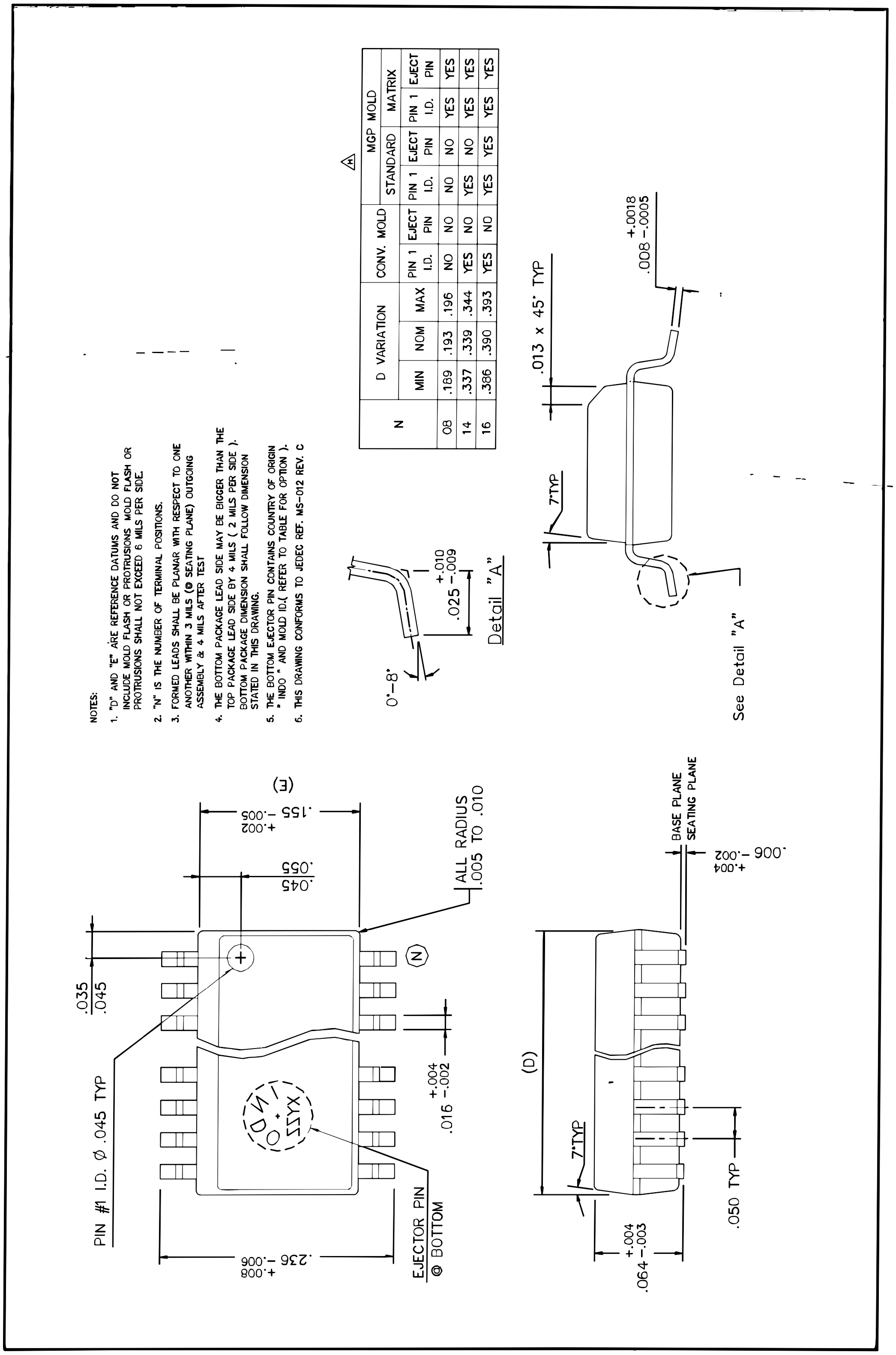
YYWW = packaging year and week

XXXXX = lot number

The orientation of marking to pin 1 is not guaranteed.

5.5 Package Dimensional Specification

The MX3000DS is packaged in a 16-pin 150mil SOIC. The dimensional specifications are defined in inches in the following diagram.



N	D VARIATION MIN	NOM	MAX	CONV. MOLD PIN 1 I.D.	CONV. MOLD EJECT PIN	MGP MOLD STANDARD PIN 1 I.D.	MGP MOLD STANDARD EJECT PIN	MGP MOLD MATRIX PIN 1 I.D.	MGP MOLD MATRIX EJECT PIN
08	.189	.193	.196	NO	NO	NO	NO	YES	YES
14	.337	.339	.344	YES	NO	YES	NO	YES	YES
16	.386	.390	.393	YES	NO	YES	YES	YES	YES

6.0 LICENSE

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6. GOVERNING LAW. This Agreement shall be governed by the substantive laws of the state of Israel, with sole and exclusive jurisdiction vesting with the relevant courts of Israel.

7.0 WEB LINKS

Additional information on the MX3000DS may be viewed on-line at www.maxx.com.