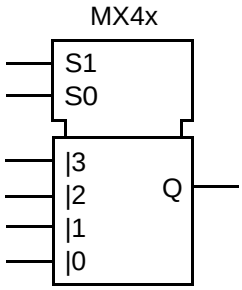
Description

MX4x is a family of four-to-one digital multiplexers.

Logic Symbol



Truth Table

I0	I1	I2	I3	S1	S0	Q
L	X	X	X	L	L	L
H	X	X	X	L	L	H
X	L	X	X	L	H	L
X	H	X	X	L	H	H
X	X	L	X	H	L	L
X	X	H	X	H	L	H
X	X	X	L	H	H	L
X	X	X	H	H	H	H

HDL Syntax

Verilog ..... MX4x *inst_name* (Q, I0, I1, I2, I3, S0, S1);

VHDL..... *inst_name*: MX4x port map (Q, I0, I1, I2, I3, S0, S1);

Pin Loading

Pin Name	Equivalent Loads			
	MX41	MX42	MX44	MX46
I0	1.0	1.0	1.0	1.0
I1	1.0	1.0	1.0	1.0
I2	1.0	1.0	1.0	1.0
I3	1.0	1.0	1.0	1.0
S0	3.3	3.3	3.3	3.3
S1	3.3	2.1	2.1	2.1

AMI5HG 0.5 micron CMOS Gate Array

Size And Power Characteristics

Cell	Equivalent Gates	Power Characteristics[a]	
		Static I_{DD} (T_J = 85°C) (nA)	EQL_{pd} (Eq-load)
MX41	8.0	TBD	15.3
MX42	9.0	TBD	19.9
MX44	11.0	TBD	24.9
MX46	12.0	TBD	23.2

a. See page 2-15 for power equation.

Propagation Delays (ns)

Conditions: T_J = 25°C, V_{DD} = 5.0V, Typical Process

	Number of Equivalent Loads		1	4	8	13	17 (max)
MX41	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.69 0.75	0.82 0.92	0.95 1.10	1.09 1.31	1.19 1.46
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.80 1.00	0.92 1.16	1.05 1.34	1.20 1.54	1.31 1.69
	Number of Equivalent Loads		**1**	**8**	**15**	**22**	**30 (max)**
MX42	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.65 0.70	0.79 0.84	0.89 0.95	0.97 1.04	1.06 1.14
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.76 0.89	0.91 1.03	1.01 1.14	1.10 1.24	1.19 1.35
	Number of Equivalent Loads		**1**	**14**	**28**	**42**	**56 (max)**
MX44	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.69 0.74	0.80 0.84	0.90 0.95	1.00 1.06	1.11 1.18
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.80 0.95	0.90 1.09	1.00 1.18	1.08 1.27	1.18 1.36
	Number of Equivalent Loads		**1**	**21**	**42**	**62**	**83 (max)**
MX46	From: Any Ix Input To: Q	t_{PLH} t_{PHL}	0.75 0.78	0.87 0.91	0.96 1.02	1.05 1.12	1.13 1.22
	From: Any Sx Input To: Q	t_{PLH} t_{PHL}	0.84 1.00	0.97 1.12	1.06 1.23	1.15 1.33	1.22 1.42

Delay will vary with input conditions. See page 2-17 for interconnect estimates.

Logic Schematic