MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX429

Standard Protocol MSK Modem for Trunked Radio

Features

- Full-duplex Operation
- Generates Preamble/Detects Carrier
- Flags both Control & Traffic Frames
- Detects Errors/Outputs Syndrome
- High Data Throughput for 2-way Radio

Applications

- Standard Protocol Radio Trunking Systems
- Mobile Radio SELCALL, ANI & Status Data
- Wireless Intercom Traffic Control
- MX429: British MPT1327 Signaling

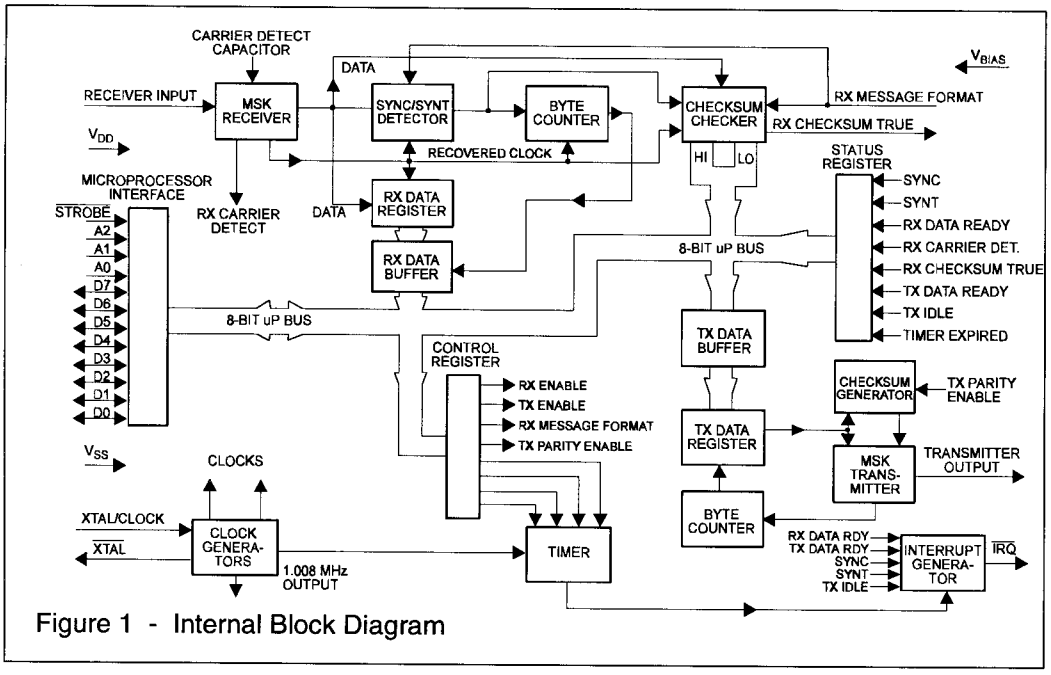

Figure 1 - Internal Block Diagram

AVAILABLE PACKAGES

MX429LH
24 pin PLCC

MX429J
24 pin CDIP

MX429P
24 pin PDIP

Description

The MX429 is a single-chip, low-power CMOS 1200 baud MSK Modem, designed primarily for use in trunked radio, telemetry and packet radio applications. The MX429 has been designed to conform to the MPT1317/1327 UK Band III trunked radio protocols.

The device is full-duplex at 1200 baud. An 8-bit parallel microprocessor interface is also provided. The on-chip programmable timer may be set for interrupt periods of 8 to 120 bits. Preamble and an error check word are automatically generated in Transmit mode. Error checking is performed and the 16-bit SYNC or SYNT words are detected in Receive.

An on-chip xtal/clock generator which requires an external 4.032 MHz xtal or clock input provides 4.032 and 1.008 MHz outputs. In addition, it performs all modem timings. The MX429 provides powersave circuitry and only requires a single 5 volt power supply.

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PIN FUNCTION TABLE

Pin J,P	Pin LH	Function
1	1	V_{BIAS}: The internal circuitry bias line, held at $V_{DD}/2$. This pin must be decoupled to V_{SS} by capacitor C_4. See Figure 3.
2	2	TRANSMIT OUTPUT: The 1200 baud, 1200/1800Hz MSK TX output. When not enabled by the Control Register (D_0), the output is set to a high impedance state.
3	4	RECEIVER INPUT: The 1200 baud received MSK signal input. The 1200/1800 Hz audio to this pin must be a.c. coupled via capacitor C_3. See Figure 3.
5	5	V_{DD}: Positive supply. A single +5V regulated supply is required. It is recommended that this power rail be decoupled to V_{SS} by capacitor C_6. See Figure 3.
6	6	CARRIER DETECT TIME CONSTANT: The on-chip carrier detect integration function requires a capacitor, C_5, to V_{SS}, together with a resistor, R_2, to V_{DD}, that determine the carrier detect response time.
7	7	$\overline{XTAL}$/CLOCK: The input to the clock oscillator inverter. A 4.032 MHz Xtal or externally derived clock pulse input should be connected here. See Figure 3.
8	8	XTAL: The output of the 4.032 MHz clock oscillator.
9	9	D_0: Microprocessor Data Interface
10	10	D_1:
11	11	D_2:
12	12	D_3: These eight lines are used by the device to communicate with a
13	13	D_4: microprocessor, and with the A_0, A_1 and A_2 inputs
14	14	D_5: determining register selection.
15	15	D_6:
16	16	D_7:
17	17	A_0: REGISTER SELECTION: These inputs, with the A_2 input,select the
18	18	A_1: required register to the data bus as shown in Table 1 (below).
19	19	$\overline{STROBE}$: This input performs the dual functions of selecting the device for Read or Write and strobing data in or out. It should be generated by gating high order address bits with a read-write clock. This device is selected when $\overline{STROBE}$ = 0 (see Figure 5). NOTE: If data at inputs D0-D7 changes during $\overline{STROBE}$ an interrupt may occur.
20	20	A_2: This input determines which internal registers are connected to the Data Interface pins (D0-D7) during $\overline{STROBE}$ (see Table 1 and Figure 5).
21	21	$\overline{IRQ}$: Interrupt Request. This line will go to a logic "0" when an interrupt occurs. This output can be "wire OR'd" with other active low components (100 kΩ pullup to V_{DD}).The conditions that cause the interrupts are indicated at the Status Register and are as follows: Timer Expired, RX Data Ready, TX Data Ready, TX Idle, RX SYNC Detect, RX SYNT detect

Table 1

Register	A_2	A_0	A_1
Control	0	1	1
Status	1	1	1
RX Data	1	0	1
TX Data	0	0	1
Syndrome Low	1	0	0
Syndrome High	1	1	0

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PIN FUNCTION TABLE

Pin		Function
J,P	LH	
23	22	V_{SS}: Negative Supply (GND)
24	23	CLOCK ÷ 4: A 1.008 MHz ($X_1 \div 4$) clock is available at this output for external circuit use. Note the source impedance and source current limits.
4,22	3,24	These pins are not connected. Leave open circuit.

Modems in Mobile Data Signaling...An Introduction

Digital Code Format

The MPT1327 Signaling Standard for Trunked LMR Systems protocol is used by the MX429 for communication between a trunking system controller (TSC) and users' radio units. The data stream format is summarized in Figure 2.

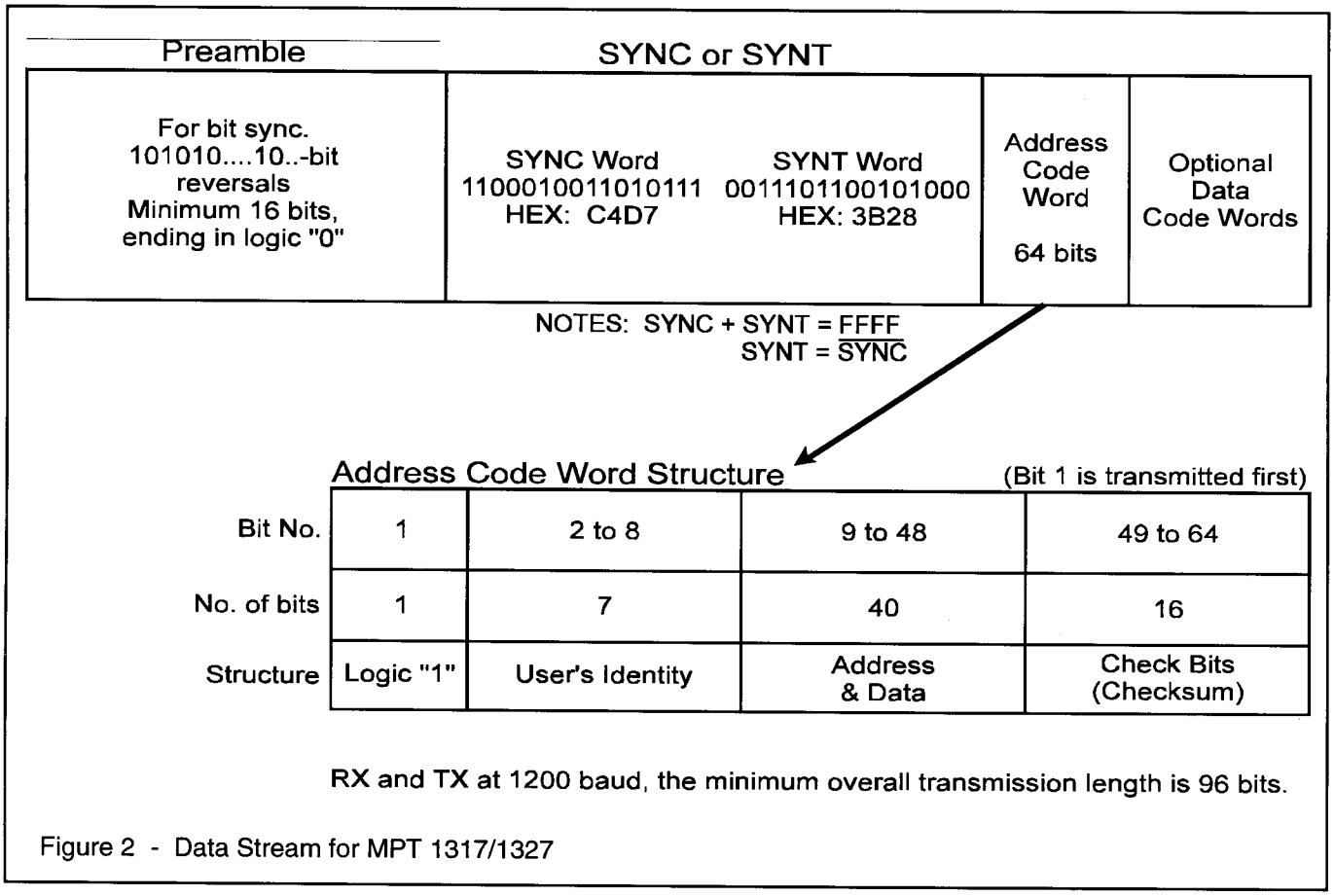

Figure 2 - Data Stream for MPT 1317/1327

Modems in Mobile Data Signaling...An Introduction (Cont.)

Operation

The MX429 can be used in full-duplex mode in conjunction with a host microprocessor, The µP operates on the data, while the MX429 handles all other signaling routines and requirements.

In the TX mode, the MX429 will:

(1) Internally generate and transmit a preamble for system bit synchronization,

(2) Accept from the host and transmit a 16-bit SYNC or SYNT word,

(3) Accept from the host and transmit 6 bytes of data (Address Code Word) and, upon a software command,

(a) internally calculate and transmit a 2-byte checksum based on the previous 6 data bytes, or

(b) disable internal checksum generation and allow continuous data transmission, and

(4) Transmit one "hang bit" and go idle when all loaded data traffic has been sent (followed by a "TX Idle" interrupt).

In the RX mode, the MX429 will:

(1) Detect and achieve bit synchronization within 16 bits,

(2) Search for and detect the 16-bit SYNC or SYNT word,

(3) Output all received data after SYNC/SYNT in byte form, and

(4) Upon a software command (RX Message Format), use the received checksum to calculate the presence (if any) of errors and advise the host with an interrupt and a 16-bit Syndrome word.

Note: In the RX mode, a software command tells the MX429 to expect either a SYNC/SYNT word every 8 received bytes (6 data + 2 checksum) or a continuous data stream. Normally the SYNC word is used on the Control channel and the SYNT word is used on the Traffic data channel.

Non-MPT Application (Full-Duplex)

The functions described here can be accessed via the commands and indications detailed in the Register Instructions pages.

Transmit: When enabled, the device transmits a "101010...010" preamble until data for transmission is loaded by the host microprocessor. The MX429/529 will transmit 6 bytes of the loaded data followed by a 2 byte checksum based on that data. As long as TX data is being loaded, the transmitter will transmit in the 6 byte data/ 2 byte checksum format.

Automatic checksum generation can be inhibited by a software command, allowing transmission of continuous data streams.

Receive: A 16-bit SYNC or SYNT word is required (see note above) before output of data bytes. The modem receiver will then output continuous bytes of data. After every 6 bytes, a 2-byte checksum word will be generated, which can be ignored or used for error checking.

Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

The Control Register, when selected, directs the modem's operation as described below.

Bit	Description	Function	Set = logic "1" (High)	Clear = logic "0" (low)
Bit 0 D_0	**TX Enable ***	**Set** - D_0 enables the transmitter for operation. A "0-1" transition causes bit synchronization and the start of 1010.....10 preamble pattern transmission. At least one byte of preamble will be transmitted. If data is loaded into the TX Data Buffer before one byte has been sent, then that data will follow. Otherwise, whole bytes of preamble will continue until data is loaded. **Clear** - The Transmitter Output pin is set to a high impedance and no transmitter interrupts are produced.		

Control Register $A_1 = 1$ $A_0 = 1$ $A_2 = 0$ Write Only

Bit 1 TX Parity Enable (D_1)

Set - D_1 indicates to the transmitter that 2-byte checksums are to be generated by the modem. A "0-1" transition starts checksum generation on the next six bytes loaded from the TX Data Buffer into the TX Data Register. Checksum generation continues for every six bytes loaded until this bit is cleared. The transmitter will send the generated checksum (2 bytes) after the last of each 6 bytes have been sent. If an underrun (no more data loaded) condition occurs before 6 bytes have been loaded, checksum generation will abort, the transmission will cease after one "hang" bit has been sent, and Bit 4 in the Status Register (TX Idle) will be set. No checksum will be transmitted.
Clear - No checksum generation is carried out and the host may supply the checksum bytes. The output is then "as written."

Bit 2 RX Enable * (D_2)

Set - D_2 enables the receiver for operation. No data is produced (i.e. no RX Ready interrupts) until a SYNC or SYNT word is found in the received bit stream.
Clear - The receiver is disabled and all interrupts caused by the receiver are inhibited.

Bit 3 RX Message Format (D_3)

Set - D_3 is sampled after a checksum has been received and allows the host to control the way the receiver handles the following data bits. If set, the receiver will assume that the next 6 bytes are data and will start error checking accordingly.
Clear - The receiver will stop data transfer to the host after the 2 checksum bytes until another SYNC or SYNT frame word is received.

Bit 4 Timer LSB (D_4)

Bit 5 Timer (D_5)

Bit 6 Timer (D_6)

Bit 7 Timer MSB (D_7)

These 4 bits control the timer as follows:

D_7	D_6	D_5	D_4	
0	0	0	0	Reset Counter and disable timer interrupts
0	0	0	1	Count and interrupt every 8 bits
0	0	1	0	" " " 16 bits
0	0	1	1	" " " 24 bits
0	1	0	0	" " " 32 bits
0	1	0	1	" " " 40 bits
0	1	1	0	" " " 48 bits
0	1	1	1	" " " 56 bits
1	0	0	0	" " " 64 bits
1	0	0	1	" " " 72 bits
1	0	1	0	" " " 80 bits
1	0	1	1	" " " 88 bits
1	1	0	0	" " " 96 bits
1	1	0	1	" " " 104 bits
1	1	1	0	" " " 112 bits
1	1	1	1	" " " 120 bits

If a new timer value is written to these inputs within 1 byte period of the last timer interrupt, the next timer period will be correct without first having to reset the timer. Otherwise, the timer must be reset to zero and then set to the new time.

***Note:** **Enabling Times** - The time taken to enable one section (receiver or transmitter) when both sections are initally disabled is 16 bit periods. If one section (receiver or transmitter) is already enabled this time is reduced to 1/2 bit period.

TX Enable - If using the internal TX Preamble generation circuitry, e.g. with the internal timer setting the preamble length, the device occasionally produces a TX Data Ready interrupt immediately after a TX Enable. Software should handle this by either:

1) Detecting that the Timer Interrupt status bit is not set and that it is not appropriate to load data for TX at that time.

or 2) By not using the timer, i.e. immediately after TX Enable, reading the status register and loading a byte of preamble. This resets any interrupt. The length of the preamble transmitted is now controlled by the number of bytes loaded.

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Status Register $A_1 = 1$ $A_0 = 1$ $A_2 = 1$ Read Only

When an interrupt is generated the $\overline{IRQ}$ output goes Low with the Status Register bits indicating the sources of the interrupt.

Bit	Description	Function	Set = logic "1" (High) Clear = logic "0" (low)
Bit 0 D_0	RX Data Ready		D_0, when set, causes an interrupt indicating that received data is ready to be read from the RX Data Buffer. This data must be read within 8 bit periods. **Set** - when a byte of data is loaded into the RX Data Buffer, if a frame (SYNC/SYNT) word has been received. **Bit and Interrupt Cleared** - a) by a read of the Status Register followed by a read of the RX Data Buffer or b) by RX Enable going Low.
Bit 1 D_1	RX Checksum True		D_1, when set, indicates that the error checking on the previous 6 bytes agreed with the received checksum. This function, which is valid when the RX Data Ready bit (D0) is set for the second byte of received checksum, does not cause an interrupt. **Set** - by a correct comparison between the received and generated checksums. **Cleared** - a) by a read of the Status Register followed by a read of the RX Data Buffer, or b) by RX Enable going Low.
Bit 2 D_2	RX Carrier Detect		D_2 is a "real time" indication from the modem receiver's carrier detect dircuit and does not cause an interrupt. When MSK tones are present at the receiver input, this bit goes High. With no MSK input, it goes Low. When the RX Enable bit (D_2 - Control Register) is Low, RX Carrier Detect will go Low.
Bit 3 D_3	TX Data Ready		D_3, when set, causes an interrupt to indicate that a byte of data should be written to the TX Data Buffer within 8 bit periods. **Set** - a) when the contents of the TX Data Buffer are transferred to the TX Data Register, or b) when theTX Enable is set--No interrupt is generated in this case. **Bit Cleared** - a) by a read of the Status Register followed by a write to the TX Data Buffer, or b) by TX Enable going Low. **Interrupt Cleared** - a) by a read of the Status Register, or b) by TX Enable going Low.
Bit 4 D_4	TX Idle		D_4 causes an interrupt when set to indicate that all loaded data and one "hang" bit have been transmitted. **Set** - one bit period after the last byte is transmitted. This last byte could be either "checksum" or "loaded data" depending on the TX Parity Enable state (Control Register D_1). **Bit Cleared** - a) by a write to the TX Data Buffer, or b) by TX Enable going Low. **Interrupt Cleared** - a) by a read of the Status Register, or b) by TX Enable going Low.
Bit 5 D_5	Timer Interrupt		D_5, when set, causes an interrupt to indicate that the set timer period has expired. (Control Register D_4 - D_7). **Set** - by the timer. **Bit and Interrupt Cleared** - by a read of the Status Register.
Bit 6 D_6	RX SYNC Detect *		D_6, when set, causes an interrupt to indicate that a 16-bit SYNC word (see Figure 2) has been detected in the received bit stream. **Set** - on receipt of the 16th bit of a SYNC word. **Bit Interrupt and Cleared** - a) by a read of the Status Register, or b) by RX Enable going Low.
Bit 7 D_7	RX SYNT Detect *		D_7, when set, causes an interrupt to indicate that a 16-bit SYNT word (see Figure 2) has been detected in the received bit stream. **Set** - on receipt of the 16th bit of a SYNT word. **Bit and Interrupt Cleared** - a) by a read of the Status Register, or b) by RX Enable going Low.
*Note			SYNC and SYNT Detection is disabled while the checksum checker is running.

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RX Data Buffer $A_1 = 1$ $A_0 = 0$ $A_2 = 1$ **Read Only**

These 8 bits are the last byte of data received. Bit 7 is received first. *Note the relative positions of the MSB and LSB presented in this stream: the position may be different from the convention used in other microprocessor peripherals.*

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

TX Data Buffer $A_1 = 1$ $A_0 = 0$ $A_2 = 0$ **Write Only**

These 8 bits loaded into the TX Data Buffer are the next byte of data that will be transmitted (bit 7 first). *Note the relative positions of the MSB and LSB presented in this stream: the position may be different from the convention used in other microprocessor peripherals.* If the TX Parity Enable bit (Control Register D_1) is set, a 2-byte checksum will be inserted and transmitted by the modem after every 6 transmitted "message" bytes.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
LSB	-	-	-	-	-	-	MSB

The Syndrome Word

This 16-bit word (both Low and High bytes) may be used to correct errors.

Bits S_1 to S_{15} are the 15 bits remaining in the polynomial divider of the checksum checker at the end of 6 bytes of "received message." For a correct message all 15 bits (S_1 to S_{15}) will be zero.

The 2 Syndrome bytes are valid when the RX Data Ready bit (Status Regiser D_0) is set for the second byte of the received checksum and should be read, if required, before 8 byte periods.

Syndrome Low Byte $A_1 = 0$ $A_0 = 0$ $A_2 = 1$ **Read Only**

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S1	S2	S3	S4	S5	S6	S7	S8

Syndrome High Byte $A_1 = 0$ $A_0 = 1$ $A_2 = 1$ **Read Only**

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
S9	S10	S11	S12	S13	S14	S15	Parity Error

D_7 is a "Parity Error Bit" indicating an error between the received parity bit and the parity bit internally generated from the incoming message. So for a correctly received message all 16 bits of the Syndrome Word (S_1 to S_{15} and Parity Error) will be zero.

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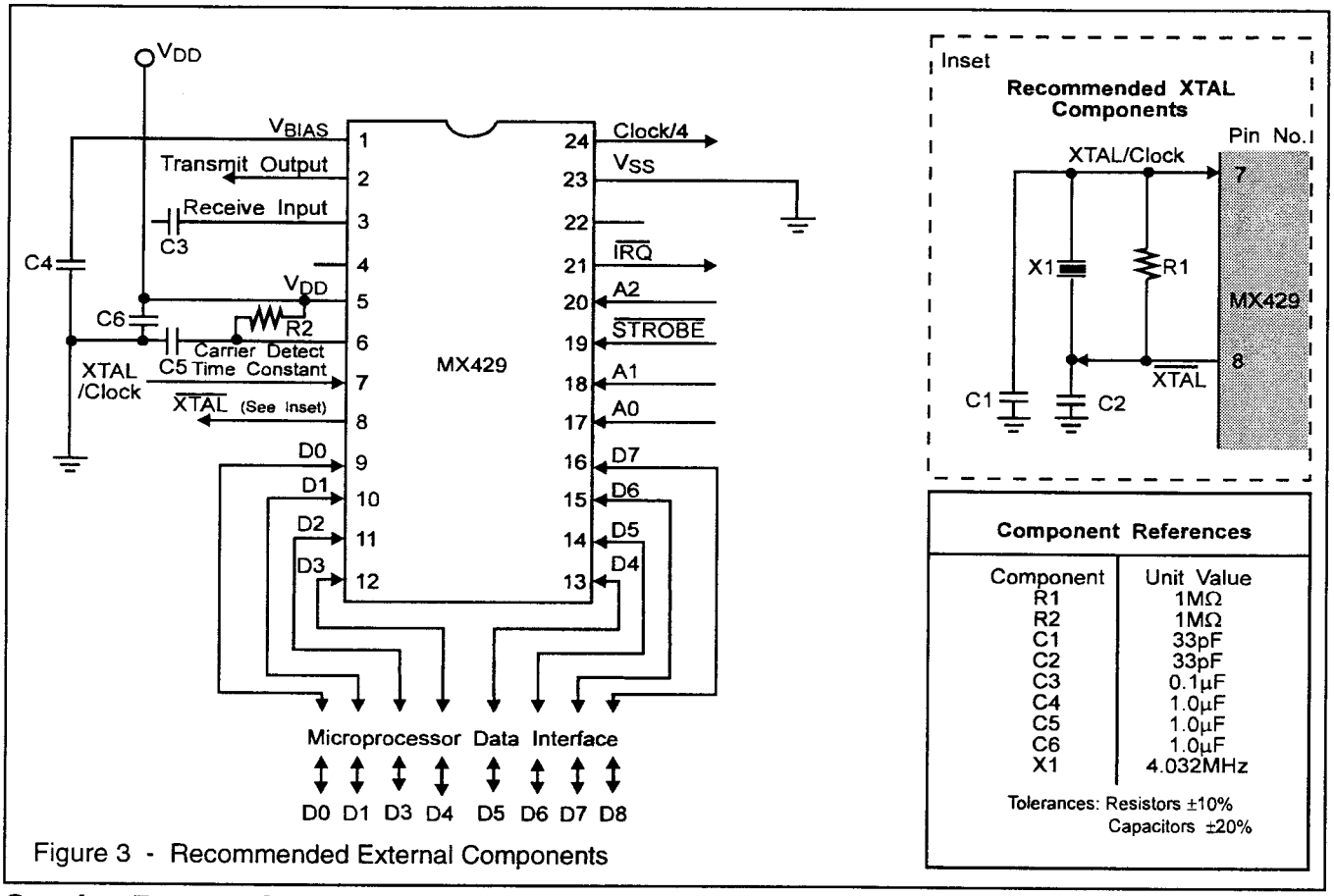

Figure 3 - Recommended External Components

Carrier Detect Capacitor

The value of the Carrier Detect Capacitor, C_5, determines the carrier detect time constant. A long time constant (larger value C_5) results in improved noise immunity but increased response time. C_5 may be varied to optimize noise immunity/response time.

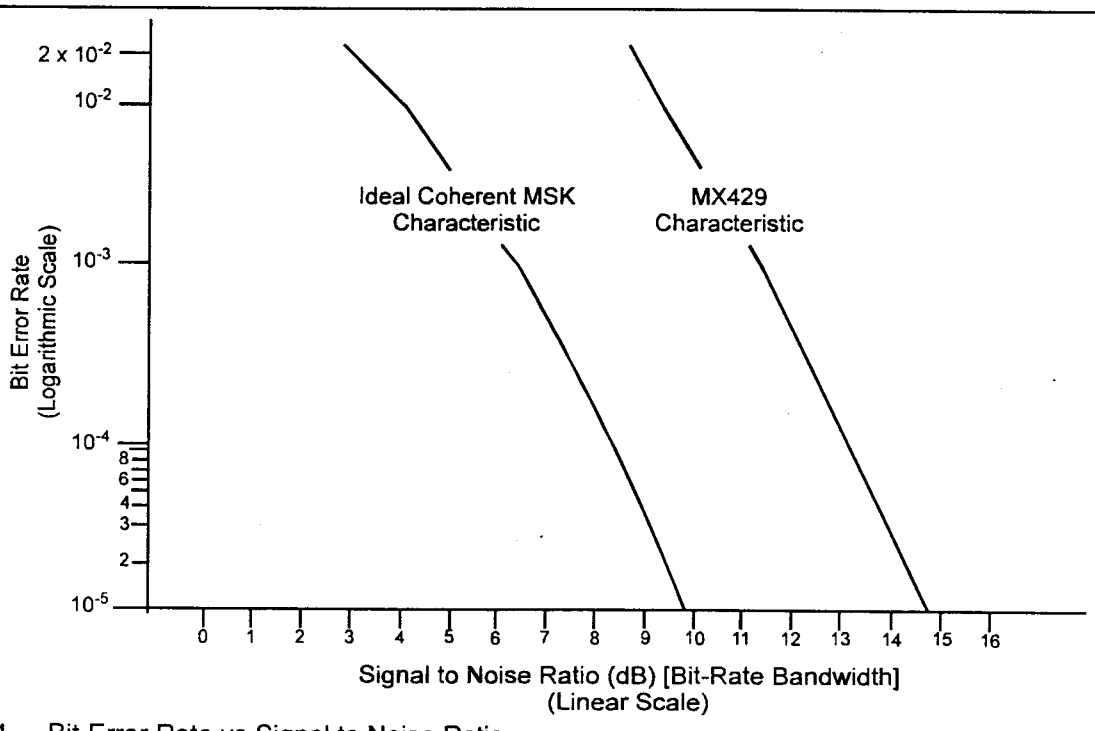

Figure 4 - Bit Error Rate vs Signal to Noise Ratio

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Timing Information

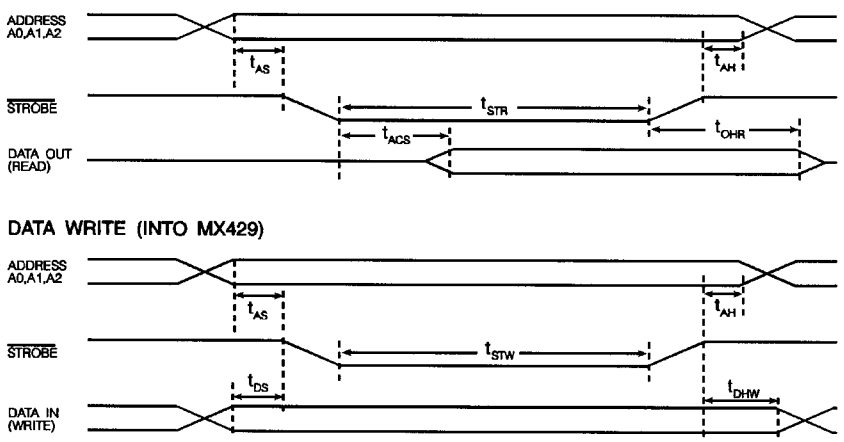

Figure 5 - Read and Write Timing Diagram

RX Operation

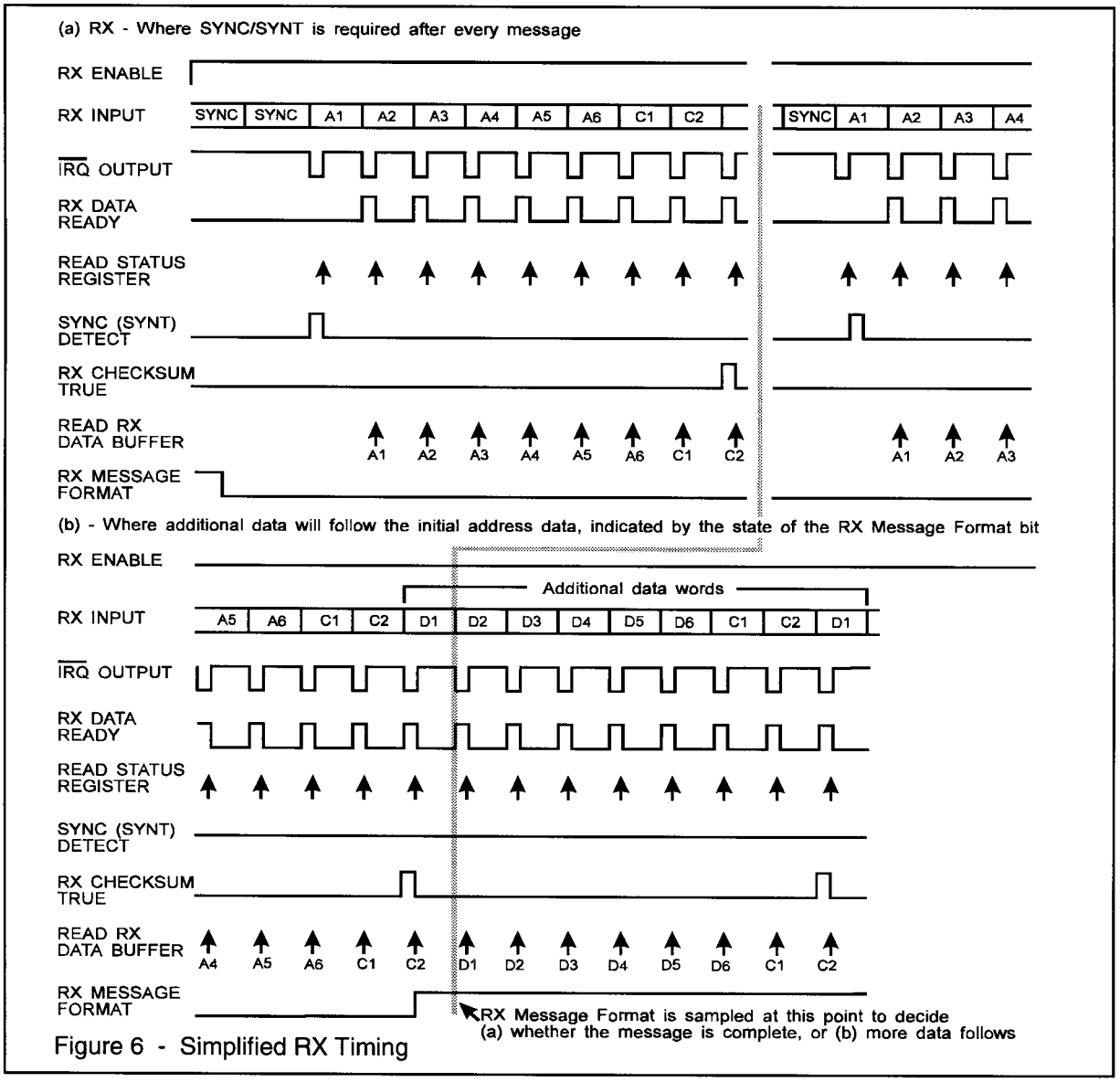

Figure 6 - Simplified RX Timing

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TX Operation

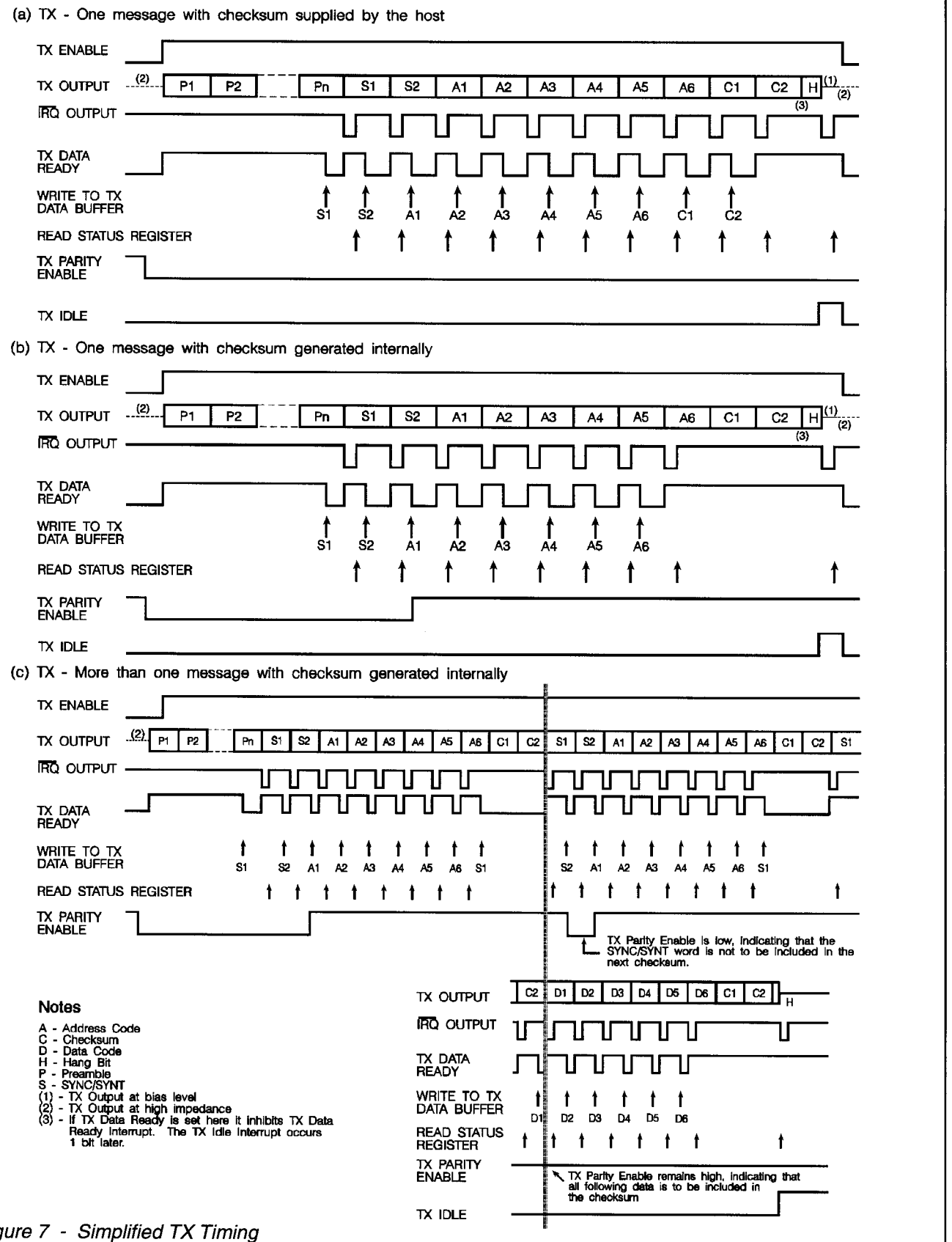

Figure 7 - Simplified TX Timing

Basic Power-up Software

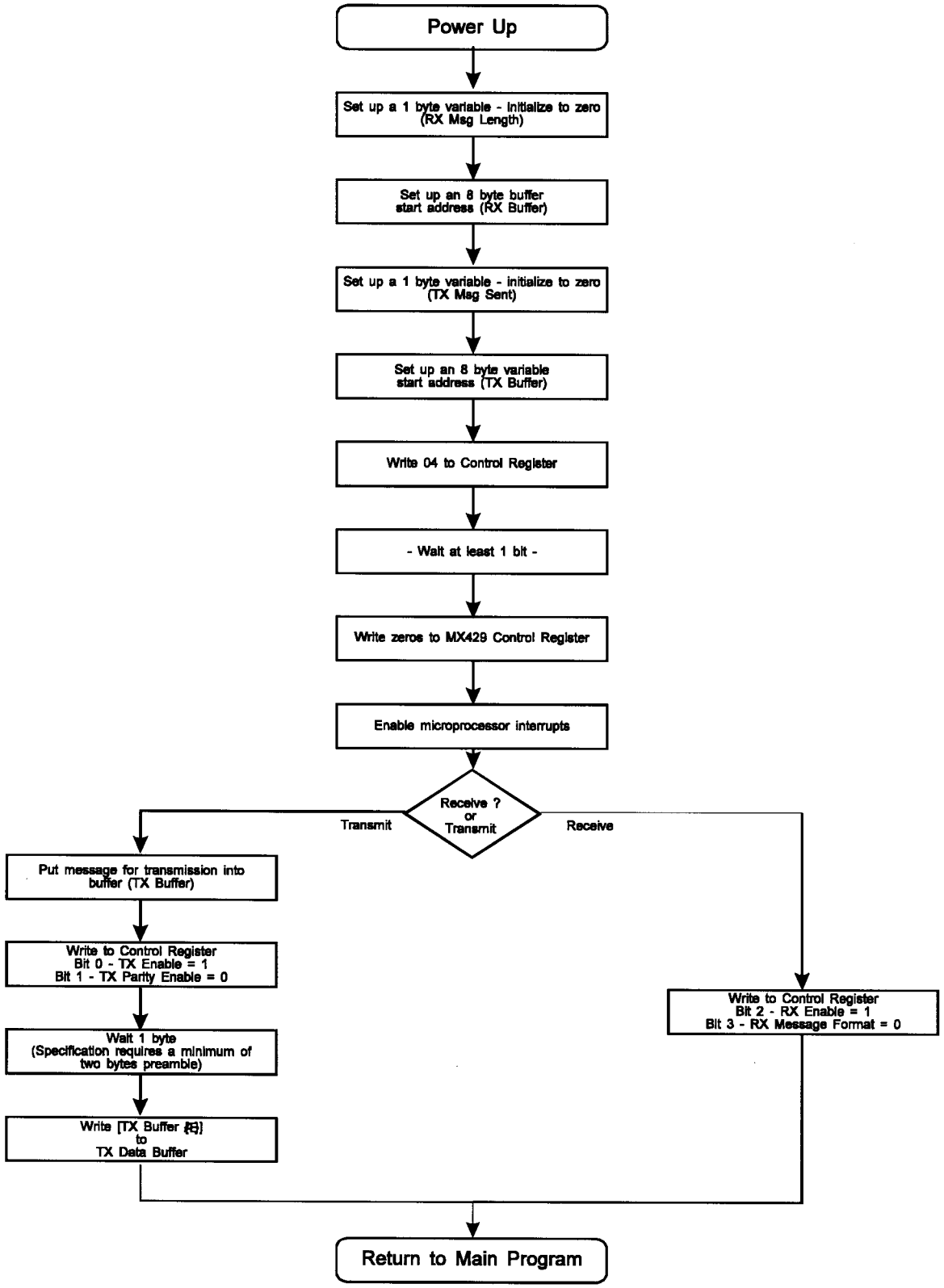

Figure 8 - Power-up Flow

Basic Software Interrupt Flow

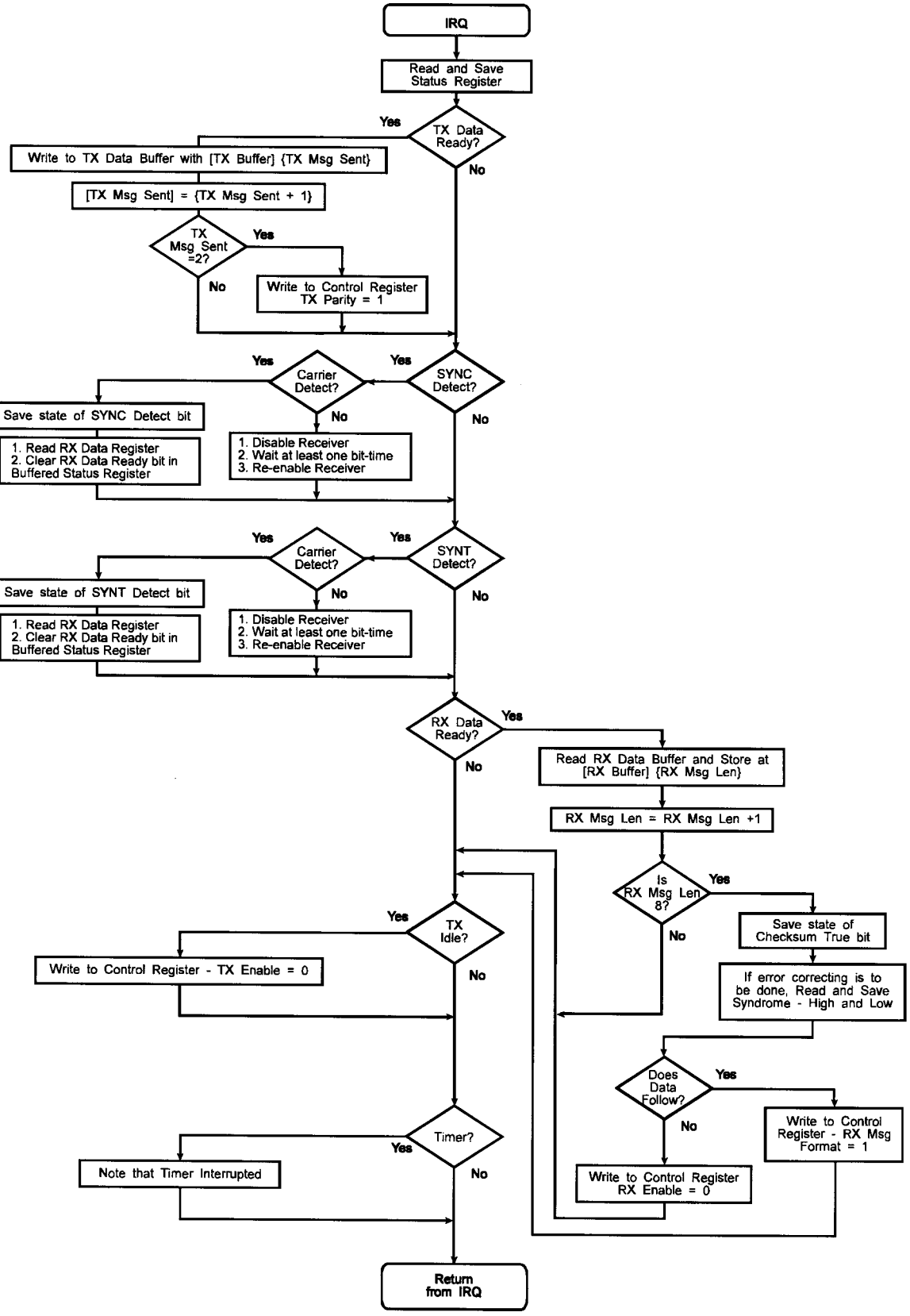

Figure 9 - Interrupt Flow

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exceeding the maximum rating can result in device damage. Operation of the device outside the operating limits is not suggested.

Supply Voltage ..... -0.3 to 7.0 V
Input Voltage at any pin
(ref V_{SS} = 0V) ..... -0.3 V to V_{DD} + 0.3 V
Sink/Source Current
(supply pins) ..... ±30mA
(other pins) ..... ±20mA
Total Device Dissipation
(@T_{AMB}25C) ..... 800mW max.
Derating ..... 10mW/°C
Operating Temperature ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C

OPERATING LIMITS

All devices were measured under the following conditions unless otherwise noted.
V_{DD}=5.0V

T_{AMB}=25°C

Xtal/Clock fo = 4.032 MHz For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer. Operation of this device without a Xtal or Clock input may cause device damage.

Audio Level 0dB ref. = 300 mVrms

Characteristics	See Note	Min.	Typ.	Max.	Unit
Static Values					
Supply Voltage		4.5	-	5.5	V
Supply Current Ranges					
RX & TX Enabled		-	5.0		mA
RX Enabled, TX Disabled		-	5.0	-	mA
RX Disabled, TX Enabled		-	5.0	-	mA
RX & TX Disabled	10	-	1	-	mA
Dynamic Values					
Modem Internal Delay		-	1.5	-	ms
Interface Levels					
Output Logic "1" Source Current	2	-	-	120	µA
Output Logic "0" Sink Current	3	-	-	360	µA
Three State Output Leakage Current		-	-	4.0	µA
D_0 - D_7 Data In/Out	1				
Logic "1" Level		3.5	-	-	V
Logic "0" Level		-	-	1.5	V
A_1, A_0, A_2, STROBE, IRQ	4				
Logic "1" Level		4.0	-	-	V
Logic "0" Level		-	-	1.0	V
Analog Impedances					
RX Input		100	-	-	kΩ
TX Output (Enabled)	11	-	10	-	kΩ
TX Output (Disabled)	11	-	5	-	MΩ
On-Chip Xtal Oscillator					
R_{IN}		10	-	-	MΩ
R_{OUT}	5	5.0	-	15	kΩ
Oscillator Gain		-	15	-	dB
Xtal Frequency		-	4.032		MHz
Timing (See Fig. 5)					
Chip Select Access Time (t_{ACS})		-	-	135	ns
Address Hold Time (t_{AH})		0	-	-	ns
Address Set-up Time (t_{AS})		0	-	-	ns
Data Hold Time (Write) - (t_{DHW})		85	-	-	ns
Data Set-up Time - (t_{DS})		0	-	-	ns
Output Hold Time (Read) - (t_{OHR})		15	-	105	ns
Strobe Time (Read) - (t_{STR})		140	-	-	ns
Strobe Time (Write) - (t_{STW})		50	-	-	ns

Characteristics (continued)	See Note	Min.	Typ.	Max.	Unit
Receiver					
Signal Input Levels	6	-9.0	-2.0	+10.5	dB
Bit Error Rate	7				
@ 12 dB Signal/Noise Ratio		-	7.0	-	10^{-4}
@ 20 dB Signal/Noise Ratio		-	1.0	-	10^{-8}
Synchronization @ 12 dB S/N Ratio	8				
Probability of Bit 16 being correct		-	99.5	-	%
Carrier Detect Response Time	8	-	13.0	-	ms
Transmitter					
Output Level		-	8.25	-	dB
Output Level Variation		-1.0	-	+1.0	dB
Output Distortion		-	3.0	5.0	%
3rd Harmonic Distortion		-	2.0	3.0	%
Logic "1" Frequency	9	-	1200	-	Hz
Logic "0" Frequency	9	-	1800	-	Hz
Isochronous Distortion					
1200-1800 Hz		-	25	40	µs
1800-1200 Hz		-	20	40	µs

Notes

1. With each data line loaded as C = 50 pf and R = 10 kΩ.
2. V_{OUT} = 4.6 V.
3. V_{OUT} = 0.4 V.
4. Sink/Source currents ≤ 0.1 mA.
5. Both Xtal and Xtal ÷ 4 Outputs.
6. With 50 dB S/N ratio.
7. See Figure 3, Bit Error Rate.
8. This response time is measured using a 10101010101...01 pattern input signal at a level of 230 mVrms (-2.3 dB) with no noise.
9. Dependent upon Xtal tolerance.
10. Powersave is only active when both RX and TX functions are disabled.
11. Recommended sequence of commands for the MX429 which ensures the Tx output is set high impedance.

Control RegisterCommand	Function
01_H	Tx enable
04_H	Rx enable & Tx enable

CAUTION: Using the following sequence of commands may cause the Tx output to go low impedance.

Control RegisterCommand	Function
01_H	Tx enable
00_H	Clear control register, i.e. disable
04_H	Rx enable

Checksum Generation and Checking

Generation - The checksum generator takes the 48 bits from the 6 bytes loaded into the TX Data Buffer and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

It then takes the 15-bit remainder from the polynomial divider, inverts the last bit and appends an EVEN parity bit generated from the initial 48 bits and the 15 bit remainder (with the last bit inverted).
The 16-bit word is used as the "checksum."

Checking - The checksum generator does two things:
It takes the first 63 bits of a received message, inverts bit 63, and divides them modulo-2, by the generating polynomial:

$$X^{15} + X^{14} + X^{13} + X^{11} + X^4 + X^2 + 1$$

The 15 bits remaining in the polynomial divider are checked for all zero.
Second, it generates an EVEN parity bit from the first 63 bits of a received message and compares this bit with the received parity bit (bit 64). If the 15 bits in the polynomial divider are all zero, and the two parity bits are equal, then the RX Checksum True bit (SR D_1) is set.

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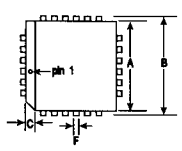
Package Information

The MX429 is available in either 24-lead Plastic Leaded Chip Carrier [PLCC] (figure 11), Ceramic Dual In-Line [CDIP] (figure 12) or a Plastic Dual In-Line [PDIP] (figure 13) package. For identification purposes there is an ident spot adjacent to pin 1 on the CDIP/PDIP diagram. On the PLCC, there is a chamfered corner between pins 3 & 4.

24 LEAD PLASTIC LEADED CHIP CARRIER "LH"

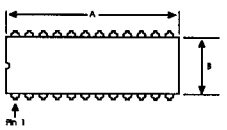


Package Tolerances

Dimension in., (mm)	Min.	Max.
A	0.382 (9.7)	0.410 (10.40)
B	0.417 (10.60)	0.435 (11.05)
C	0.045 (1.15)x45°	typical
D	0.050 (1.27)	typical
E	0.366 (9.30)	typical
F	0.018 (0.45)	0.022 (0.55)
H	0.250 (6.35)	typical
J	0.128 (3.25)	0.146 (3.70)
K	0.007 (0.17)	0.011 (0.27)

Figure 11 - MX429LH

24 PIN PLASTIC DUAL IN-LINE "P"

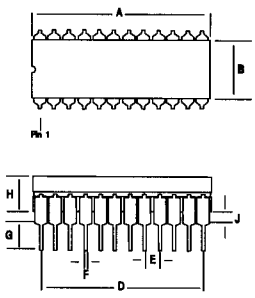


Package Tolerances

Dimension [in. (mm)]	Min.	Max.
A	1.23 (31.24)	1.26 (32.004)
B	0.53 (13.46)	0.55 (13.97)
C	0.59 (14.98)	0.610 (15.49)
D	0.63 (16.002)	0.67 (17.018)
E	0.170 (4.318)	0.220 (5.588)
F	0.125 (3.175)	0.160 (4.064)
G	0.015 (.381)	0.020 (.508)
H	0.040 (1.016)	0.065 (1.651)
J	0.090 (2.286)	0.110 (2.794)
K	0.015 (0.381)	0.065 (.165)

Figure 12 - MX429P

24 PIN CERAMIC DUAL IN-LINE "J"



Package Tolerances

Dimension in., (mm)	Min.	Max.
A	1.24 (31.50)	1.26 (32.03)
B	0.514 (13.06)	0.583 (14.81)
C	0.60 (15.14)	0.615 (15.61)
D	1.10 (27.84)	1.11 (28.04)
E	0.100 (2.54)	typical
F	0.018 (0.46)	typical
G	0.171 (4.35)	typical
H	0.171 (4.35)	0.196 (4.99)
J	0.020 (0.50)	------

Figure 13 - MX429J

Handling Precautions

The MX429 is a CMOS LSI circuit which includes input protection. However, precautions should be taken to prevent static discharges which may cause damage.

CAUTION
MOS Device. May be damaged by static discharge. Observe handling precautions.

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CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

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