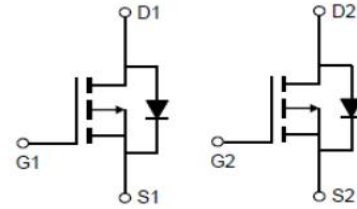




Dual P-Channel Enhancement Mode Power MOSFET

Description

The MX4805 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as -4.5V. This device is suitable for use as a load switch or in PWM applications.



Schematic diagram

General Features

$V_{DS} = -30V, I_D = -9A$

$R_{DS(ON)}$ (Typ.) $12m\Omega$ @ $V_{GS} = -20V$

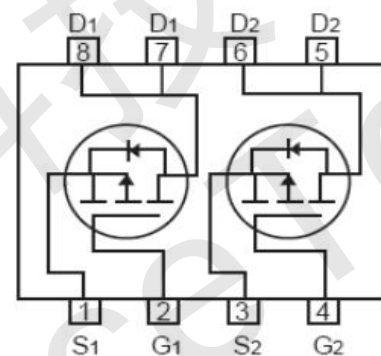
$R_{DS(ON)}$ (Typ.) $13m\Omega$ @ $V_{GS} = -10V$

$R_{DS(ON)}$ (Typ.) $20m\Omega$ @ $V_{GS} = -4.5V$

High Power and current handing capability

Lead free product is acquired

Surface mount package

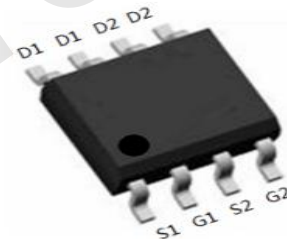


Application

PWM applications

Load switch

Power management



SOP-8 top view

Absolute Maximum Ratings ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Drain Current-Continuous	I_D	-9	A
Drain Current-Pulsed (Note 1)	I_{DM}	-27	A
Maximum Power Dissipation	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ C$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	41.67	$^\circ C/W$
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Electrical Characteristics ($T_A=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V I _D =-250μA	-30	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-30V, V _{GS} =0V	-	-	-1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} =±25V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250μA	-1.5	-2.2	-3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-20V, I _D =-9A	-	12	15	mΩ
		V _{GS} =-10V, I _D =-8A	-	13	18	mΩ
		V _{GS} =-4.5V, I _D =-5A	-	20	35	mΩ
Forward Transconductance	g _{FS}	V _{DS} =-10V, I _D =-10A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{iss}	V _{DS} =-15V, V _{GS} =0V, F=1.0MHz	-	2010	-	PF
Output Capacitance	C _{oss}		-	346	-	PF
Reverse Transfer Capacitance	C _{rss}		-	297	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =-15V, I _D =-9A, V _{GS} =-10V, R _{GEN} =1Ω	-	11	-	nS
Turn-on Rise Time	t _r		-	6	-	nS
Turn-Off Delay Time	t _{d(off)}		-	28	-	nS
Turn-Off Fall Time	t _f		-	10	-	nS
Total Gate Charge	Q _g	V _{DS} =-15V, I _D =-9A, V _{GS} =-10V	-	26	-	nC
Gate-Source Charge	Q _{gs}		-	3.9	-	nC
Gate-Drain Charge	Q _{gd}		-	9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =-1A	-	-	-1	V

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production



Typical Electrical and Thermal Characteristics

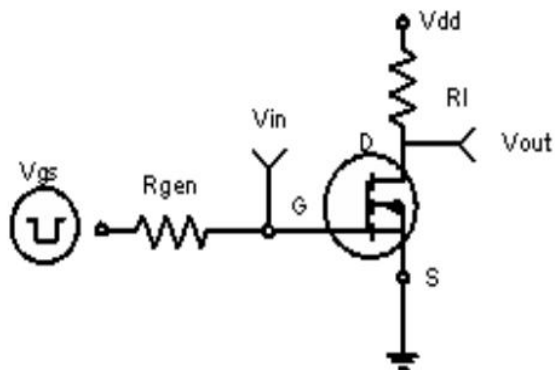


Figure 1: Switching Test Circuit

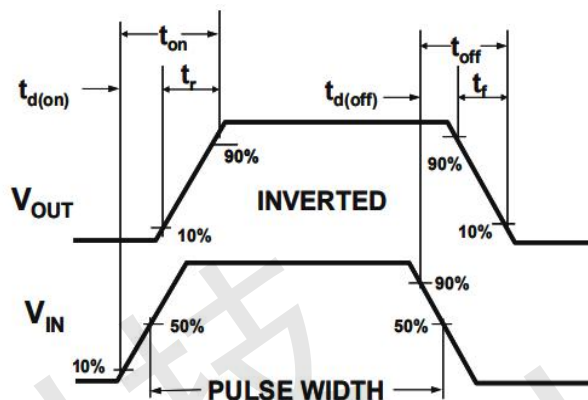


Figure 2: Switching Waveforms

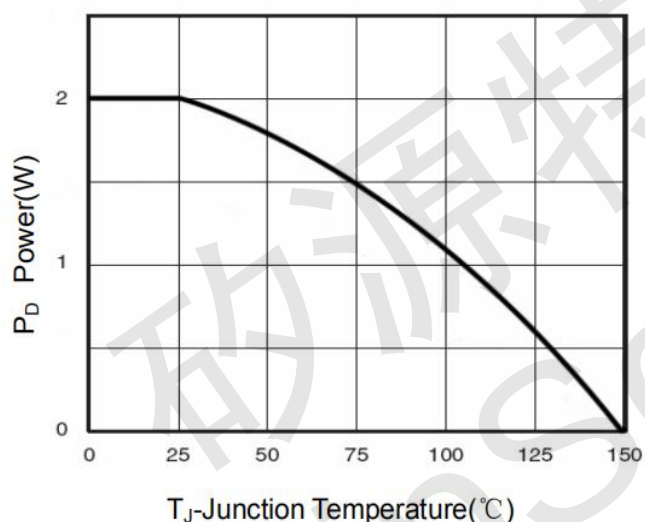


Figure 3 Power Dissipation

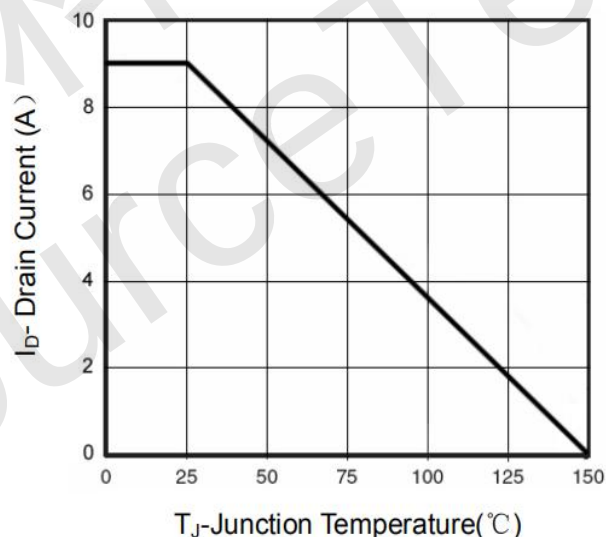


Figure 4 Drain Current

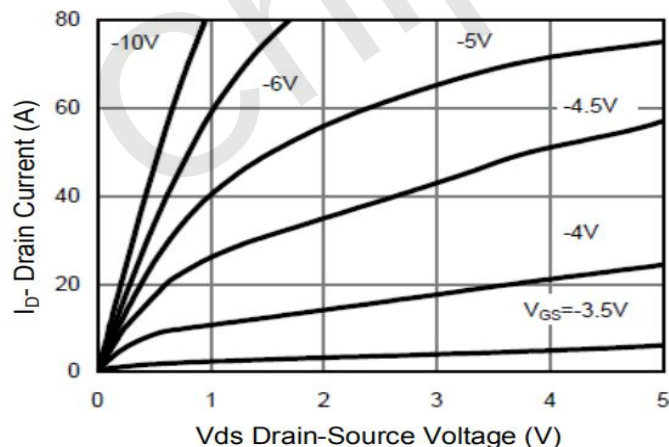


Figure 5 Output Characteristics

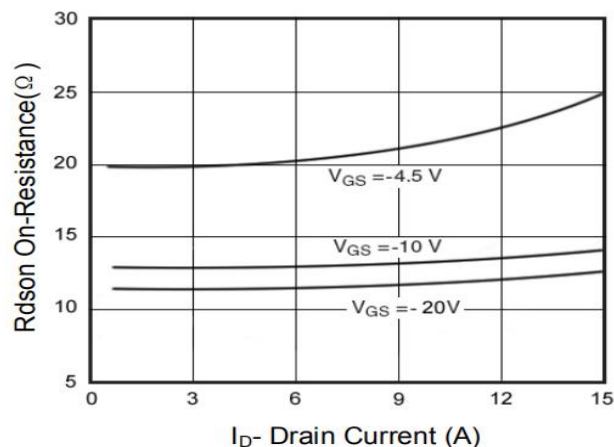


Figure 6 Drain-Source On-Resistance

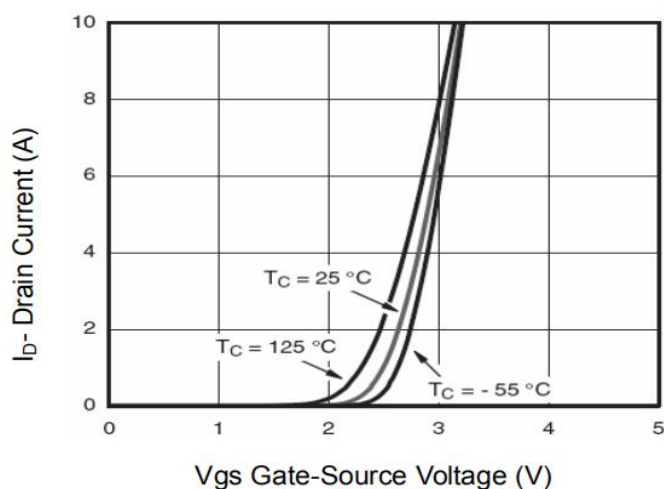


Figure 7 Transfer Characteristics

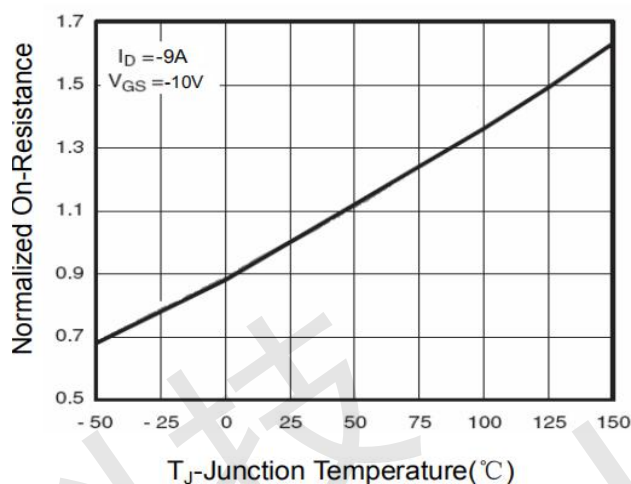


Figure 8 Drain-Source On-Resistance

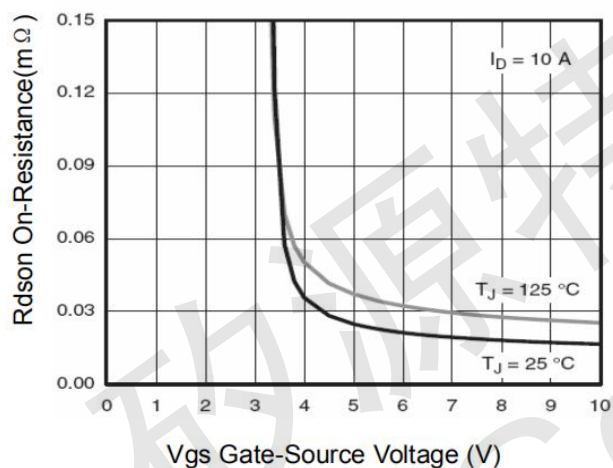


Figure 9 $R_{DS(on)}$ vs V_{GS}

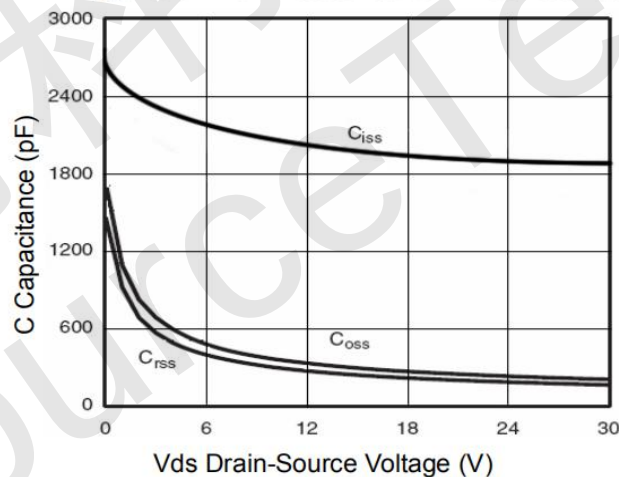


Figure 10 Capacitance vs V_{DS}

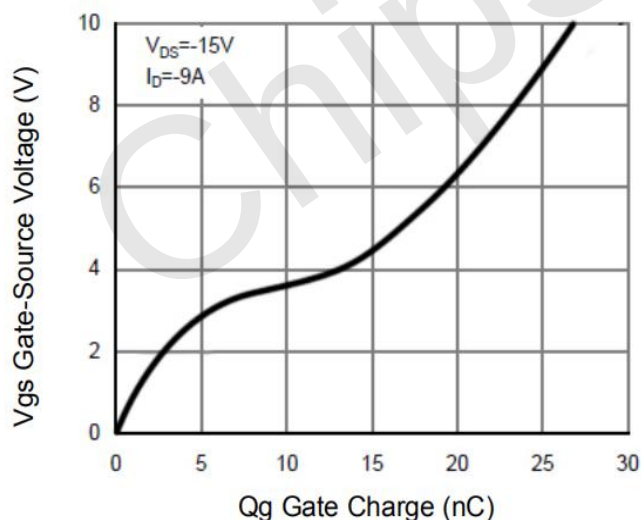


Figure 11 Gate Charge

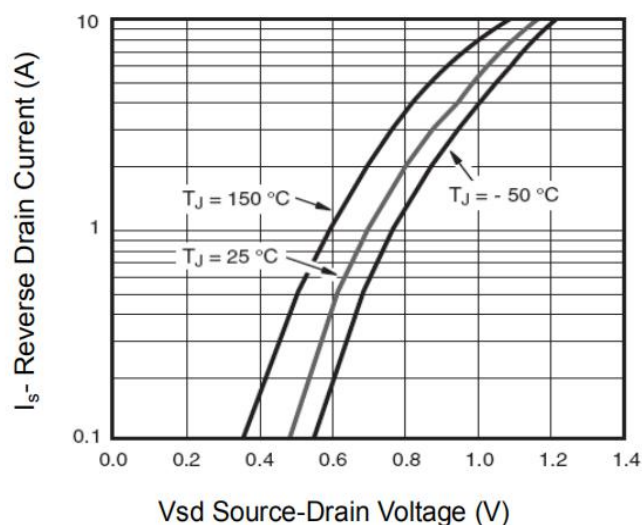


Figure 12 Source- Drain Diode Forward

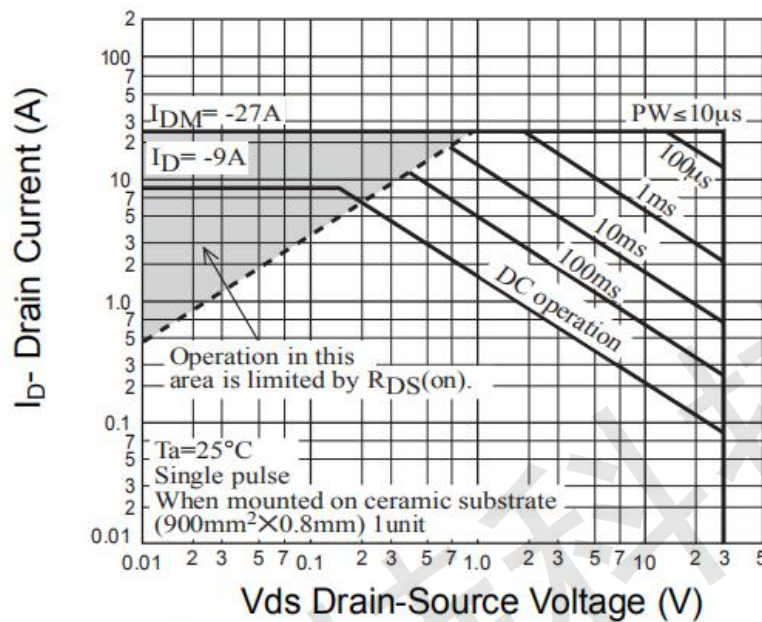


Figure 13 Safe Operation Area

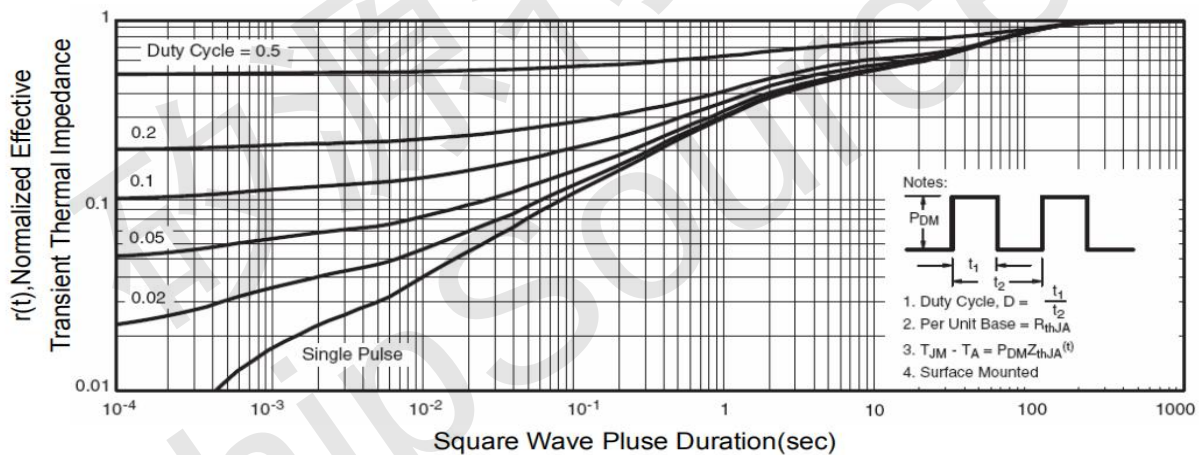
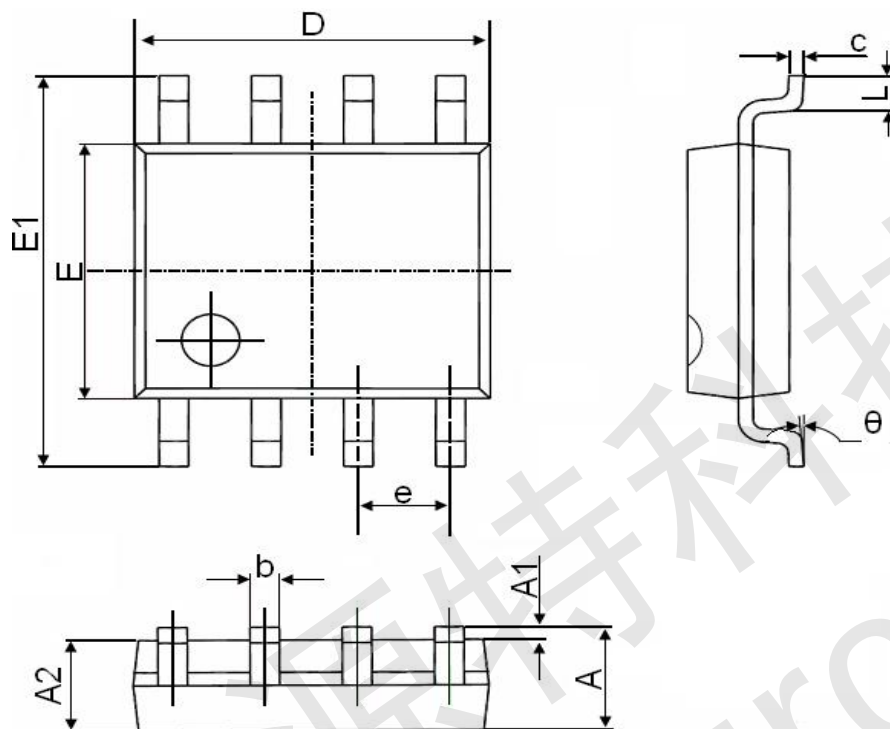


Figure 14 Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°