GENERAL DESCRIPTION

MX5012D is a cost effective, resettable fuse which can greatly enhance the reliability of a board drive or other circuit from both catastrophic and shutdown failures. The device is designed to protect systems such as USB hubs against sudden output short to battery events. The device monitors VIN and VOUT to provide true reverse blocking from output when output short to battery fault condition or input power fail condition is detected.

It is designed to buffer the load device from excessive input voltage which can damage sensitive circuits. It includes an overvoltage clamp circuit that limits the output voltage during transients but does not shut the unit down, thereby allowing the load circuit to continue its operation.

FEATURES

♦44mR Typical RDSON with 2 FET

♦Tristate Enable

♦Over current Protection

♦Thermally Protection

♦Integrated Soft Start Circuit

♦Fast Response Overvoltage Clamp Circuit

♦Internal Undervoltage Lockout Circuit

♦Internal Charge Pump

♦Hot Pluggable

♦MX5012D in WDFN10 4*4 Package

♦These devices are Pb-Free, Halogen Free and ROHS Compliant

APPLICATIONS

Solid State Drives

White Goods Applications

Smart Load Switches/USB Switches

Adapter Power Devices

Servers

Hard Drives

Mother Board

Fan Drives

Solar Rapid Shutdown

Hot Plug Devices

GENERAL INFORMATION

Ordering information

Part Number	Description
MX5012D	WDFN10 4*4，Halogen-free，T&R

Package dissipation rating

Package	RθJC（℃/W）
WDFN4*4	50

Absolute maximum ratings

Parameter	Value
VCC DC supply voltage	-0.3 to 18V
EN/Fault pin voltage	-0.3 to 18V
dv/dt and Ilimit pin voltage	-0.3 to 6V
Source pin voltage	-0.3 to 18V
Junction temperature T_J	-40 to 150℃
Storage temperature T_{STG}	-55 to 150℃
Leading temperature （soldering, 10secs）	260℃
ESD Susceptibility HBM	2000V

Over Stress Caution

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. The MAXIN MICRO recommends that all integrated circuits be handled with appropriate precautions. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Recommended operating condition

Symbol	Parameter	Range
VCC	VCC supply voltage	4.5-14.4V
PD_MAX	@TA=25℃ WDFN4*4	2.0W

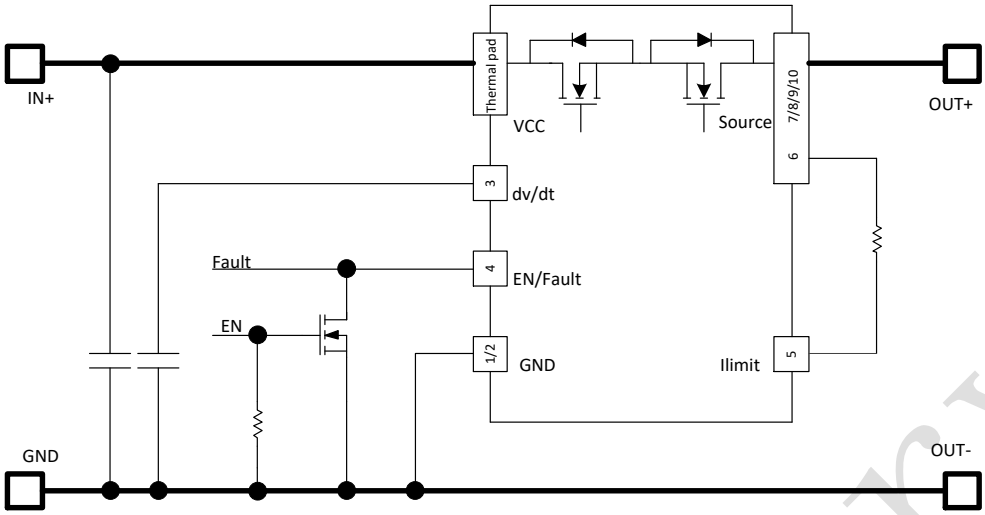


Figure1 MX5012D Application Circuit with Kelvin Current Sensing

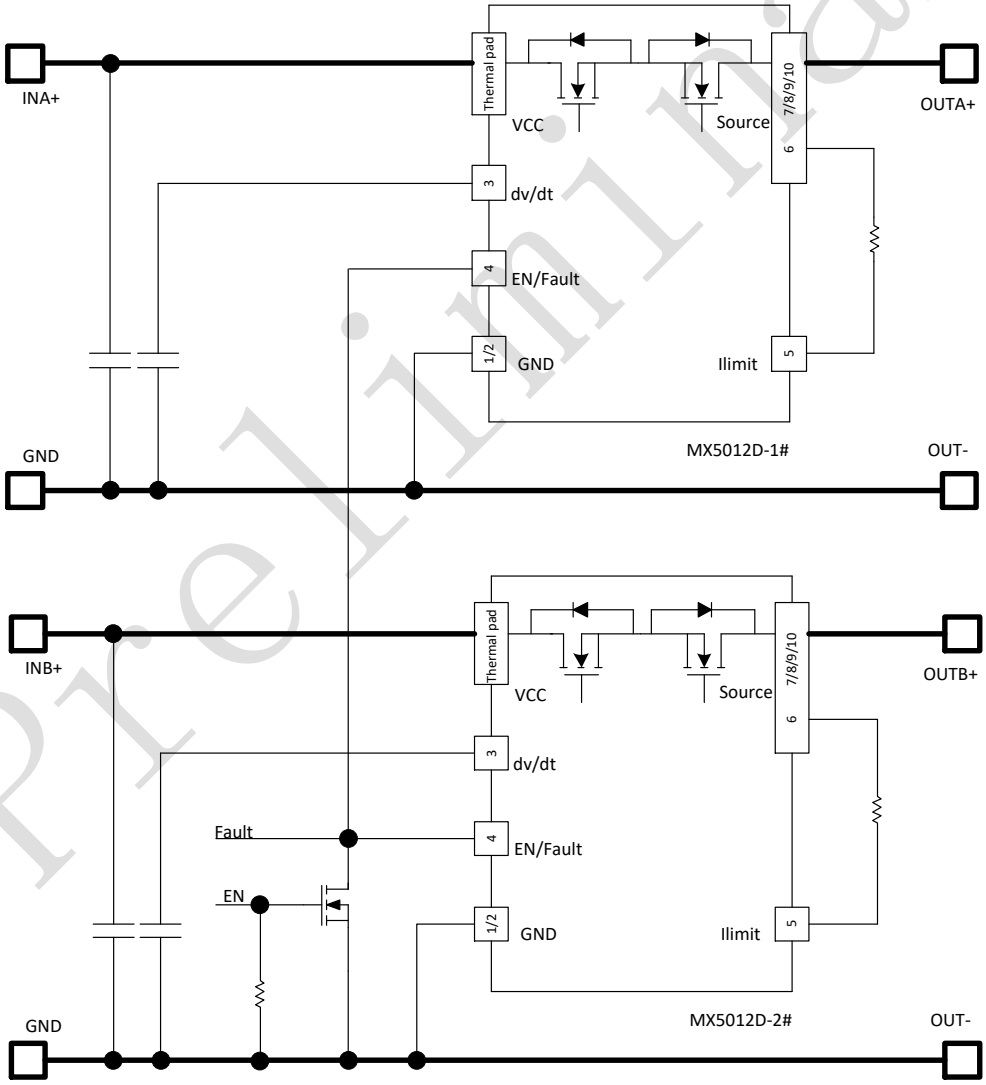


Figure2 Common Thermal Shutdown between Different load

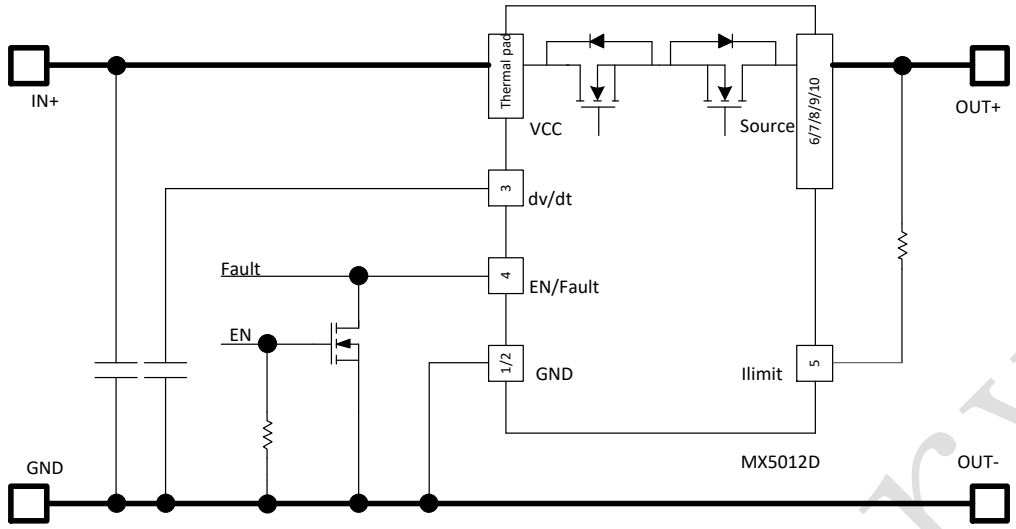


Figure3 MX5012D Application Circuit with Direct Current Sensing

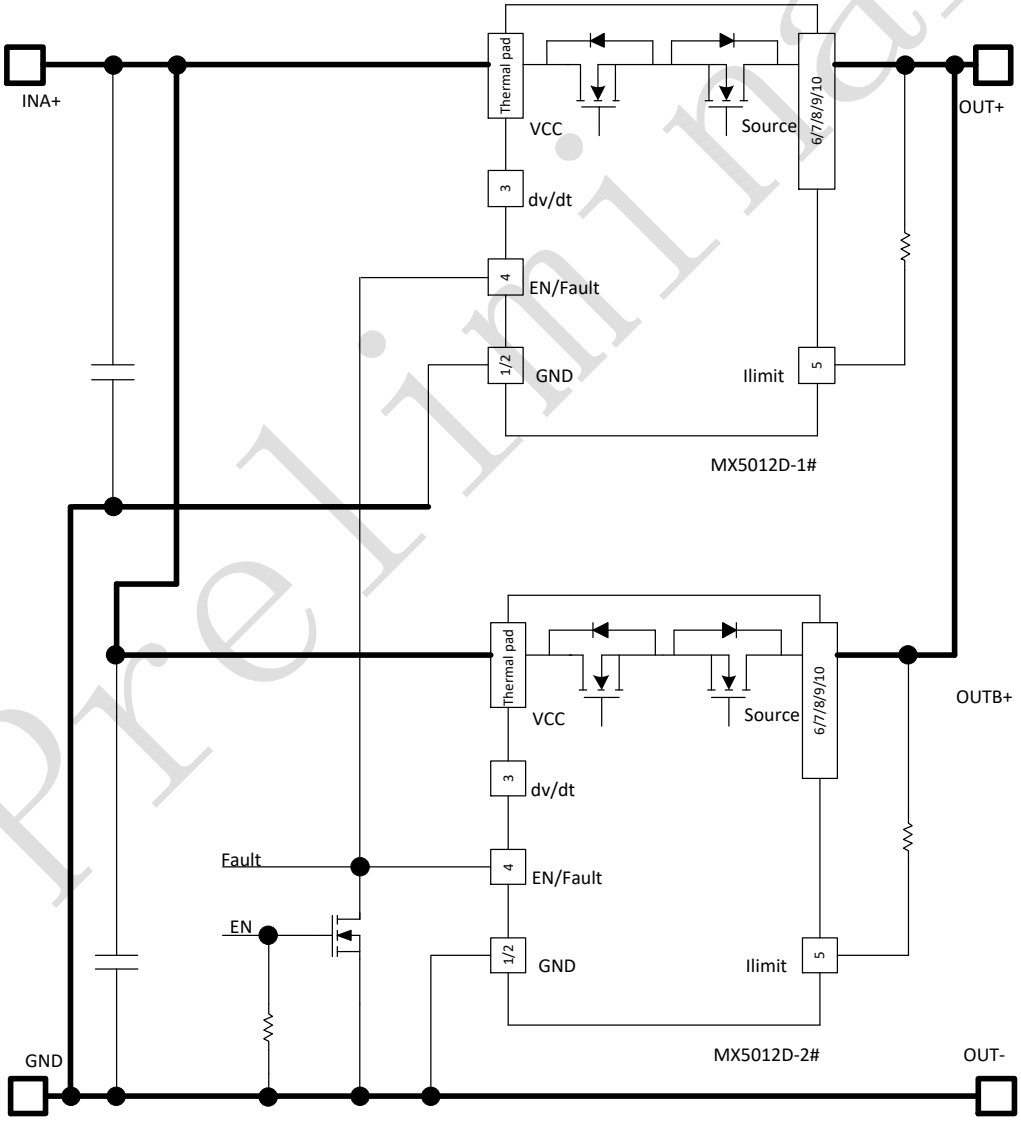


Figure4 Paralleling Application eFuse

TERMINAL ASSIGMENTS

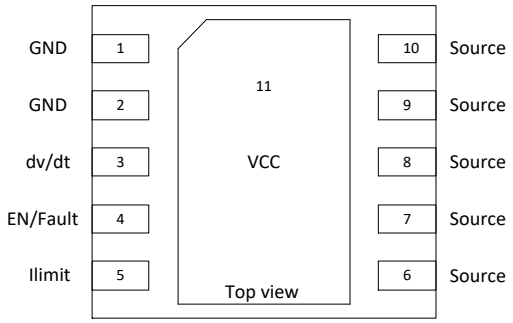


Figure5 pin information

PIN NO.	PIN name	Description
1/2	**GND**	Negative input to the device. This is used as the internal reference for the MX5012D.
3	**dv/dt**	The internal dv/dt circuit controls the slew rate of the output voltage at turn on. It has an internal capacitor that allows it to ramp up over a period of 1ms. An external capacitor can be added to this pin to increase the ramp time. If an additional time delay is not required, this pin should be left open.
4	**EN/Fault**	The enable/fault pin is a tri-state, bidirectional interface. It can be pulled to ground with an external open drain or open collector device to shut down the MX5012D. It can also be used as a status indicator, if the voltage level is intermediate (around 1.4V)， the MX5012D is in thermal shutdown. If the voltage level is high (around 3.0V) the MX5012D is operating normally. Do not actively drive this pin to any voltage. Do not connect a capacitor to this pin.
5	**Ilimit**	A resistor between this pin and the source pin set the over load and short circuit limit levels.
6-10	**Source**	Source of the internal power FET and the output terminal of the MX5012D.
11	**VCC**	Positive input voltage to the device. Connect a 1.0uF or greater capacitor from VCC to GND as close as possible to the MX5012D.

BLOCK DISGRAM

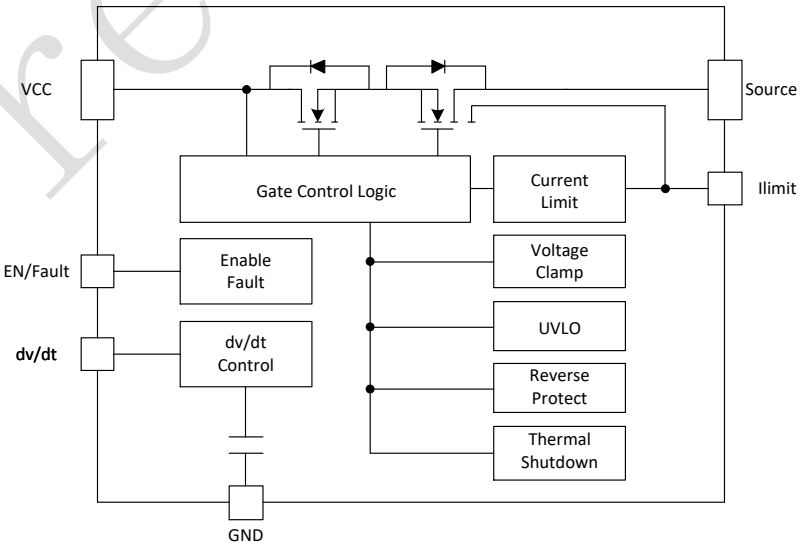


Figure6 block diagram

Electrical characteristics

（TA=25℃， VCC=12V， C_L=20uF, dv/dt pin open, R_{LIM}=75Ω, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
UVLO/OVER VOLTAGE PROTECTION						
VO_CLAMP	VOUT Maximum voltage	VCC=18V	13	14	15	V
UVLO_ON	Undervoltage Lockout	VCC Step down	7.8	8.5	9.2	V
UVLO_OFF	Undervoltage Lockout off	VCC Step up		9.3		V
UVLO_Hyst	UVLO Hysteresis			0.8	V	
KELVIN CURRENT LIMIT						
I_TRIP	Overload/Trip Current	RLIM=75ohm		3.5		A
I_HOLD	Short Circuit/Holding Current	RLIM=75ohm		2.0		A
SLEW RATE CONTROL						
T_SR	Slew Rate (No Capacitor on dv/dt Pin)		0.7	1.0	1.9	ms
ENABLE/FAULT PIN						
V_LOW	Logic Level Low	Output Disabled	0.35	0.58	0.81	V
V_MID	Logic Level Mid, Thermal Fault	Output Disabled	0.82	1.40	1.95	V
V_HIGH	Logic Level High	Output Enabled	1.96	2.20	2.50	V
V_MAX	High State Maximum Voltage		2.51	3.30	5.00	V
I_LOW	Logic Low Sink Current	ENABLE=0V	-25	-17		uA
I_LEAK	Logic High Leakage Current for External Switch	ENABLE=3.3V			1.0	uA
Fan	Maximum Fanout for Fault Signal (Total number of chips that can be connected to this pin for simultaneous shutdown)				3	Units
TOTAL DEVICE						
I_BIAS	Bias Current			650	800	uA
I_OP	Operation Current	No Load		650	800	uA
I_SD	Shutdown Current	ENABLE=0V		100	150	uA
I_FAULT				110	200	uA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted.

Product performance may not be indicated by the electrical characteristics if operated under different conditions.

1. eFuse is latched off until the EN/Fault pin is pulled low and then released or a power on reset is applied to the device.
2. Does not include fan out of EN/Fault function.
3. Pulse test: Pulse width 300 s, duty cycle 2%.
4. Verified by design.

Characteristic plots

VDD=18V, TA=25℃

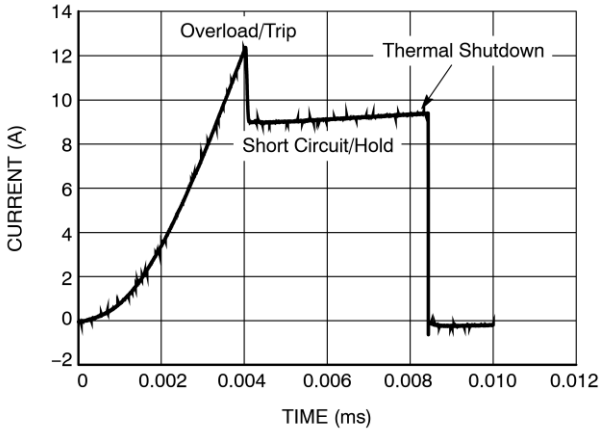


Figure7 Slow fault current limit for MX5012D

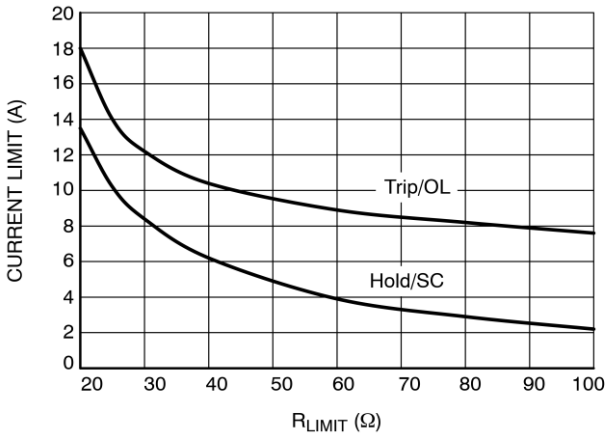


Figure8 Curent limit vs RLMT for kelvin sensing

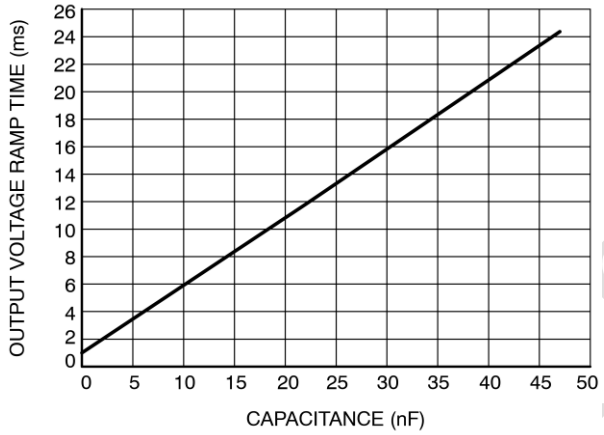


Figure9 Output voltage ramp vs dv/dt capacitance

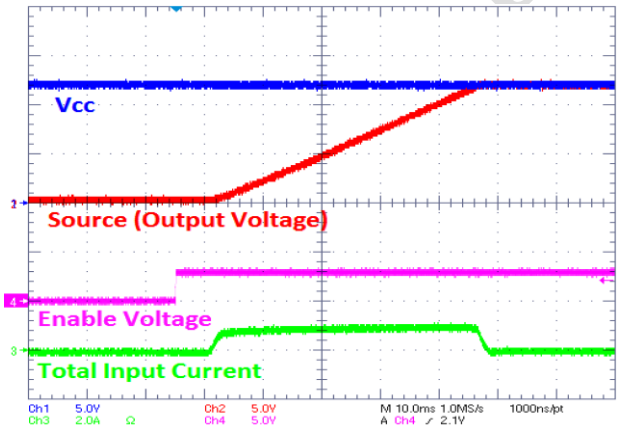


Figure10 MX5012D slew rate control

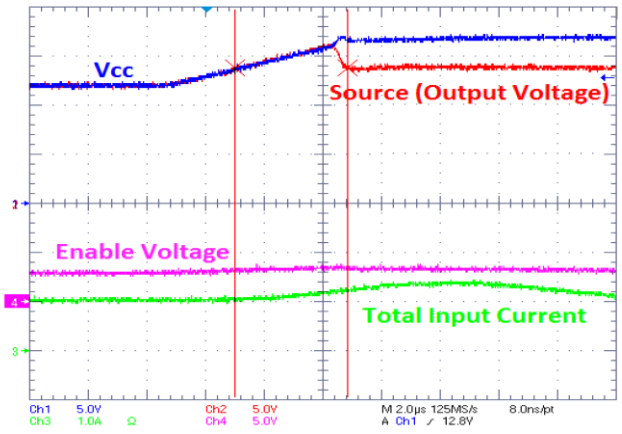


Figure11 MX5012D overvoltage clamp operation

Operation description

Paralleling eFuse

If the output current capability required by an application is higher than the current which can be carried by a single eFuse, it is possible to parallel eFuses to achieve a higher current throughput. Up to four eFuses can be paralleled to achieve a higher current. All of the eFuses will have a common thermal shutdown. Refer to Figure1 for the schematic connection of parallel eFuses. The VCC pins of every eFuse must be shorted together. The source pins of each eFuse must be shorted together. Each eFuse should be configured either in Kelvin or Direct mode and have its individual current limiting resistor RLIM connected between I_{limit} and Source pins. The Enable pins of all eFuses must be shorted together for common shutdown functionality and connected to an open drain or open collector device in case it is desired to turn off all the eFuses at the same time. The dv/dt pins of eFuses must NOT be shorted together; they should be either left floating for a standard output ramp up time or have individual dv/dt capacitor to ground.

Every eFuse will carry equal amount of current during normal operation and overcurrent events. If any of the eFuses goes to thermal shutdown first, it will pull down the Enable pin and make the other eFuses to shut down as well.

Basic operation

This device is a self-protected, resettable, electronic fuse. It contains circuits to monitor the input voltage, output voltage, output current and die temperature.

On application of the input voltage, the device will apply the output voltage to the load based on the restrictions of the controlling circuits. The output voltage, which is controlled by an internal dv/dt circuit, will slew from 0V to the rated output voltage in 1ms （typical）. The device will remain on as long as the temperature does not exceed the 175℃ limit that is programmed into the chip.

The internal current limit circuit does not shut down the part but will reduce the conductivity of the FET to maintain a constant current at the internally set current limit level. The input overvoltage clamp also does not shutdown the part, but will limit the output voltage in the event that the input exceeds the V_CLAMP level.

An internal charge pump provides bias for the gate voltage of the internal N-channel power MOSFET and also for the current limit circuit. The remainder of the control circuitry operates between the input voltage and ground.

Current Limit

The current limit circuit uses a SENSEFET along with a reference and amplifier to control the peak current in the device. The SENSEFET allows for a small fraction of the load current to be measured, which has the advantage of reducing the losses in the sense resistor.

The current limit circuit has two limiting values, one for short circuit events which are defined as the mode of operation in which the gate is high and the FET is fully enhanced. The overload mode of operation occurs when the device is actively limiting the current and the gate is at an intermediate level.

MAXIN micro's Electronic Fuses uses a power MOSFET known as a SENSEFET to control current in the load. All power MOSFETs are made up of thousands of parallel FETs or cells. In a SENSEFET a small percent of the FET cells have their sources separated from the sources of the remaining FET cells. The ratio of cells in the main and small section of the SENSEFET is about 1200. All of the FET cells share common gate and drain connections. The use of a SENSEFET in an eFuse is illustrated conceptually in Figure12, where QM is the main section of the SENSEFET, and QS is the small, or sense, section of the SENSEFET.

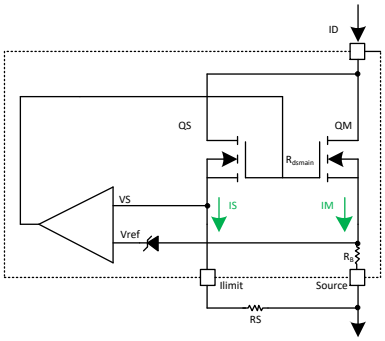


Figure12 SENSEFET and current limit circuit

Since only a small fraction of the main current flows in the sense FET, the current sensing resistor can be a more reasonable value in terms of resistance and power dissipation. This results in a significant cost saving for the current sense resistor.

$$I_m = \frac{k \cdot V_{ref}}{R_s + k \cdot R_B} + \frac{R_S \cdot V_{ref}}{R_{dsmain}(R_s - k \cdot R_B)} \quad \text{eq1}$$

Equation 1 is the overload current with direct connection.

Where R_B is the resistor of bonding wire for source PAD.

$$I_m = \frac{k \cdot V_{ref}}{R_s} + \frac{V_{ref}}{R_{dsmain}} \quad \text{eq2}$$

Equation 2 gives an expression for the limiting current for the MX5012D in linear mode when the eFuse is wired in Kelvin mode.

Connection of RLIM current limit setting resistor can be made as shown in Fgure1 (Kelvin connection), or Figure 3 (Direct connection). Both connections result in a similar current limit threshold and behavior. It is important to make sure that layout trace connecting RLIM resistor to pins 4 and 6 is as short as possible. The shortest possible distance on a PCB must be used to connect pin 6 to RLIM resistor before pin 6 is connected to a common load node.

Overvoltage Clamp

The overvoltage clamp consists of an amplifier and reference. It monitors the output voltage and if the input voltage exceeds 14V (typical), the gate drive of the main FET is reduced to limit the output. This is intended to allow operation through transients while protecting the load. If an overvoltage condition exists for many seconds, the device may overheat due to the voltage drop across the FET combined with the load current. In this event, the thermal protection circuit would shut down the device. Refer to Figure11 for typical overvoltage clamp behavior.

Undervoltage Lockout

The undervoltage lockout circuit uses a comparator with hysteresis to monitor the input voltage. If the input voltage drops below the specified level, the output switch will be switched to a high impedance state.

Slew Rate Control

The dv/dt circuit brings the output voltage up under a linear, controlled rate regardless of the load impedance characteristics. An internal ramp generator creates a linear ramp, and a control circuit forces the output voltage to follow the ramp, scaled by a factor.

The default ramp time is approximately 1ms. This pin includes an internal current source of approximately 1uA. Since the current level is very low, it is important to use a ceramic cap or other low leakage capacitor. Aluminum electrolytic capacitor are not recommended for this circuit. The ramp time from 10% to 90% of the nominal output voltage can be determined by the following equation:

$$C_{ext} = \left(\frac{t}{0.5E06}\right) - 1.4nF$$

Where C_{ext} is in Farads, t is in seconds

Anytime that the unit shuts down due to a fault, enable shutdown, or recycling of input power, the timing capacitor will be discharged and the output voltage will ramp from 0 at turn on. Refer to Figure9 and 10 for slew rate control and typical slew rate behavior.

EN/Fault

The EN/Fault pin is a multi-function, bidirectional pin that can control the output of the chip as well as send information to other devices regarding the state of the chip. When this pin is low the output of the fuse will be turned off. When this pin is high the output of the fuse will be turned on. If a thermal fault occurs, this pin will be pulled low to an intermediate level by an internal circuit. To use as a simple enable pin, an open drain or open collector device should be connected to this pin. Due to its tri-state operation, it should not be connected to any type of logic with an internal pull-up device. Do not connect external capacitor directly to this pin.

If the chip shuts down due to the die temperature reaching its thermal limit, this pin will be pulled down to an intermediate level. This signal can be monitored by an external circuit to communicate that a thermal shutdown has occurred. If this pin is tied to another device in this family, a thermal shutdown of one device will cause both devices to disable their outputs. Both devices will turn on once the fault is removed for the auto-retry devices.

Since this is a latching thermal device, the outputs will be enabled after the enable pin has been pulled to ground with an external switch and then allowed to go high of after the input power has been recycled.

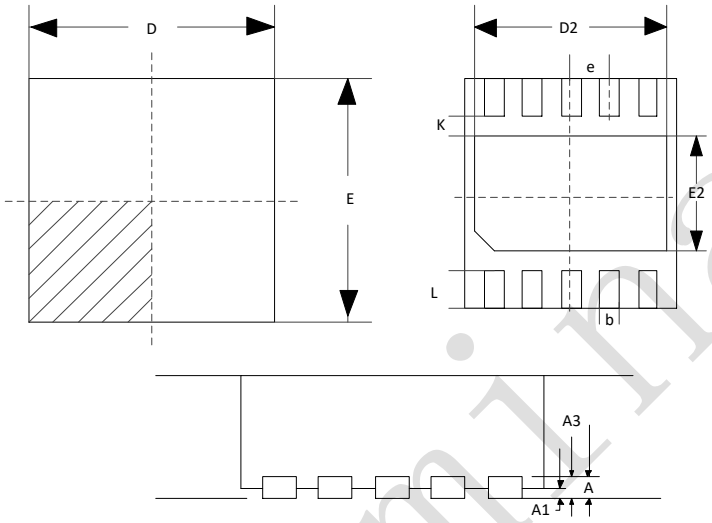
Thermal Protection

The MX5012D includes an internal temperature sensing circuit that sense the temperature on the die of the power MOSFET. If the temperature on the die reaches 175℃，the device will shut down, and remove power from the load. Output power can be restored by either recycling the input power or toggling the enable pin. Power will automatically be reapplied to the load for auto-retry devices once the die

temperature has been reduced by 45℃.

The thermal limit has been set high intentionally, to increase the trip time during high power transient events. It is not recommended to operate this device above 150℃ for extended period of time.

The similar devices from different voltage families can be configured together as shown in Figure2 for a common thermal shutdown.



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80			
A1	0.00	0.03	0.05			
A3	0.20REF					
b	0.25	0.30	0.35			
D	4.00BSC					
D2	3.30	3.40	3.50			
E	4.00BSC					
E2	2.69	2.79	2.89			
e	0.80BSC					
K	0.20					
L	0.30	0.40	0.50			

WDFN4*4 for MX5012D

Restrictions on Product Use

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