GENERAL DESCRIPTION

The MX5114T is designed to drive low-side MOSFETs in boost-type configurations or to drive secondary synchronous MOSFETs in isolated topologies. With strong sink current capability, the MX5114T can drive multiple MOSFETs in parallel. The MX5114T also has the features necessary to drive low-side enhancement mode Gallium Nitride (GaN) FETs. The MX5114T provides inverting and noninverting inputs to satisfy requirements for inverting and noninverting gate drive in a single device type. The inputs of the MX5114 are TTL/CMOS Logic compatible and withstand input voltages up to 18 V regardless of the VDD voltage. The MX5114T has split gate outputs, providing flexibility to adjust the turn on and turn off strength independently. The MX5114T has fast switching speed and minimized propagation delays, facilitating high-frequency operation. The MX5114T is available in a 6-pin SOT23-6 package.

FEATURES

- ♦ Independent Source and Sink Outputs for Controllable Rise and Fall Times
- ♦ 4V to 18V Single Power Supply
- ♦ 7.6A Peak Sink and Source Drive Current
- ♦ 0.20Ω Open-drain Pulldown Sink Output
- ♦ 0.25Ω Open-drain Pullup Source Output
- ♦ 10ns (Typical) Propagation Delay
- ♦ Matching Delay Time Between Inverting and Noninverting Inputs
- ♦ TTL/CMOS Logic Inputs
- ♦ Up to 18V Logic Inputs (Regardless of VDD Voltage)
- ♦Low Input Capacitance: 2.5pF (Typical)
- ♦–40°C to 125°C Operating Temperature Range
- ♦ 6-Pin SOT23-6L

APPLICATIONS

Battery Management System

Lidar Driver for Distance Test

Boost Converters

Flyback and Forward Converters

Secondary Synchronous FETs Drive in Isolated Topologies

These are Pb-free device

Motor Control

GENERAL INFORMATION

Ordering information

Part Number	Description
MX5114T	SOT23-6L

Package dissipation rating

Package	RθJA（℃/W）
SOT-23 (6)	108.1

Absolute maximum ratings

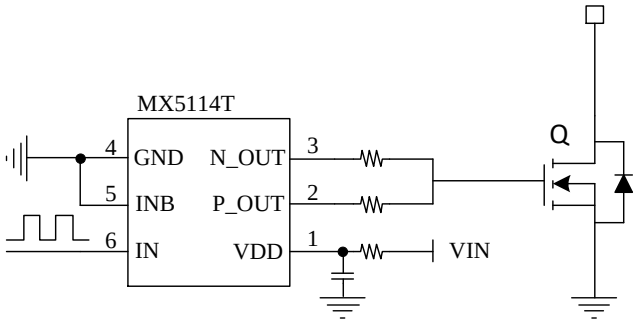
Parameter	Value
VDD to GND	-0.3 to 20V
IN, INB to GND	-0.3 to 20V
N_OUT to GND	-0.3 to VDD+0.3V
P_OUT to GND	-0.3 to VDD+0.3V
Junction temperature	150℃
Storage temperature, Tstg	-55 to 150℃
Leading temperature （soldering，10secs）	260℃
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

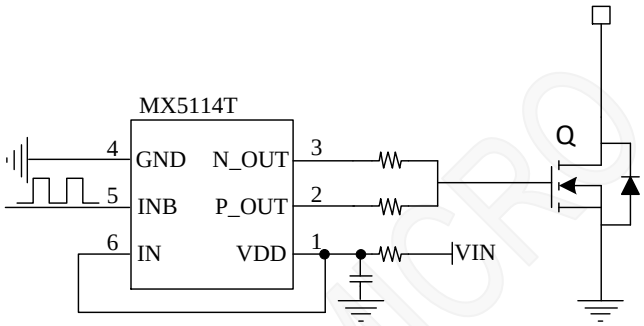
Recommended operating condition

Symbol	Parameter	Range
VDD	VDD supply voltage	4-18V
Junction temperature		-40~125℃
PD	Power dissipation	0.59W

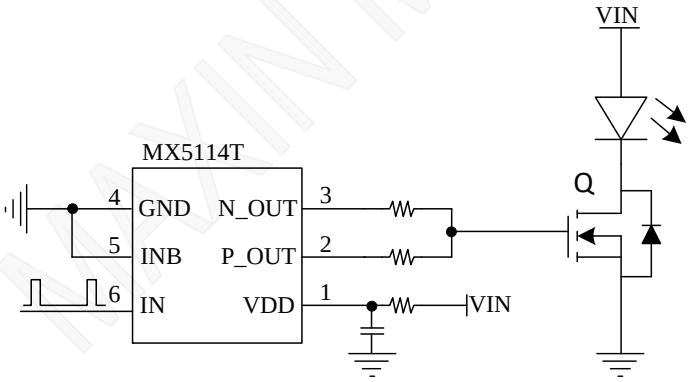
TYPICAL APPLICATION



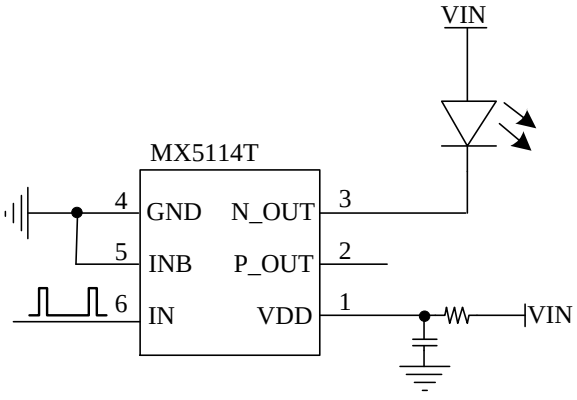
Noninverting input and source/sink current can be adjusted independently



Inverting input and source/sink current can be adjusted independently

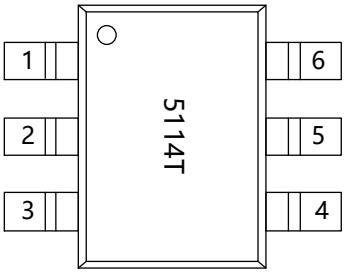


Laser driver for distance with external MOSFET



Laser driver for distance with internal MOSFET

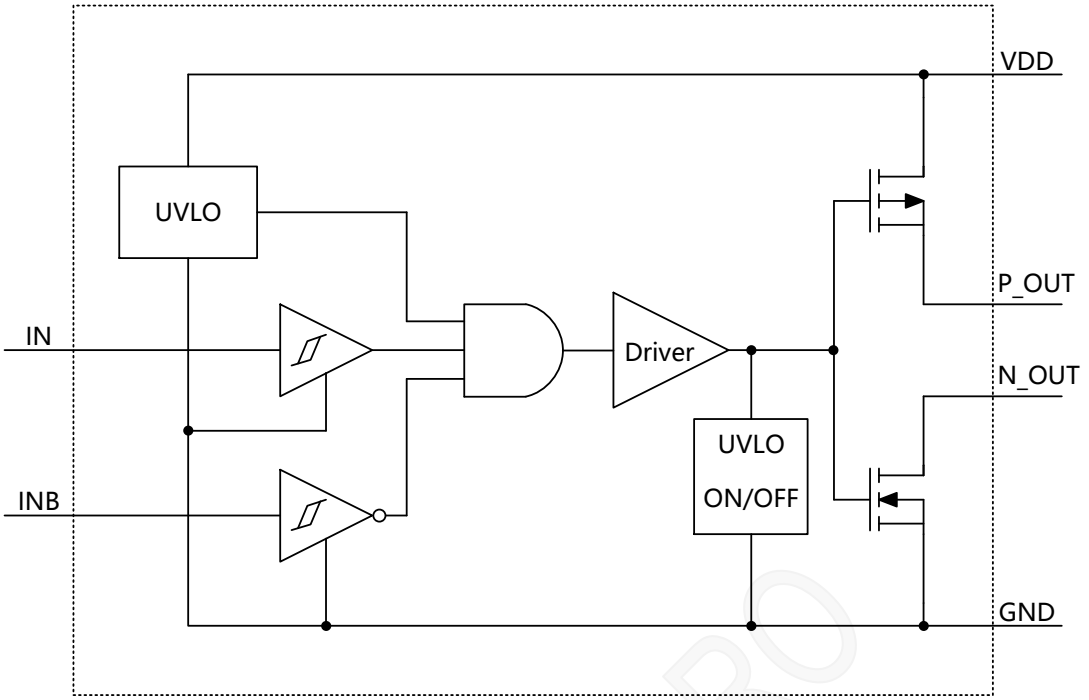
TERMINAL ASSIGMENTS



Pin information

PIN NO.	PIN name	Description
1	VDD	Gate drive supply Locally decouple to GND using low ESR/ESL capacitor located as close as possible to the IC.
2	P_OUT	Source-current output Connect to the gate of the MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turn on speed.
3	N_OUT	Sink-current output Connect to the gate of the MOSFET with a short, low inductance path. A gate resistor can be used to adjust the turnoff speed.
4	GND	Ground All signals are referenced to this ground.
5	INB	Inverting logic input Connect to GND when not used.
6	IN	Noninverting logic input Connect to VDD when not used.

BLOCK DIAGRAM

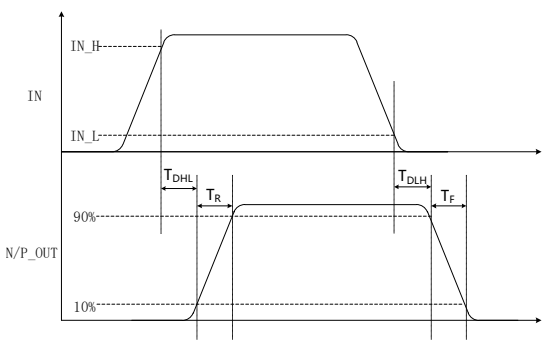


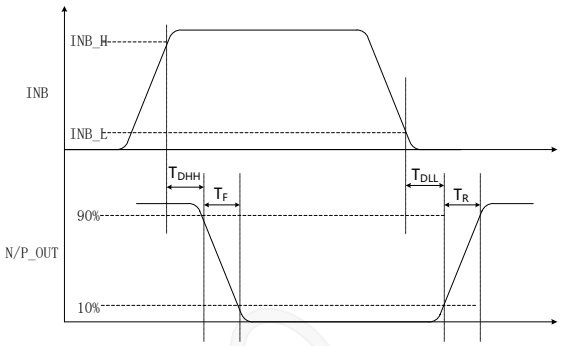
Electrical characteristics

（TA=25℃，VDD=12V, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
POWER SUPPLY						
I_{DD}	Supply current， VDD=12V			1.0	2.5	mA
I_{DD_OFF}	VDD=3.0V，IN=GND，INB=VDD			50	100	μA
	VDD=3.0V，IN=VDD，INB=GND			50	100	μA
U_{VLO_ON}	UVLO rising threshold	VDD rising	3.1	3.3	3.5	V
U_{VLO_OFF}	UVLO falling threshold	VDD falling	3.5	3.85	4.2	V
U_{VLO_HYS}	UVLO threshold hysteresis		0.2	0.5	0.8	V
LOGIC INPUT						
V_{IN_H}	Noninverting input high voltage	IN input rising	1.8	2.1	2.4	V
V_{IN_L}	Noninverting input low voltage	IN input falling	0.9	1.2	1.5	V
V_{INB_H}	Inverting input high voltage	INB input rising	1.8	2.1	2.4	V
V_{INB_L}	Inverting input low voltage	INB input falling	0.9	1.2	1.5	V
R_{INBH}	Inverting input pull up resistor			400		kΩ
R_{INL}	Noninverting input pull down resistor			400		kΩ
N-CHANNEL OUTPUT						
R_{ON_N}	Output resistance-pulling down @ 4.5V	VDD=4.5V, IIN_OUT=-50mA		0.60	0.85	Ω
	Output resistance-pulling down @ 10V	VDD=10V, IIN_OUT=-50mA		0.4	0.60	Ω
I_{PK_N}	Peak sink current			-7.6		A
P-CHANNEL OUTPUT						
R_{ON_P}	Output resistance-pulling up @ 4.5V	VDD=4.5V, IIN_OUT=-50mA		0.60	0.85	Ω
	Output resistance-pulling up @ 10V	VDD=10V, IIN_OUT=-50mA		0.40	0.60	Ω
I_{PK_P}	Peak source current			7.6		A
SWITCHING CHARACTERISTICS						
C_{IN}	Input capacitance			2.5		pF
T_{RISE}	Rise time	C_{LOAD}=1.8nF		6	12	ns

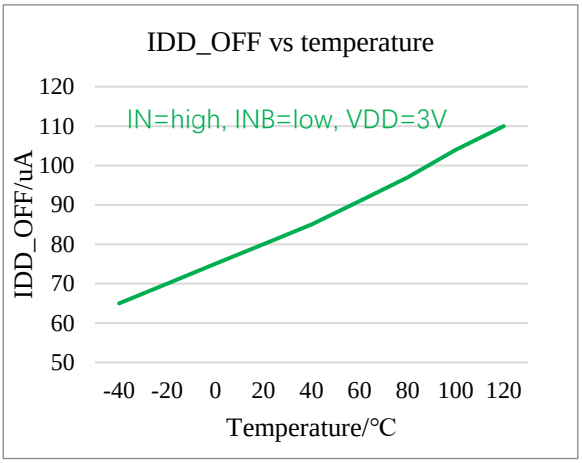
T_{FALL}	Fall time	C_{LOAD}=1.8nF		6	12	ns
T_{DLH}	Propagation delay, Low to High, noninverting	C_{LOAD}=1.8nF	5	15	20	ns
T_{DHL}	Propagation delay, High to Low, noninverting	C_{LOAD}=1.8nF	5	10	20	ns
T_{DHH}	Propagation delay, High to High, inverting	C_{LOAD}=1.8nF	5	10	20	ns
T_{DLL}	Propagation delay, Low to Low, inverting	C_{LOAD}=1.8nF	5	10	20	ns



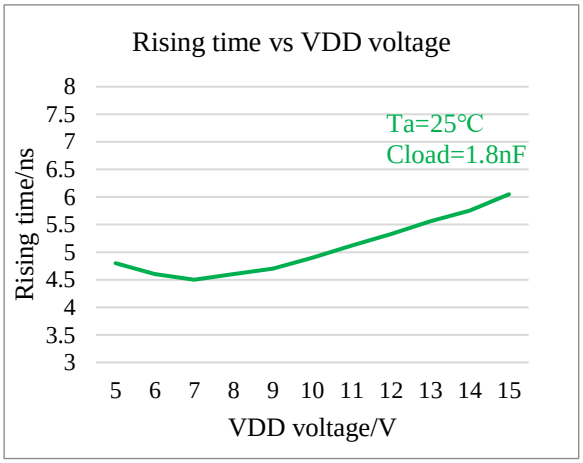


Note：P_OUT and N_OUT are tied together

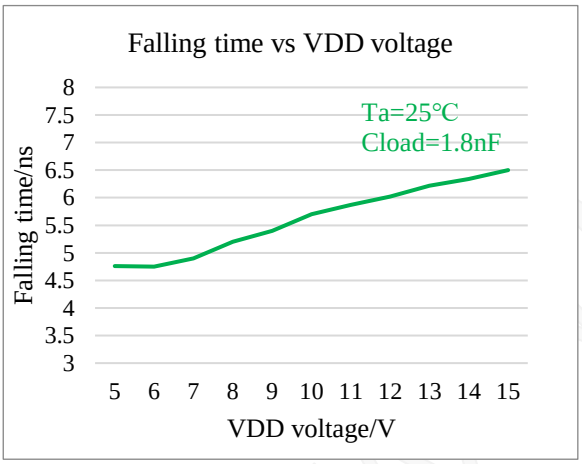
Characteristic plots



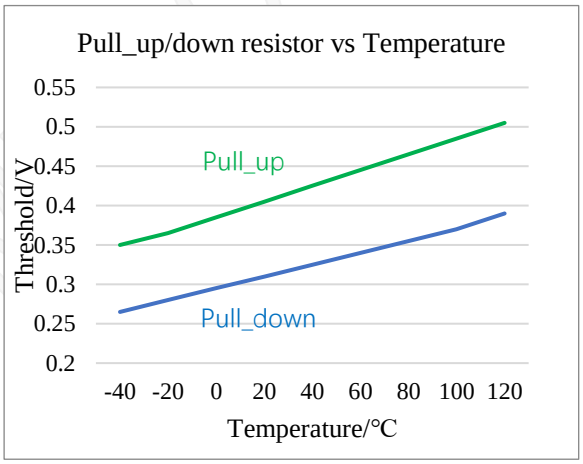
Operation current vs frequency with Cload=1.8nF



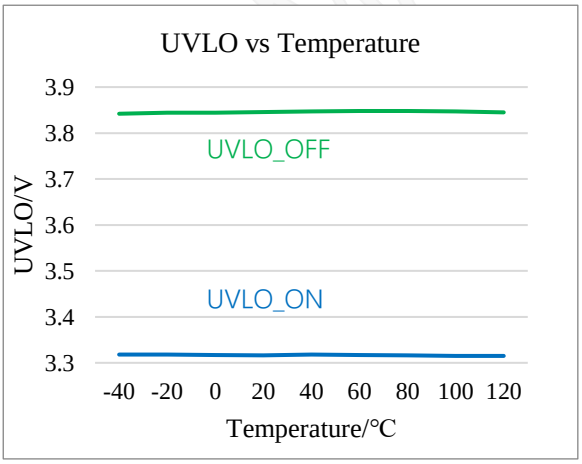
Rising time vs VDD voltage with load is 1.8nF



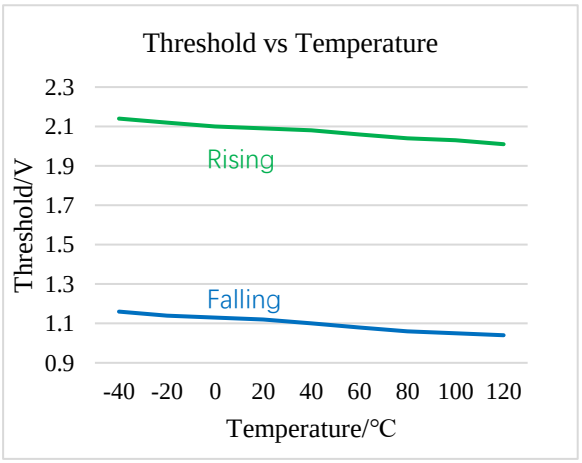
Falling time vs VDD voltage with load is 1.8nF



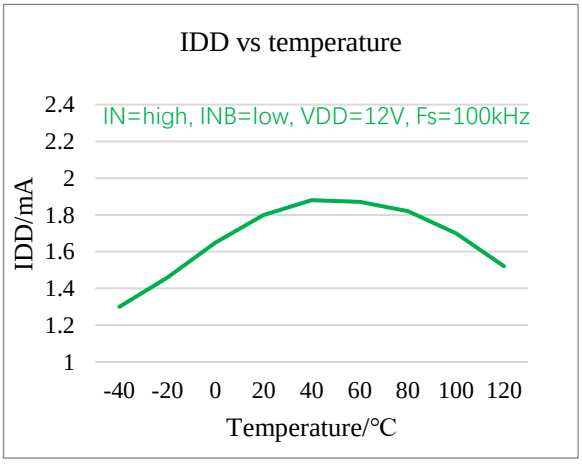
Pull up and pull down resistor vs temperature



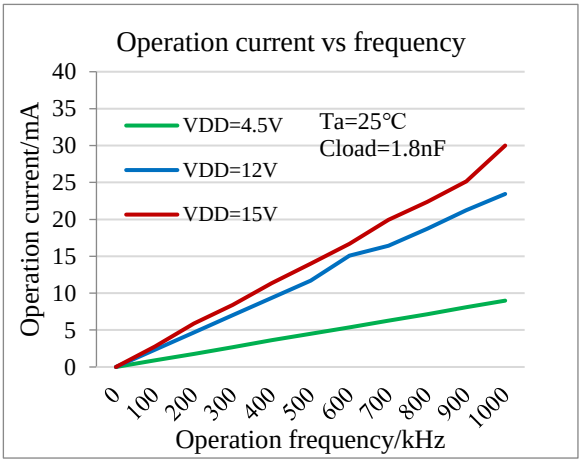
UVLO vs temperature



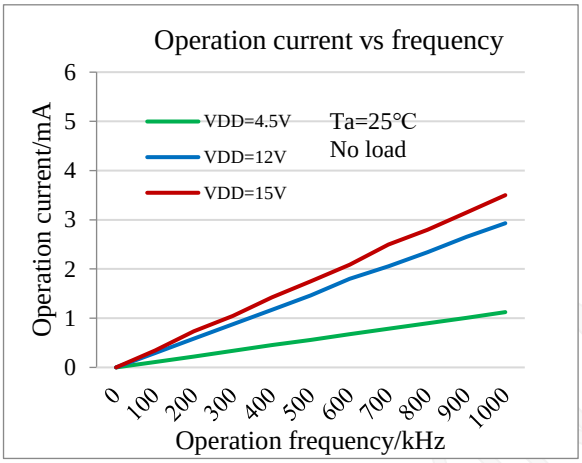
IN and INB high and low threshold vs temperature



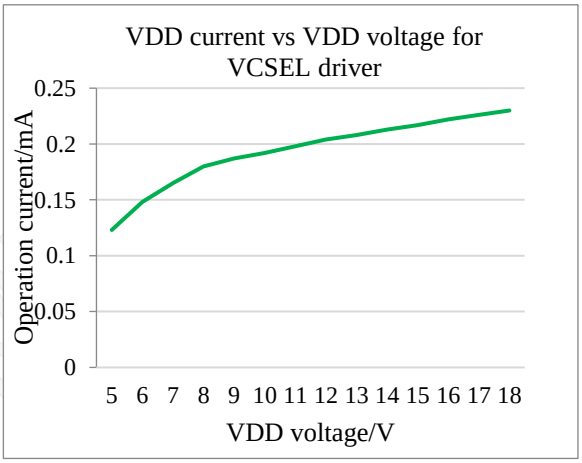
Operation current vs temperature



Operation current vs frequency with different VDD



Operation current vs frequency with no load



VDD current vs VDD voltage with only N_OUT

Operation description

The MX5114T is a single low-side gate driver with 7.6A/7.6A peak sink/source drive current capability. Inputs of the MX5114T are TTL Logic compatible and can withstand the input voltages up to 18V regardless of the VDD voltage. This allows inputs of the MX5114T to be connected directly to most PWM controllers. The split outputs of the MX5114T offer flexibility to adjust the turn on and turn off speed independently by adding additional impedance in either the turn on path or the turn off path.

The MX5114T startup logic is optimized to drive ground-referenced N channel MOSFETs with an under voltage lockout function to ensure that the IC starts up in an orderly fashion. When VDD is rising, yet below the UVLO level, this circuit holds the output LOW, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.5V before the part shuts down. This hysteresis helps prevent chatter when low VDD supply voltages have noise from the power switching. This configuration is not suitable for driving high side P channel MOSFETs because the low output voltage of the driver would turn the P channel MOSFET on with VDD below the UVLO level.

VDD bypass capacitor guidelines

To enable this IC to turn a device on quickly, a local high frequency bypass capacitor, with low ESR and ESL should be connected between the VDD and GND pins with minimal trace length. This capacitor is in addition to the bulk electrolytic capacitance of 10uF to 47uF commonly found on the driver and controller bias circuits.

A typical criterion for choosing the value of bypass capacitor is to keep the ripple voltage on the VDD supply to ⩽5%. This is often achieved with a value ⩾20 times the equivalent load capacitance, defined here as QG/VDD. Ceramic capacitors of 0.1uF to 1uF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

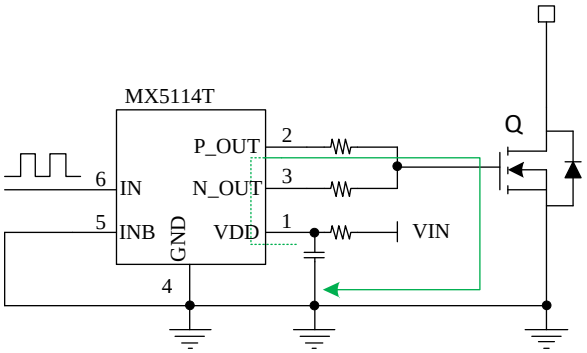
If circuit noise affects normal operation, the value of bypass capacitor may be increased to 50-100 times the equivalent load capacitance, or bypass capacitor may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1-10nF mounted closest to the VDD and GND pins to carry the higher frequency components of the current pulses.

Layout and connection guidelines

The MX5114T family of gate drivers incorporates fast-reacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 7.6A to facilitate voltage transition times from under 10ns to over 150ns. The following layout and connection guidelines are strongly recommended:

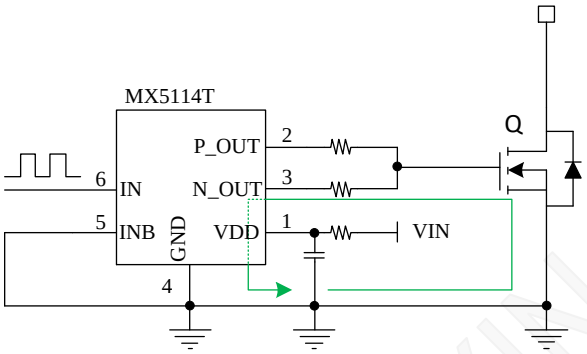
- Keep high current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.
- In noisy environments, it may be necessary to tie inputs of an unused PIN to VDD or GND using short traces to prevent noise from causing spurious output switching.
- Many high speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long IN, INB, or N_OUT, P_OUT leads. For best results, make connections to all pins as short and direct as possible.
- The MX5114T is compatible with many other industry standard drivers. In single input pin IN, there is an internal resistor tied to GND and INB tied to VDD to enable the driver by default, this should be considered in the PCB layout.
- The turn on and turn off current paths should be minimized, as discussed in the following section

The figure below shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized bypass capacitor acts to contain the high peak current pulses within this driver MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.



Current path for MOSFET turn on

The figure below shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn off times, the resistance and inductance in this path should be minimized.



Current path for MOSFET turn off

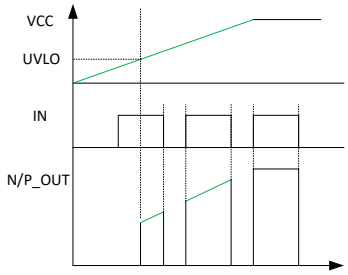
Truth table of logic operation

The MX5114T truth table indicates the operational states using the dual input configuration. MX5114T can be used in laser distance test, and only INB and N_OUT can be used without external NMOSFET. And at this time, the IN must be connected to VDD pin.

IN	INB	P_OUT	N_OUT
L	L	Open Circuit	L
L	H	Open Circuit	L
H	L	H	Open Circuit
H	H	Open Circuit	L

Operational waveforms

At power up, the driver output remains LOW until the VCC voltage reaches the turn on threshold. The magnitude of the output pulsed rises with VCC until steady state VCC is reached. The operation illustrated in the figure below shows that the output remains LOW until the UVLO threshold is reached, then the output is in phase with the input.



MX5114T start up waveform

Power dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$P_{DISS}=P_{DC}+P_{GATE}$

The DC portion of the power dissipation is $P_{DC}=I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so on, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of internal parasitic capacitances, parasitic shoot-through). The MX5114T features low quiescent currents and contains internal logic to minimize any shoot-through in the output driver stage. Thus, the effect of the PDC on the total power dissipation within the gate driver can be assumed to be negligible.

Gate driving loss P_{GATE} is the most significant power loss result from suppling gate current to switch the load on and off at the switching frequency. The power dissipation that results from driving a power switch at a special gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, F_{SW}, is determined by:

$$P_{GATE} = Q_G \times V_{GS} \times F_{SW}$$

To give a numerical example, assume for a 12V VDD system, the power MOSFETs which have a total charge of 60nC at VGS=12V. Therefore, two devices in parallel would have 120nC gate charge. At a switching frequency of 100kHz, the total power dissipation is:

$P_{DISS}=P_{DC}+P_{GATE}$

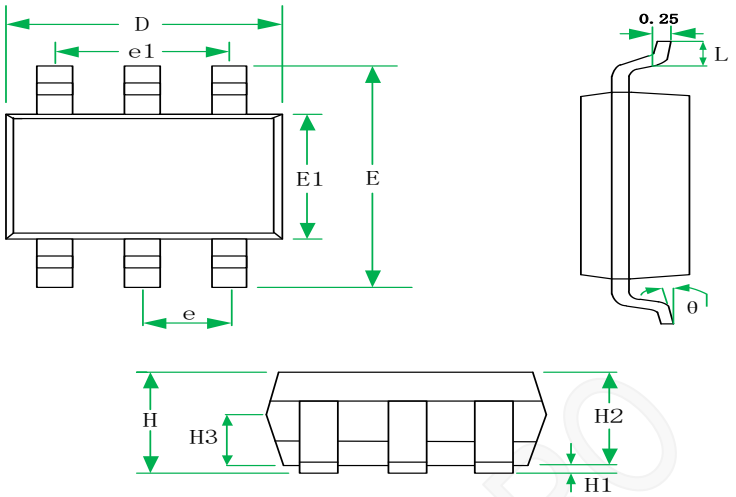
$P_{DC}=12V \times 1.4mA=0.0168W$

$P_{GATE}=120nC \times 12V \times 100kHz=0.144W$

So the total dissipation is:

$P_{DISS}=P_{GATE}+P_{DC}=0.0168W+0.144W=0.161W$

Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
H			1.45			0.057
H1	0.04		0.15	0.0016		0.0059
H2	1.00	1.10	1.20	0.039	0.043	0.047
H3	0.55	0.65	0.75	0.022	0.026	0.029
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.074BSC		
L	0.30		0.60	0.012		0.024
θ	0		8°	0		8°

SOT23-6 for MX5114T

Restrictions on Product Use

◆ MAXIN micro is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing MAXIN products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such MAXIN products could cause loss of human life, bodily injury or damage to property.

◆ In developing your designs, please ensure that MAXIN products are used within specified operating ranges as set forth in the most recent MAXIN products specifications.

◆ The information contained herein is subject to change without notice.