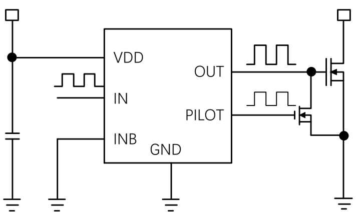
GENERAL DESCRIPITION

The MX5134 is a high speed single low side driver capable of sinking and sourcing 7.6A and 4.5A peak currents. The MX5134 has inverting and noninverting inputs that give the user greater flexibility in controlling the FETs. The MX5134 features one main output and an extra gate drive output. The PILOT pin logic is complementary to the OUT pin, and can be used to drive a small FET located close to the main power FET. This configuration minimizes the turn off loop and reduces the consequent parasitic inductance. It is particularly useful for driving high speed FETs or multiple FETs in parallel. The MX5134 is available in the 6-pin SOT23 package.

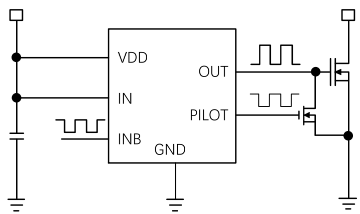
FEATURES

- ♦ 4V to 15V Single Power Supply
- ♦ 7.6A and 4.5A Peak Sink and Source Drive Current for Main Output
- ♦ 820mA and 660mA Peak Sink and Source Current for PILOT Output
- ♦ 0.70Ω Open-drain Pullup Source Output
- ♦ 10ns (Typical) Propagation Delay
- ♦ Matching Delay Time Between Inverting and Noninverting Inputs
- ♦ TTL/CMOS Logic Inputs
- ♦ Up to 15V Logic Inputs (Regardless of VDD Voltage)
- ♦Low Input Capacitance: 2.5pF (Typical)
- ♦–40°C to 125°C Operating Temperature Range

TYPICAL APPLICATION



Noninverting Input



Inverting Input

APPLICATIONS

Battery Management System

Lidar Driver for Distance Test

Boost Converters

Power Factor Correction Converters

Motor Driver

GENERAL INFORMATION

Ordering information

Part Number	Description
MX5134	SOT23-6L

Package dissipation rating

Package	RθJA（℃/W）
SOT-23 (6)	108.1

Absolute maximum ratings

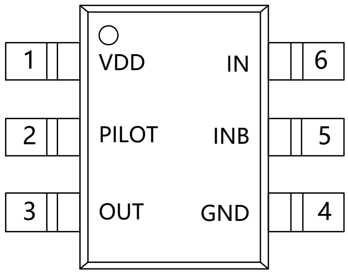
Parameter	Value
VDD to GND	-0.3 to 18V
IN+ to GND	-0.3 to 18V
OUT to GND	-0.3 to VDD+0.3V
Junction temperature	150℃
Storage temperature, Tstg	-55 to 150℃
Leading temperature （soldering，10secs）	260℃
ESD Susceptibility HBM	±2000V

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

Recommended operating condition

Symbol	Parameter	Range
VDD	VDD supply voltage	4-15V
Junction temperature		-40~125℃
PD	Power dissipation	0.59W

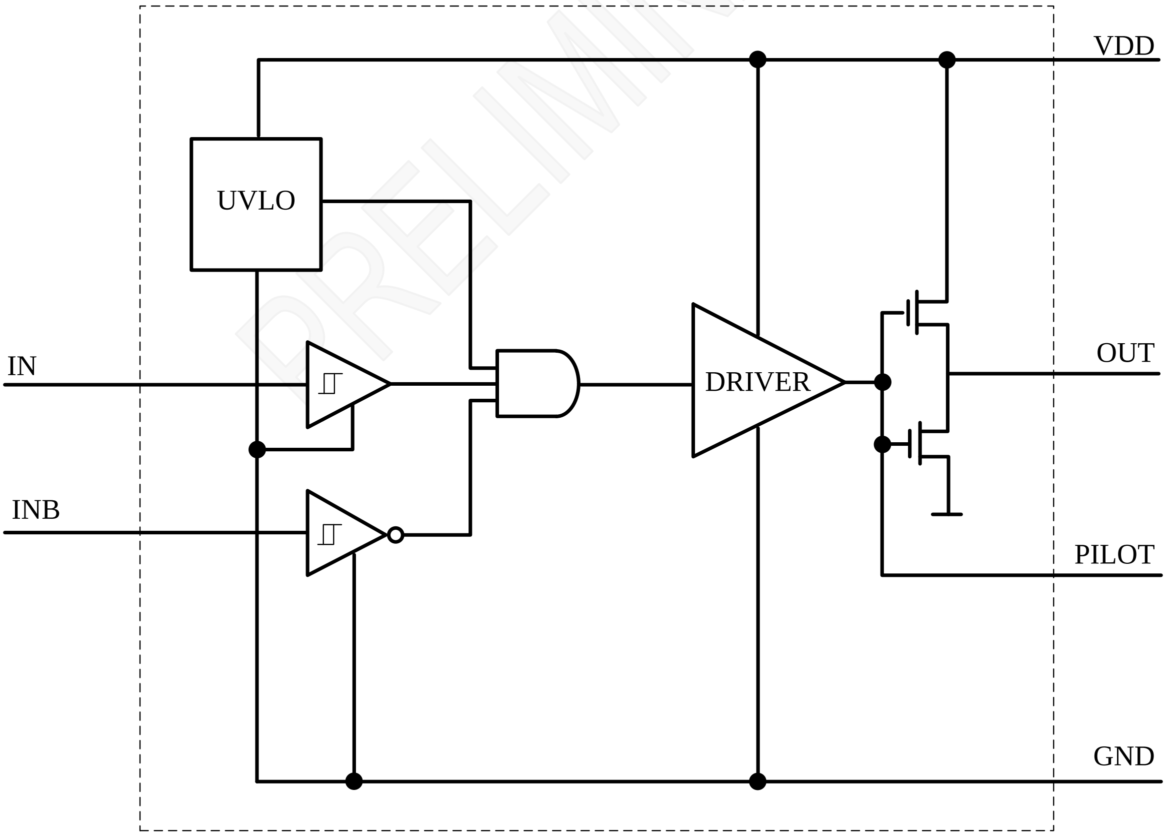
TERMINAL ASSIGMENTS



Pin information

PIN NO.	PIN name	Description
1	**VDD**	Gate drive supply. Locally decouple to GND using low ESR/ESL capacitor located as close as to the MX5134.
2	**PILOT**	Gate drive output for an external turnoff FET. Connect to the gate of a small turnoff MOSFET with a short, low inductance path. The turnoff FET provides a local turnoff path.
3	**OUT**	Gate drive output for the power FET. Connect to the gate of the power FET with a short, low inductance path. A gate resistor can be used to eliminate potential gate oscillations.
4	**GND**	Ground. All signals are referenced to this ground.
5	**INB**	Inverting logic input. Connect to GND when not used.
	IN	Noninverting logic input. Connect to VDD when not used.

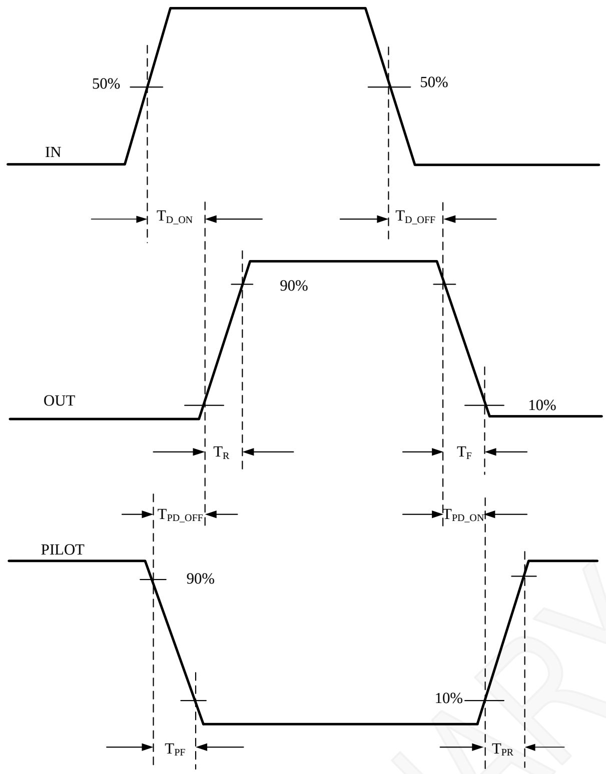
BLOCK DIAGRAM



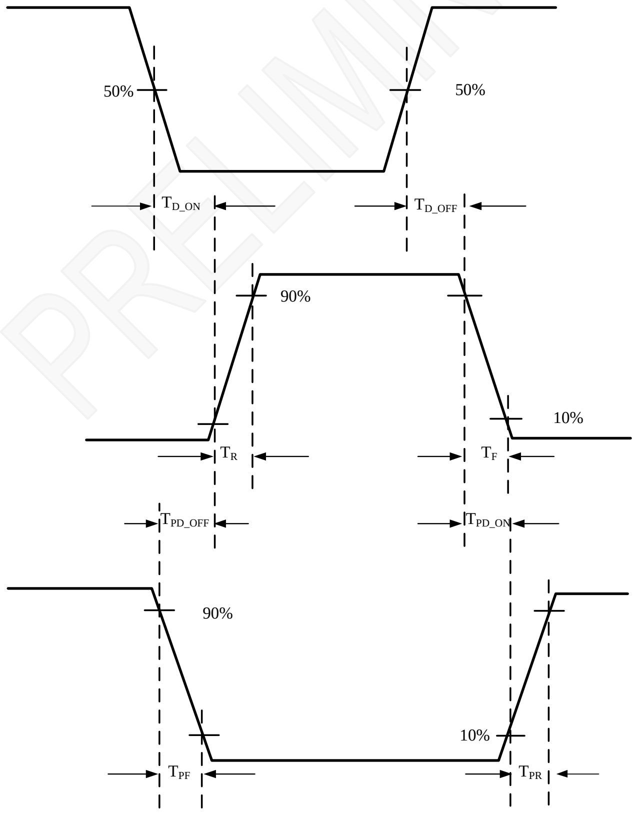
Electrical characteristics

（TA=25℃，VDD=12V, unless otherwise noted）

Symbol	Parameter	Test condition	Min	Typ.	Max	Unit
POWER SUPPLY						
I_{DD}	Supply current， VDD=12V	FS=25kHz		1.0	2.5	mA
I_{DD_OFF}	VDD=3.0V，IN=INB=GND			50	100	μA
	VDD=3.0V，IN==INB=VDD			50	100	μA
U_{VLO_ON}	UVLO rising threshold	VDD rising	3.1	3.3	3.5	V
U_{VLO_OFF}	UVLO falling threshold	VDD falling	3.5	3.85	4.2	V
U_{VLO_HYS}	UVLO threshold hysteresis		0.2	0.5	0.8	V
LOGIC INPUT						
V_{IN_H}	Noninverting input high voltage	IN input rising	1.8	2.1	2.4	V
V_{INB_H}	Inverting input high voltage		1.8	2.1	2.4	V
V_{IN_L}	Noninverting input low voltage	IN input falling	0.9	1.2	1.5	V
V_{INB_L}	Inverting input high voltage		0.9	1.2	1.5	V
R_{INL}	Noninverting input pull down resistor			400		kΩ
R_{INBH}	Inverting input pull up resistor			400		kΩ
OUTPUT						
V_{DD}-V_{OH}	High output voltage	VDD = 12 V, IOUT = 10 mA		4	9.0	mV
V_{OL}	Low output voltage	VDD = 12 V, IOUT =- 10 mA		4.5	9.5	mV
R_{ON_P}	Output resistance-pulling up @ 10V	VDD=10V, IOUT=10mA		0.45	0.65	Ω
	Output resistance-pulling up @ 4.5V	VDD=4.5V, IOUT=10mA		0.65	0.95	Ω
R_{ON_N}	Output resistance-pulling down @ 10V	VDD=10V, IOUT=-10mA		0.40	0.60	Ω
	Output resistance-pulling down @ 4.5V	VDD=4.5V, IOUT =-10mA		0.60	0.90	Ω
I_{SNK}	Peak sink current			-7.6		A
I_{SRC}	Source current			7.6		A
PILOT						
R_{ON_N}	PILOT output resistance pulling down	VDD=10V, PILOT=-100mA		3.5		Ω
		VDD=4.5V, PILOT=-100mA		4.5		Ω
$I_{SNK\text{-}P}$	Peak sink current for PILOT			820		mA
R_{ON_P}	PILOT output resistance pulling up	VDD=10V, PILOT=100mA		6.0		Ω
		VDD=4.5V, PILOT=100mA		10.0		Ω
I_{SRC_P}	Peak source current for PILOT			660		mA
SWITCHING CHARACTERISTICS						
C_{IN}	Input capacitance			2.5		pF
T_{RISE}	Rise time	C_{LOAD}=1.0nF		4		ns
T_{FALL}	Fall time	C_{LOAD}=1.0nF		3		ns
TPR	PILOT rise time	CL=330pF		9.5		ns
TPF	PILOT fall time	CL=330pF		4		ns
T_{D_ON}	Propagation delay, Low to High, noninverting	C_{LOAD}=1.0nF		15		ns
T_{D_OFF}	Propagation delay, High to Low, noninverting	C_{LOAD}=1.0nF		15		ns
TPD_ON	Out turn off to PILOT turn on propagation delay	CL=330pF		7		ns
TPD_OFF	PILOT turn off to out turn on propagation delay	CL=330pF		10		ns

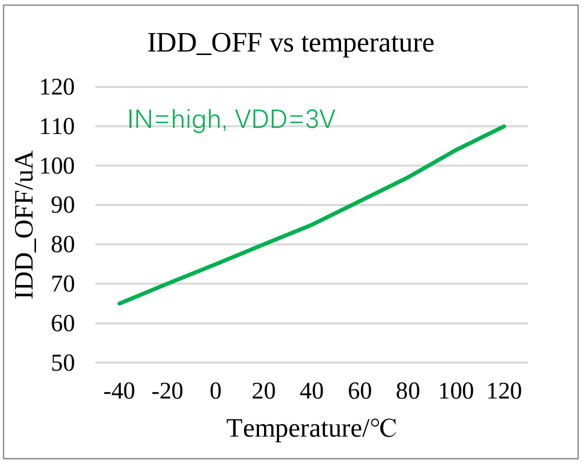


Timing diagram-noninverting input

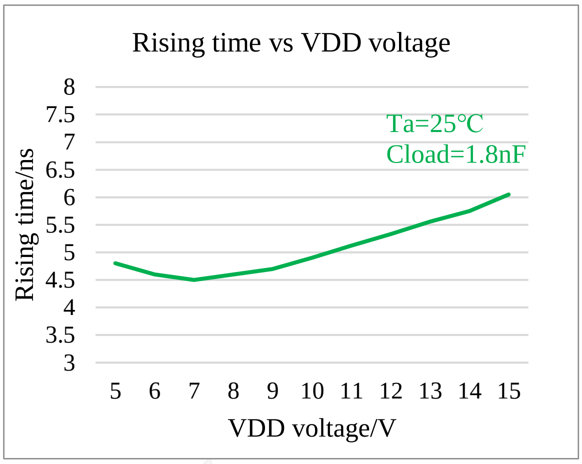


Timing diagram- inverting diagram

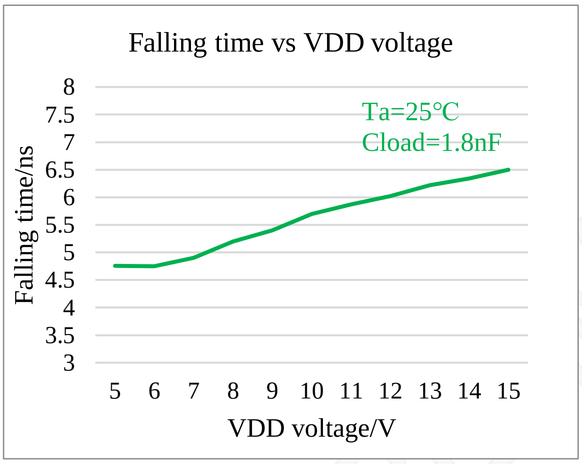
Characteristic plots



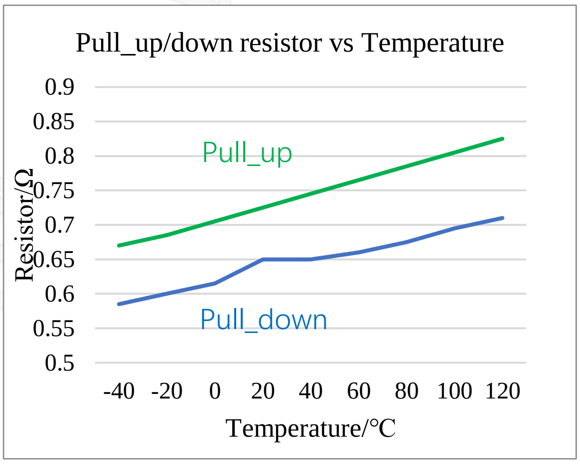
Operation current vs frequency with Cload=1.8nF



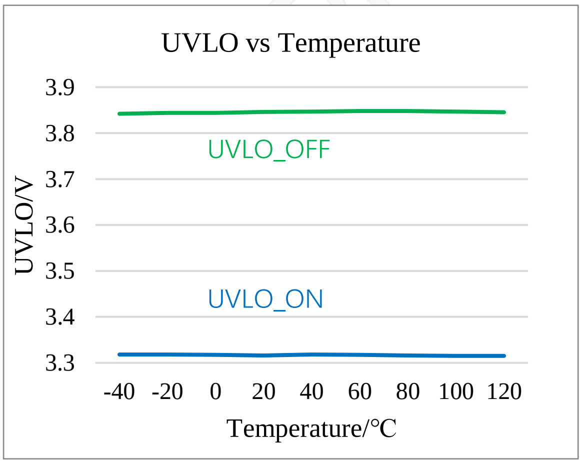
Rising time vs VDD voltage with load is 1.8nF



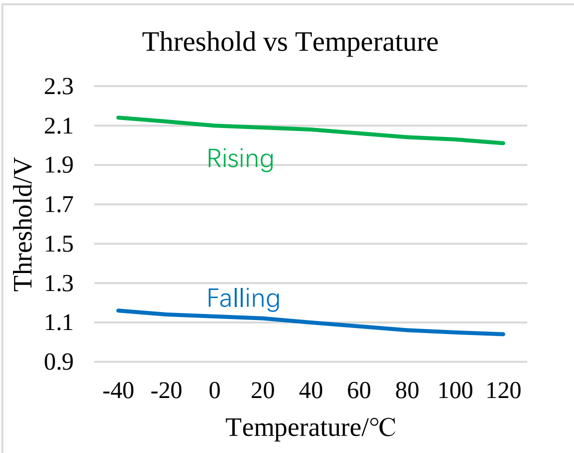
Falling time vs VDD voltage with load is 1.8nF



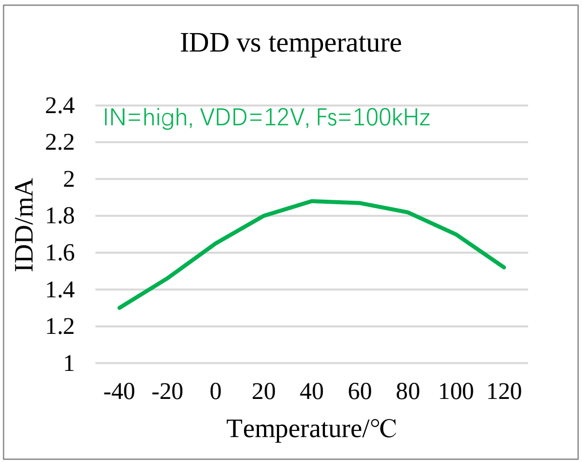
pull down resistor vs temperature



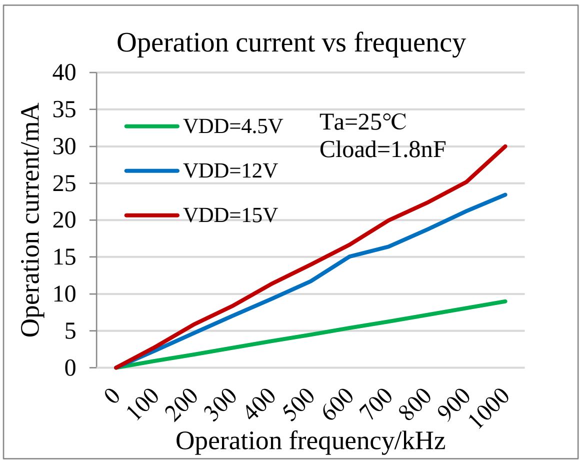
UVLO vs temperature



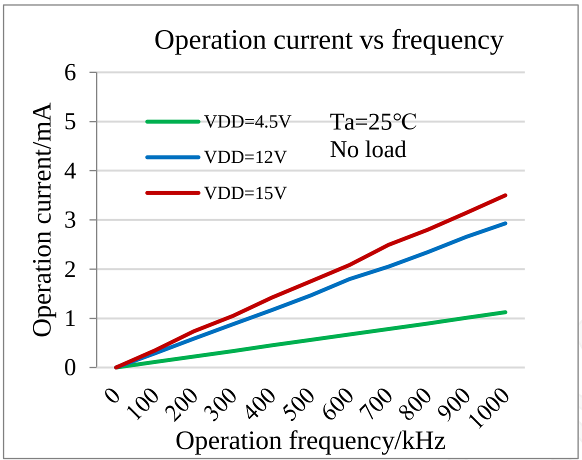
IN+ high and low threshold vs temperature



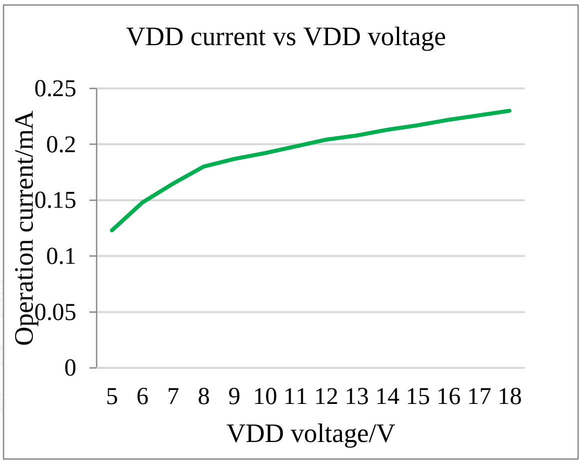
Operation current vs temperature



Operation current vs frequency with different VDD



Operation current vs frequency with no load



VDD current vs VDD voltage with OUT

Operation description

The MX5134 is a single low-side gate driver with one main output and a complementary output PILOT. The OUT pin has high 7.6A peak sink and source current and can be used to drive large power MOSFETs or multiple MOSFETs in parallel. The PILOT pin has 820mA and 660mA peak sink and source current, and is intended to drive an external turnoff MOSFET. The external turnoff FET can be placed close to the power MOSFETs to minimize the loop inductance, and therefore helps eliminate stay induced oscillations or undesired turn on. This feature also provides the flexibility to adjust turn on and turn off speed independently.

Feature Description

When using the external turn off switch, it is important to prevent the potential shoot-through between the external turn off switch and the MX5134 internal pullup switch. The propagation delay, T_{PD_ON} and T_{PD_OFF}, has been implemented in the MX5134 between PILOT and OUT pins, as depicted in the timing diagram. The turn on delay T_{PD_ON} is designed to be shorter than the turn off delay T_{PD_OFF} because the rising time of the external turn off can attribute to the additional delay time. It is also desirable to minimize T_{PD_ON} to favor the fast turn off of the power MOSFET.

The MX5134 offers both inverting and noninverting inputs to satisfy requirements for inverting and noninverting gate drive signals in a single device type. Inputs of the MX5134 are TTL and CMOS logic compatible and can withstand input voltages up to 15V regardless of the VDD voltage. This allows inputs of the MX5134 to be connected directly to most PWM controllers.

The MX5134 includes an UVLO circuit. When the VDD voltage is below the UVLO threshold voltage, the IN and INB inputs are ignored, and if there is sufficient VDD voltage, the OUT is pulled low. In addition, the PNP transistor will be on and clamp the OUT voltage below 1V. this feature ensures the OUT remains low even with insufficient VDD voltage.

Input to output logic

The design should specify which type of input to output configuration should be used. if turning on the power MOSFET when the input signal is in high state is preferred, then the noninverting configuration must be selected. If turning off the power MOSFET when the input signal is in high state is preferred, the inverting configuration must be chosen. The MX5134 device can be configured in either an inverting or noninverting input to output configuration respectively.

VDD bias supply voltage

The bias supply voltage applied to the VDD pin of the device should never exceed the values listed in recommended operating conditions. However, different power switches demand different voltage levels to be applied at the gate terminals for effective turn on and turn off. with an operating range from 4V to 15V, the MX5134 device can be used to drive a variety of power switches.

PILOT MOSFET selection

In general, a small sized 20V MOSFET with logic level gates can be used as the external turnoff switch. To achieve a fast switching speed and avoid the potential shoot through, select a MOSFET with the local gate charge less than 3nC. Verify that no shoot through occurs for the entire operating temperature range. In addition, a small Rds(on) is preferred to obtain the strong sink current capability. The power losses of the PILOT MOSFET can be estimated in the down equation.

$$P_g = \frac{1}{2} \cdot Q_{go} \cdot VDD \cdot F_{sw}$$

Where Q_{go} is the total input gate charge of the power MOSFET.

Layout and connection guideline

The MX5134 family of gate drivers incorporates fast-reacting input circuits, shortage propagation delays, and powerful output stages capable of delivering current peaks over 7.6A to facilitate voltage transition times from under 10ns to over 150ns. The following layout and connection guidelines are strongly recommended:

●Keep high current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL-level logic thresholds at driver inputs and enable pins.

●In noisy environments, it may be necessary to tie inputs of an unused pin to VDD or GND using short traces to prevent noise from causing spurious output switching.

●Many high speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re-triggering. These effects can be obvious if the circuit is tested in breadboarding or non-optimal circuit layouts with long IN+ or OUT leads. For best results, make connections to all pins as short and direct as possible.

● The MX5134 is compatible with many other industry standard drivers. In single input pin IN+, there is an internal resistor tied to GND to enable the driver by default, this should be considered in the PCB layout.

● The turn on and turn off current paths should be minimized.

Truth table of logic operation

The MX5134 truth table indicates the operational states.

IN	INB	OUT	PILOT
L	L	L	H
L	H	L	H
H	L	H	L
H	H	L	H

Power dissipation

Power dissipation of the gate driver has two portions as shown in equation below:

$P_{DISS}=P_{DC}+P_{GATE}$

The DC portion of the power dissipation is $P_{DC}=I_Q\times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and so on, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of internal parasitic capacitances, parasitic shoot-through). The MX5134 features low quiescent currents and contains internal logic to minimize any shoot-through in the output driver stage. Thus, the effect of the PDC on the total power dissipation within the gate driver can be assumed to be negligible.

Gate driving loss P_{GATE} is the most significant power loss result from suppling gate current to switch the load on and off at the switching frequency. The power dissipation that results from driving a power switch at a special gate-source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, F_{SW}, is determined by:

$$P_{GATE}=Q_G\times V_{GS}\times F_{SW}$$

To give a numerical example, assume for a 12V VDD system, the power MOSFETs which have a total charge of 60nC at VGS=12V. Therefore, two devices in parallel would have 120nC gate charge. At a switching frequency of 100kHz, the total power dissipation is:

$P_{DISS}=P_{DC}+P_{GATE}$

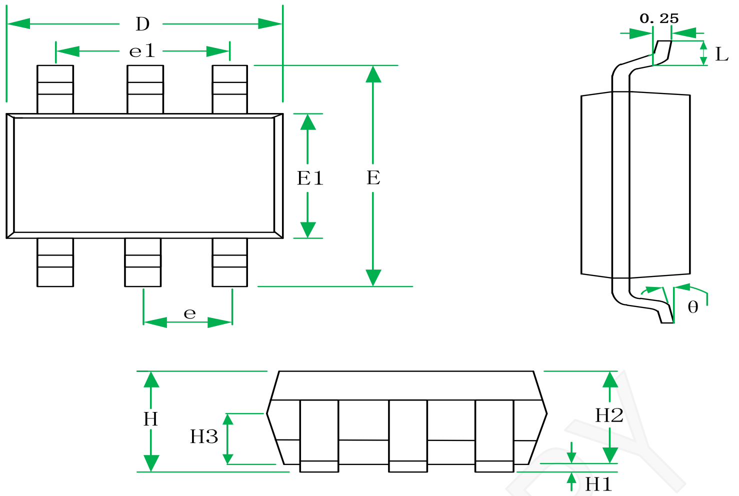
$P_{DC}=12V\times 1.4mA=0.0168W$

$P_{GATE}=120nC\times 12V\times 100kHz=0.144W$

So the total dissipation is:

$P_{DISS}=P_{GATE}+P_{DC}=0.0168W+0.144W=0.161W$

Package information



SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
H			1.45			0.057
H1	0.04		0.15	0.0016		0.0059
H2	1.00	1.10	1.20	0.039	0.043	0.047
H3	0.55	0.65	0.75	0.022	0.026	0.029
D	2.72	2.92	3.12	0.107	0.115	0.123
E	2.60	2.80	3.00	0.102	0.110	0.118
E1	1.40	1.60	1.80	0.055	0.063	0.071
e	0.95BSC			0.037BSC		
e1	1.90BSC			0.074BSC		
L	0.30		0.60	0.012		0.024
θ	0		8°	0		8°

SOT23-6 for MX5134

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