

# MX555ABH25M0000

#### Ultra-low Jitter 25MHz LVCMOS XO

#### ClockWorks<sup>TM</sup> FUSION

### **General Description**

The MX555ABH25M0000 is an ultra-low phase jitter XO with LVCMOS output optimized for high line rate applications.

### Features

- 25MHz LVCMOS
- Typical phase noise:
  - 100fs (Integration range: 1.875MHz-20MHz)
- ±50ppm total frequency stability
- -40°C to +85°C temperature range
- Industry standard 6-Pin 5mm x 3.2mm LGA package

## **Absolute Maximum Ratings**

Supply Voltage (VIN)	+3.6V
Lead Temperature (soldering, 10s)	260°C
Storage Temperature (T <sub>s</sub> )	125°C
ESD Rating (HBM)	

## **Electrical Characteristics**

VDD = 2.375 - 3.63V, TA =  $-40^{\circ}C$  to  $+85^{\circ}C$ , output terminated with 50 Ohms to VDD/ $2.^{1}$ 

#### Units Symbol Parameter Condition Min. Typ. Max. IDD Supply Current 95 mΑ Center Frequency F0 25 MHz Frequency Stability ±50 Note 2 ppm 220 Integration Range (12kHz to 20MHz) Øj Phase Noise fsRMS Integration Range (1.875MHz to 20MHz) 100 Start-Up Time Tstart 20 ms TR/TF Rise/Fall time 300 ps 45 Duty Cycle 55 % 2 VIH V Input High Voltage 3.3V Operation VDD + 0.3VIL Input Low Voltage 3.3V Operation -0.3 0.8 V VOH Output High Voltage LVCMOS output levels VDD - 0.6 V VOL Output Low Voltage LVCMOS output levels 0.6 V

Notes:

1. Guaranteed after thermal equilibrium.

2. Inclusive of initial accuracy, temperature drift, aging, shock, vibration from -40°C to +85°C.

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## **Operating Ratings**

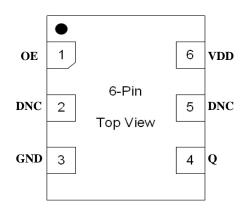
Supply Voltage (VIN)	+2.375V to +3.63V
Ambient Temperature (TA)	$\dots$ -40°C to +85°C

# **Ordering Information**

Ordering Part Number	Marking Line 1	Marking Line 3	Shipping	Package
MX555ABH25M0000	MX555A	BH0250	Tube	6-Pin 5mm x 3.2mm LGA
MX555ABH25M0000 TR	MX555A	BH0250	Tape and Reel	6-Pin 5mm x 3.2mm LGA

Devices are Green and RoHS compliant. Sample material may have only a partial top mark.

# **Pin Configuration**



# **Pin Description**

Pin Number	Pin Name	Pin Type	Pin Level	Pin Function
1	OE	I, SE	LVCMOS	Output Enable, disables output to tri-state, 1 = Disabled, 0 = Enabled, 50k Ohms Pull-Down
2	DNC			Make no connection, leave floating.
3	GND	PWR		Power Supply Ground
4, 5	Q, DNC	O, SE	LVCMOS	Clock Output Frequency = 25MHz
6	VDD	PWR		Power Supply

## TOP VIEW BOTTOM VIEW 0.900 bbb C 悤 BSC 2.600 SIDE VIEW 1.270 BSC RECOMMENDED LAND PATTERN DE Di nsions are in millimeters 2. Di 3. 'e' represents the basic LGA pitch 4. 'n' is the maximum no. of Land for 5. Package warp shall be 0.050 max. 1.85 1.951 6. Substrate base is BT Resin DETAIL A 7. The Pin#1 corner must be identified on top side .111 1.15 SCALE 5.1 8. Reference Jedec Spec M0-220

### Package Information and Recommended Land Pattern for 6-Pin LGA<sup>3</sup>

Note:

6-Pin LGA (5x3.2mm)

3. Package information is correct as of the publication date. For updates and most current information, go to www.micrel.com.

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