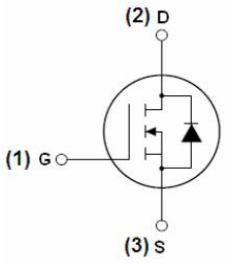
N-Channel Enhancement Mode Power MOSFET

Description

The MX6018 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.



Schematic diagram

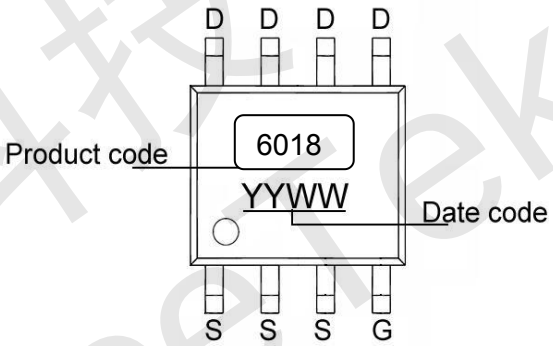
General Features

- V_{DS} =60V，I_D =18A
- $R_{DS(ON)}$(Typ.)10mΩ @ Vgs=10V
- $R_{DS(ON)}$(Typ.)13.5mΩ @ Vgs=4.5V

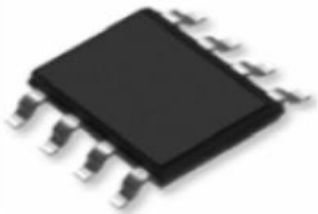
High density cell design for ultra low Rdson
Fully characterized Avalanche voltage and current
Special process technology for high ESD capability
Good stability and uniformity with high E_{AS}
Excellent package for good heat dissipation

Application

Power switching application
Hard Switched and High Frequency Circuits
Uninterruptible Power Supply



Marking and pin assignment



SOP-8 top view

Absolute Maximum Ratings (TA=25℃ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	18	A
Drain Current-Continuous(Tc=100℃)	I_D (100℃)	12	A
Pulsed Drain Current	I_{DM}	35	A
Maximum Power Dissipation	P_D	2.5	W

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com

Electrical Characteristics (TA=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1.2	2.0	2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=18A	-	10	14	mΩ
		V_{GS}=4.5V, I_D=10A	-	13.5	18	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=10A	20	-	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C_{lss}	V_{DS}=15V,V_{GS}=0V, F=1.0MHz	-	3240	-	PF
Output Capacitance	C_{oss}		-	210	-	PF
Reverse Transfer Capacitance	C_{rss}		-	146	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DD}=30V, R_D=8A, V_{GS}=10V,R_{GEN}=3Ω	-	10.6	-	nS
Turn-on Rise Time	t_r		-	9	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	65.6	-	nS
Turn-Off Fall Time	t_f		-	4.8	-	nS
Total Gate Charge	Q_g	V_{DS}=48V,I_D=8A, V_{GS}=4.5V	-	30	-	nC
Gate-Source Charge	Q_{gs}		-	10.7	-	nC
Gate-Drain Charge	Q_{gd}		-	9.4	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=10A	-	-	1.2	V
Diode Forward Current (Note 2)	I_S	-	-	-	8	A
Reverse Recovery Time	t_{rr}	TJ = 25°C, IF =8A di/dt = 100A/μs (Note3)	-	18	-	nS
Reverse Recovery Charge	Qrr		-	15.6	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Thermal Characteristic

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	50	℃/W

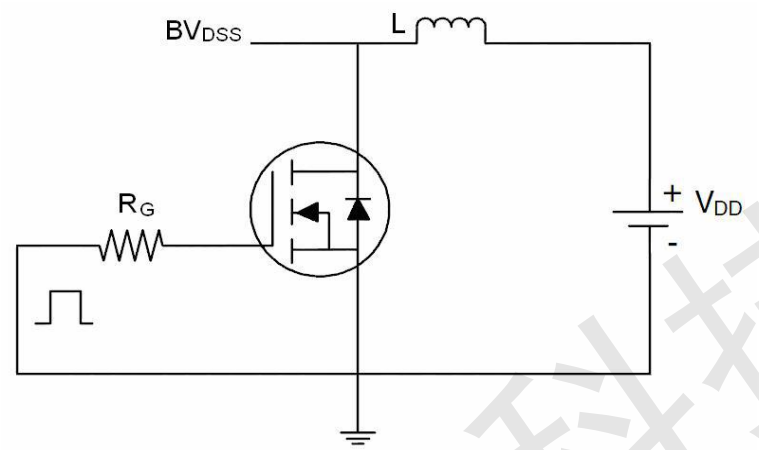
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. E_{AS} condition:Tj=25℃,V_{DD}=30V,V_G=10V,L=0.5mH,Rg=25Ω

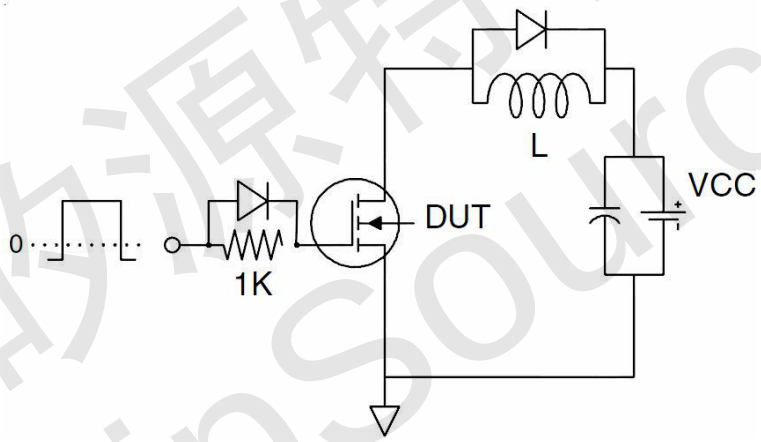
TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com

Test Circuit

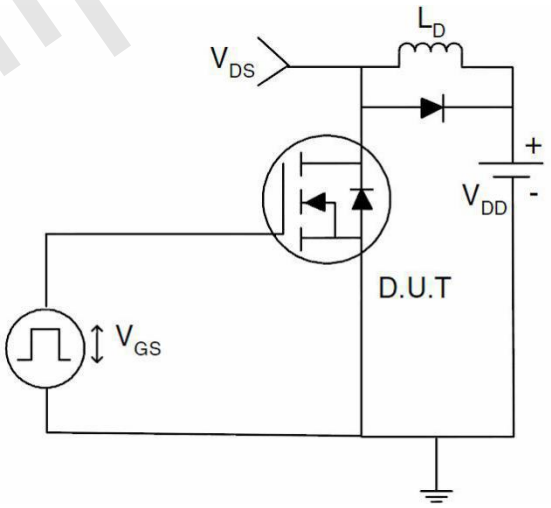
1) E_{AS} Test Circuits



2) Gate Charge Test Circuit:



3) Switch Time Test Circuit:



TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com

Typical Electrical and Thermal Characteristics (Curves)

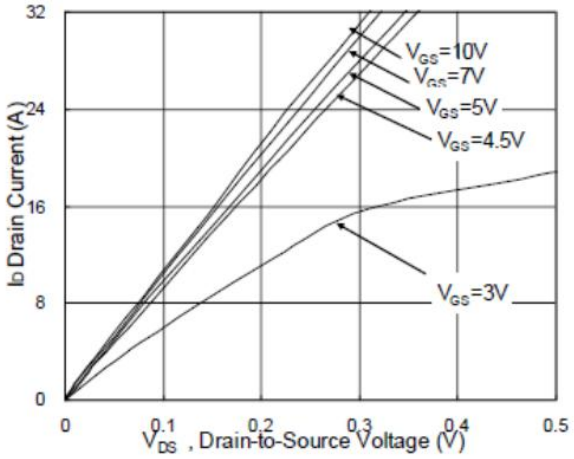


Figure 1 Output Characteristics

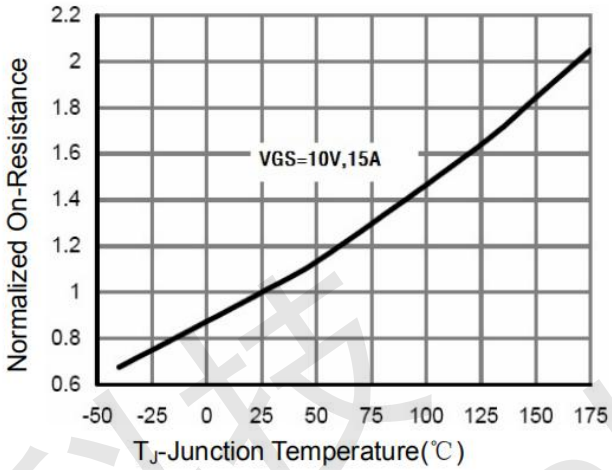


Figure 4 Rdson-JunctionTemperature

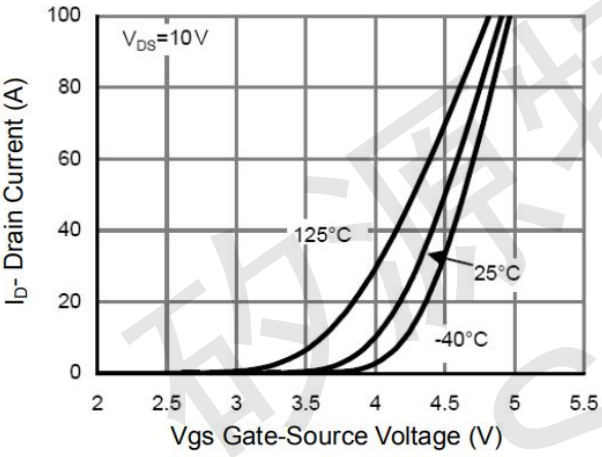


Figure 2 Transfer Characteristics

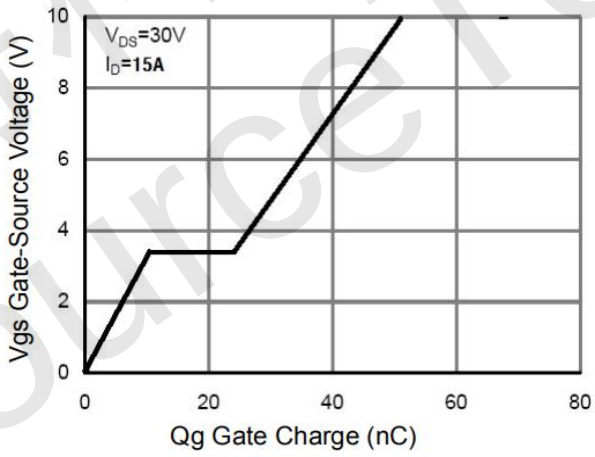


Figure 5 Gate Charge

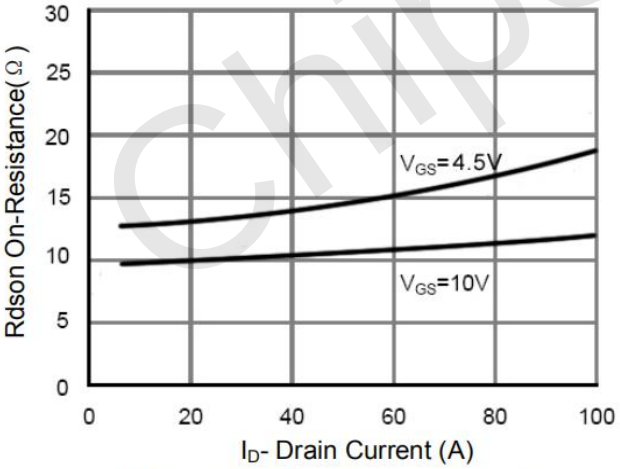


Figure 3 Rdson- Drain Current

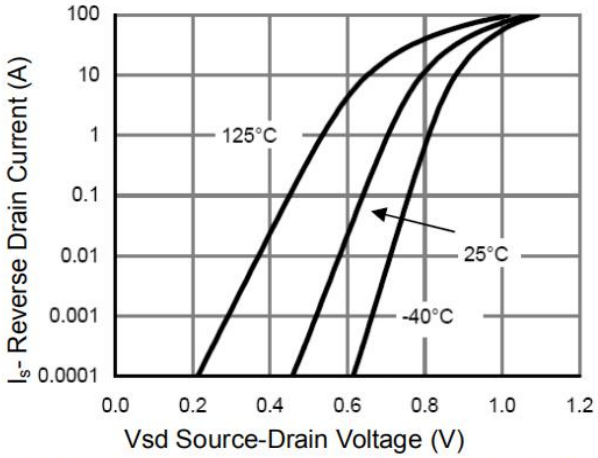


Figure 6 Source- Drain Diode Forward

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com

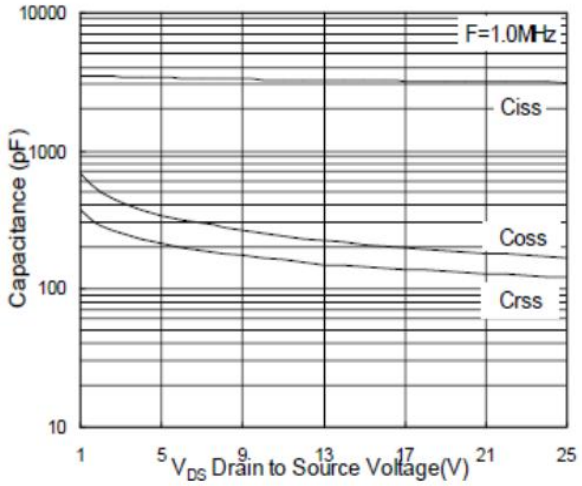


Figure 7 Capacitance vs Vds

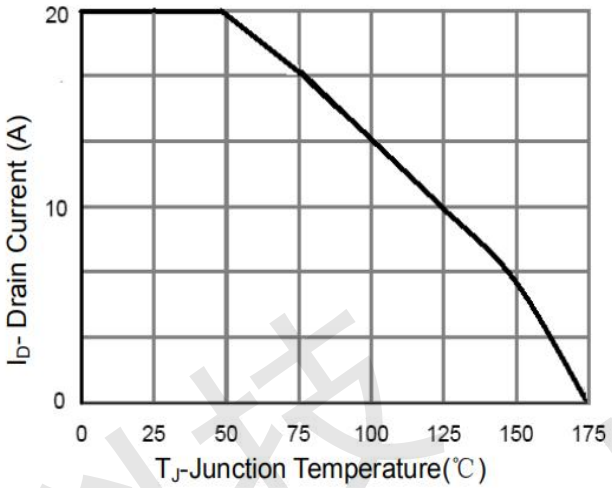


Figure 9 I_D De-rating

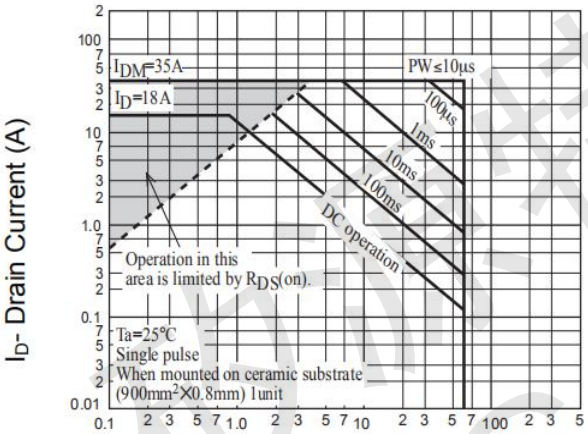


Figure 8 Safe Operation Area

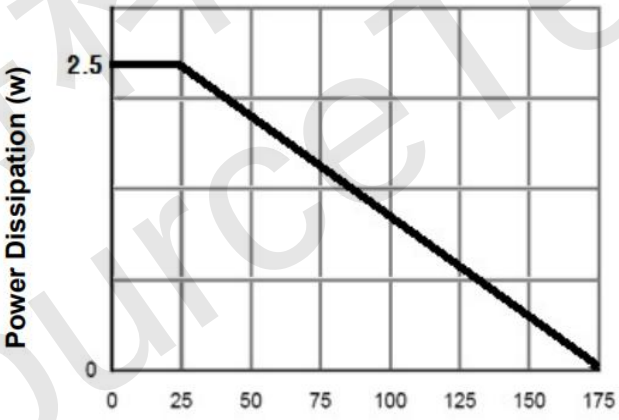


Figure 10 Power De-rating

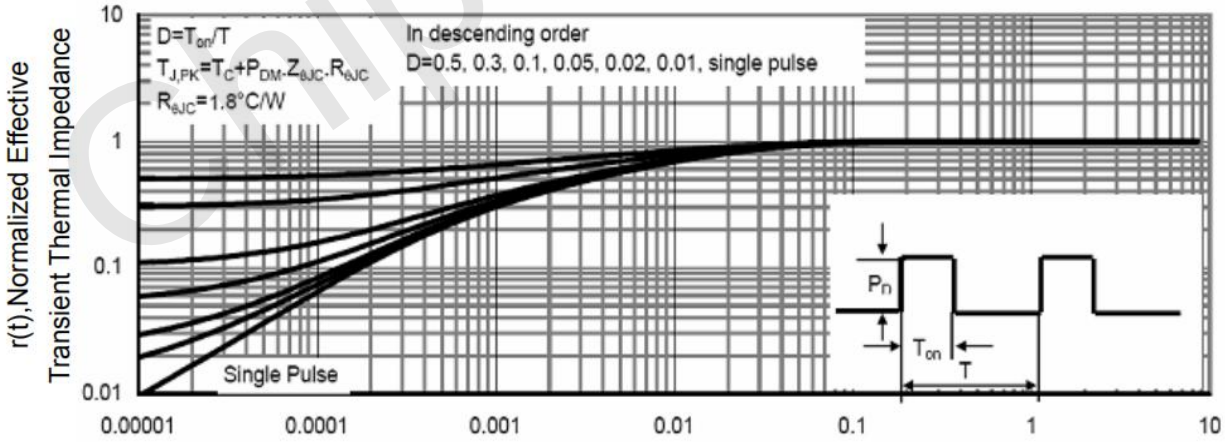
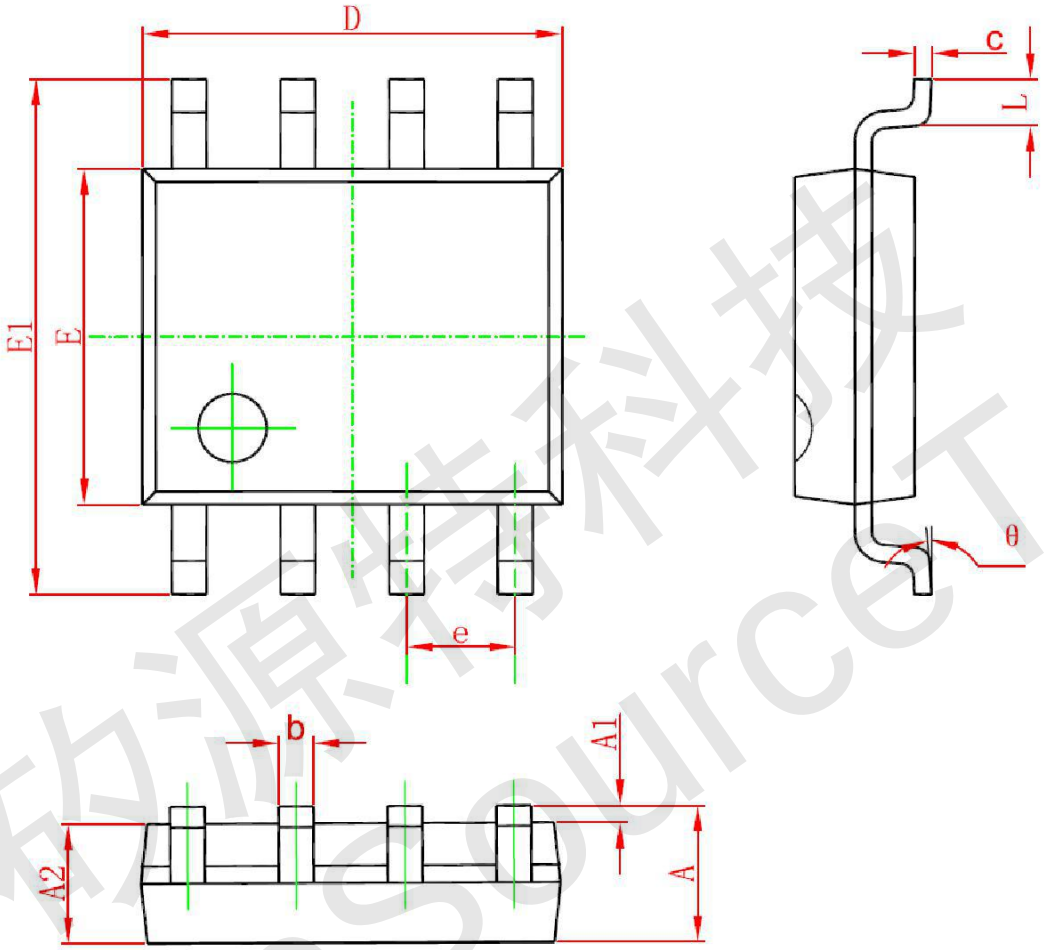


Figure 11 Normalized Maximum Transient Thermal Impedance

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com

SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TEL: +86-0755-27595155 27595165
FAX: +86-0755-27594792
WEB:Http://www.ChipSourceTek.com
E-mail: Tony.Wang@.ChipSourceTek.com InFo@ChipSourceTek.com