MX87

Ultra-Low Jitter Clock Synthesizer with Integrated Quartz Crystal Master Data Sheet

Features

- Generates Up to Six Differential or Single-Ended Outputs
- 85 fs Phase Jitter (typical) @ 156.25 MHz (12 kHz to 20 MHz)
- 83 fs Phase Jitter (typical) @ 312.5 MHz (12 kHz to 20 MHz)
- Twelve On-Chip Power Supply Regulators for Excellent Power Supply Noise Immunity: 75 dB
- Integrated Quartz Crystal for Superior Noise/Jitter Performance
- Independently Programmable Output Logics and Frequencies:
  - Output Logic: LVPECL, LVDS, HCSL, LVC-MOS
  - Available External Reference Input: 50 MHz to 875 MHz
- 2.5V to 3.3V Operating Power Supply
- Separate Output Power Supplies: Each Bank Can be at a Different Voltage Level (Two Banks of Three Outputs Each)
- Industrial Temperature Range: –40°C to +85°C
- Green, RoHS, and PFOS Compliant TQFN
- Industry Standard 48-Lead 7 mm x 7 mm x 1 mm TQFN Package
- Moisture Sensitivity Level (MSL): Level 1

Applications

- 10/40/100/400 Gigabit Ethernet (GMII)
- SONETSDH
- PCI Express Gen 1/2/3/4/5
- CPRI/OBSAI Wireless Base Station
- Fibre Channel
- HDMI/HDTV-4K/-8K
- DIMM (DDR2-3-4/AMB)

General Description

The MX87 series are a family of PLL clock synthesizers with an integrated quartz crystal that achieves ultra-low phase jitter (<90 fs_{RMS} typical). With up to six total outputs available and dividers on each output, this device can generate up to six different frequencies up to 875 MHz.

Each output can be programmed to any combination of LVPECL, LVDS, HCSL, or LVCMOS logic. For LVCMOS, however, only the true side of the channel is available.

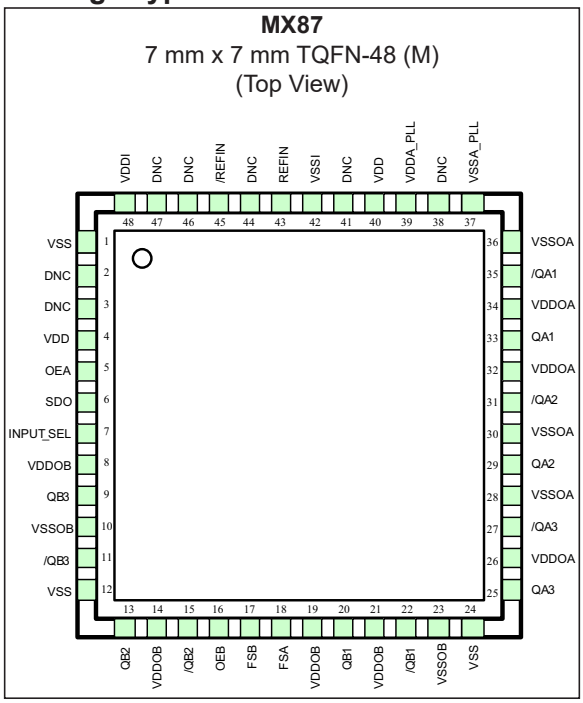
The MX87 is packaged in a standard 48-lead TQFN.

Package Type

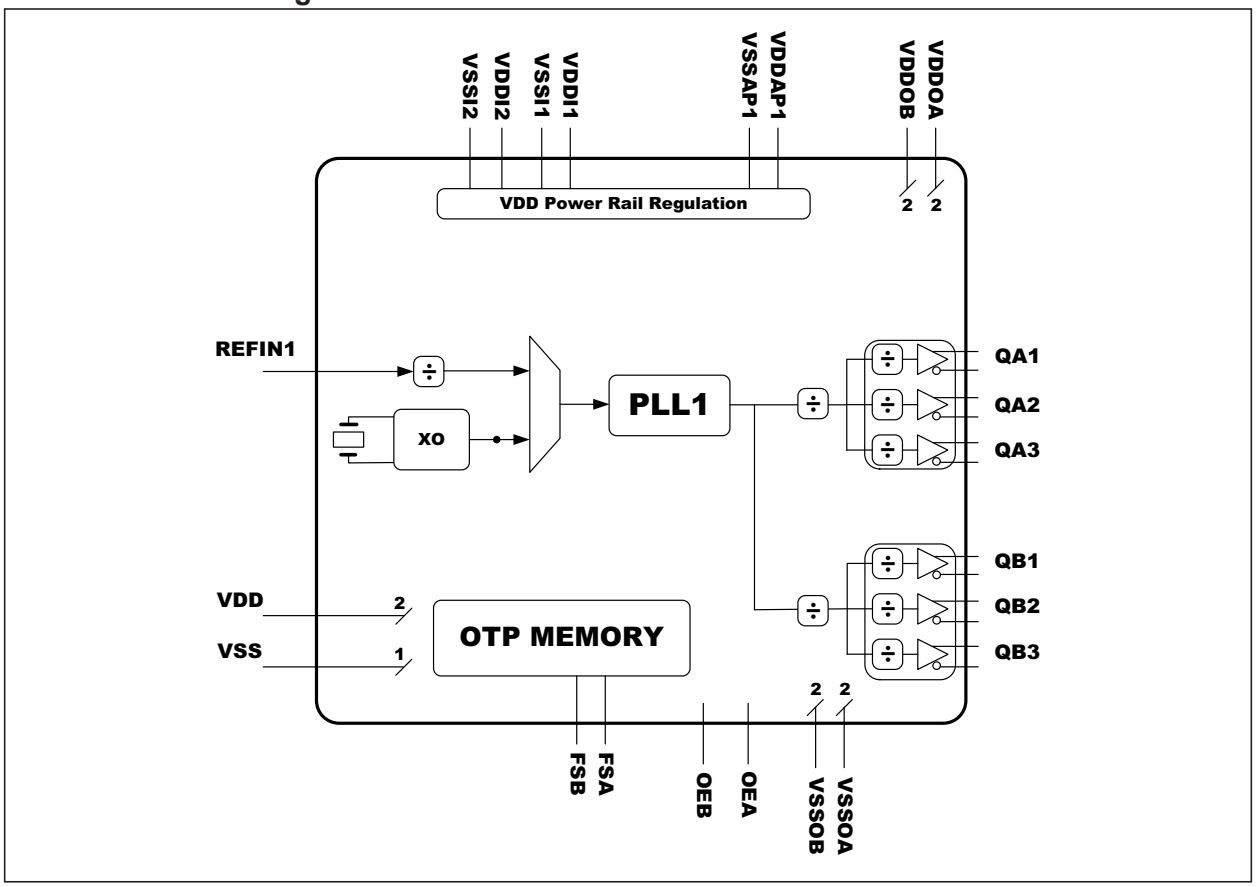
MX87

7 mm x 7 mm TQFN-48 (M)

(Top View)



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{DD}, V_{DDA}, V_{DDI}, V_{DDO})..... +4.6V
Input Voltage (V_{IN}) .....–0.5V to +4.6V
ESD Rating (Machine Model.....200V
ESD Rating (Human Body Model) .....2 kV

Operating Ratings ††

Supply Voltage (V_{DD}, V_{DDO}) .....+2.375V to +3.465V

† Notice: Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

†† Notice: The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated, typical values are for T_A = +25°C. The min. and max. values are for –40°C ≤ T_A ≤ +85°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Condition
Supply Voltage	V_{DD}, V_{DDO}	2.375	2.5	2.625	V	2.5V operation
		3.135	3.3	3.465		3.3V operation
Analog and I/O Supply	V_{DDI}	2.375	—	3.465	V	—
PLL Core	V_{DDA}	2.375	—	3.465	V	—
PLL Core Current Consumption	I_{DDA}	—	—	60	mA	—
Analog and I/O Current	I_{DDI}	—	—	20	mA	—
Output Stage Current Consumption	I_{DDO}	—	—	70	mA	Per output bank, unloaded
Miscellaneous Logic	I_{DD}	—	—	8	mA	—

LVPECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO} – 2V.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{DDO} – 1.35	V_{DDO} – 1.01	V_{DDO} – 0.8	V	50Ω to V_{DDO} – 2V
Output Low Voltage	V_{OL}	V_{DDO} – 2	V_{DDO} – 1.78	V_{DDO} – 1.6	V	50Ω to V_{DDO} – 2V
Peak-to-Peak Output Voltage	V_{SWING}	0.65	0.77	0.95	V	Figure 5-7

LVDS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 100Ω between Q and /Q.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Differential Output Voltage	V_{OD}	245	350	454	mV	Figure 5-7
Common Mode Voltage	V_{CM}	1.125	1.2	1.375	V	—
Output High Voltage	V_{OH}	1.248	1.375	1.602	V	—
Output Low Voltage	V_{OL}	0.898	1.025	1.252	V	—

HCSL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{SS}.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	660	700	850	mV	—
Output Low Voltage	V_{OL}	–150	0	27	mV	—
Crossing Point Voltage	V_{CROSS}	—	350	—	V	—

LVCMOS DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DDCORE} = V_{DD} = V_{DDO} = 3.3V ±5% or 2.5V ±5%, T_A = –40°C to +85°C, unless otherwise noted. R_L = 50Ω to V_{DDO}/2.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Output High Voltage	V_{OH}	V_{DD} – 0.8	—	—	V	Highest drive (default)
Output Low Voltage	V_{OL}	—	—	0.5	V	—
Input High Voltage	V_{IH}	V_{DD} – 0.7	—	V_{DD} + 0.3	V	—
Input Low Voltage	V_{IL}	V_{SS} – 0.3	—	0.3 x V_{DD}	V	—
Input High Current	I_{IH}	—	—	5	µA	V_{DD} = V_{IN} = 3.465V
Input Low Current	I_{IL}	–150	—	—	µA	V_{DD} = 3.465V, V_{IN} = 0V

REF_IN DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = 3.3V ±5% to 2.5V ±5%, T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input Common Mode Voltage	V_{CMR}	0.3	—	V_{DD} – 0.3	V	Note 1
Input Voltage Swing	V_{SWING}	0.2	—	—	V_{PP}	Note 1

Note 1: See the Input Selection section.

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{DD} = $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; V_{DD} = 3.3V ±5%, $V_{DDO1/2}$ = 3.3V ±5% or 2.5V ±5%; T_A = –40°C to +85°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Condition
Input Frequency (Note 1)	f_{IN}	12.5	—	875	MHz	Reference input
Output Frequency	f_{OUT}	12.5	—	875	MHz	LVPECL, LVDS, HCSL
		12.5	—	400		LVCMOS
Output Rise/Fall Time (Note 2)	t_r/t_f	85	135	350	ps	LVPECL output
		85	140	300		LVDS output
		175	200	400		HCSL output
		100	200	400		LVCMOS output (default drive)
Output Duty Cycle	ODC	45	50	55	%	All output frequencies
		48	50	52		<450 MHz output frequency
Input-to-Output Propagation Delay	t_{PD}	—	4	—	ns	Synthesizer mode
Output-to-Output Skew (Note 3)	t_{SKEW}	—	—	50	ps	Same output bank, (Note 4)
PLL Lock Time	t_{LOCK}	—	5	20	ms	Time from 90% V_{DD}
RMS Phase Jitter (Note 5, Note 6)	$t_{JIT(Ø)}$	—	85	—	fs	156.250 MHz, Integration range (12 kHz – 20 MHz)
		—	65	—		156.250 MHz, Integration range (1.875 MHz – 20 MHz)

Note 1: Available on REF_IN package versions only.

2: See Figure 5-7.

3: Output-to-output skew is defined as skew between outputs at the same supply voltage and with equal load conditions. It is measured at the output differential crossing points.

4: Output-to-output skew is only defined for outputs in the same PLL bank [A:B, C:D] with the same output logic type setting.

5: All phase noise measurements were taken with an Agilent 5052B phase noise system.

6: If using an external reference input, use a low phase noise source. The output phase noise will follow the input source phase noise up to about 1.5 MHz.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Case Temperature	—	—	—	+115	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 20 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances (Note 1)						
Thermal Resistance, 7x7 TQFN-48Ld	θ_{JC}	—	26	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +85°C rating. Sustained junction temperatures above +85°C can impact the device reliability.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Type	Pin Level	Description
33	QA1	O, (DIF/SE)	LVPECL LVDS HCSL LVCMOS (Q only)	Differential/Single-Ended Clock Output (LVCMOS)
35	/QA1			
29	QA2			
31	/QA2			
25	QA3			
27	/QA3			
20	QB1			
22	/QB1			
13	QB2			
15	/QB2			
9	QB3			
11	/QB3			
18	FSA	I, (SE)	LVCMOS	Frequency Select, on-chip 75 kΩ pull-up 1 = Primary Selection 0 = Secondary Selection
17	FSB			
4	V_{DD}	PWR	—	Power Supply
40				
26	V_{DDOA}	PWR	—	Power Supply for Outputs QA
32				
34				
8	V_{DDOB}	PWR	—	Power Supply for Outputs QB
14				
19				
21				
39	V_{DDAPLL}	PWR	—	Analog Power Supply for PLL
48	V_{DDI}	PWR	—	Power Supply for Reference Input Circuits and Crystal
42	V_{SSI}	PWR	—	Ground for Reference Input Circuits and Crystal Oscillator
1	GND-V_{SS} (Exposed Pad)	PWR	—	Power Supply Ground. The exposed pad must be connected to the V_{SS} ground plane.
12				
21				
ePAD				
28	V_{SSOA}	PWR	—	Ground Return Path for the Bank A Output Drivers
30				
36				
10	V_{SSOB}	PWR	—	Ground Return Path for the Bank B Output Drivers
23				
5	OEA1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QA1/2/3 disable to tri-state 0 = Disabled 1 = Enabled, on-chip 75 kΩ pull-up
16	OEB1/2/3	I, (SE)	LVCMOS	Output Enable, Outputs QB1/2/3 disable to tri-state 0 = Disabled 1 = Enabled, on-chip 75 kΩ pull-up

TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin Number	Pin Name	Pin Type	Pin Level	Description
43	REFIN1	I, (Diff/SE)	LVPECL, LVDS, HCSL, LVCMOS	Reference Clock Input 1
45	/REFIN1			
38	NC	—	—	No Connect No internal connections to the ASIC are made
41				
44				
46				
47				

Truth Tables

TABLE 2-2: OUTPUT ENABLE

OEA	OEB	Output
0	1	3 QA outputs tri-state
1	0	3 QB outputs tri-state

TABLE 2-3: FREQUENCY SELECT PIN

FSA	FSB	Output Frequency
0	1	QA Outputs: Secondary output dividers QB Outputs: Primary output dividers
1	0	QA Outputs: Primary output dividers QB Outputs: Secondary output dividers
1	1	QA Outputs: Primary output dividers QB Outputs: Primary output dividers
0	0	QA Outputs: Secondary output dividers QB Outputs: Secondary output dividers

3.0 KEY PROGRAMMABLE PARAMETERS

3.1 Frequency Settings for One PLL and One Output Bank

The REF input frequency can be from a reference clock input. The REF input frequency range is 12.5 MHz to 875 MHz.

The VCO has a range of 2875 MHz to 3540 MHz.

Counters M and P0 have a range of 4 to 259.

Counters P1, P2, and P3 have a range of 1 to 16.

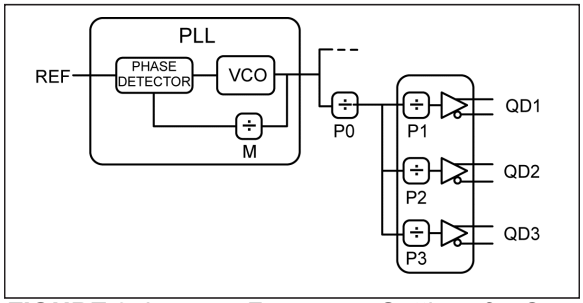


FIGURE 3-1: *Frequency Settings for One PLL and One Output Bank.*

EQUATION 3-1:

$$f_{VCO} = REF \times M$$

EQUATION 3-2:

$$QD1 = f_{VCO} \div (P0 \times P1)$$

EQUATION 3-3:

$$QD2 = f_{VCO} \div (P0 \times P2)$$

EQUATION 3-4:

$$QD3 = f_{VCO} \div (P0 \times P3)$$

3.2 Output Logic Programming

Available output logic types are LVPECL, LVDS, HCSL, and LVCMOS.

Each output can be programmed individually to one of the four logic types.

All logic types are differential except LVCMOS. For LVCMOS, only the true channel of the output pair is enabled, and the complementary channel is disabled. With LVCMOS there is also an output drive setting. There is one setting for all LVCMOS outputs, so all LVCMOS outputs will have the same drive strength.

Unused outputs are disabled to high impedance.

3.3 Input Selection

The reference input can be programmed to be either the crystal or an external reference clock.

The crystal oscillator circuit has capacitors on the IC so external capacitors are not required.

The reference inputs can be differential or single-ended and require only a small amplitude signal, >200 mV, to operate, but a higher level, ~1.5V to 2.5V, will give optimum jitter performance.

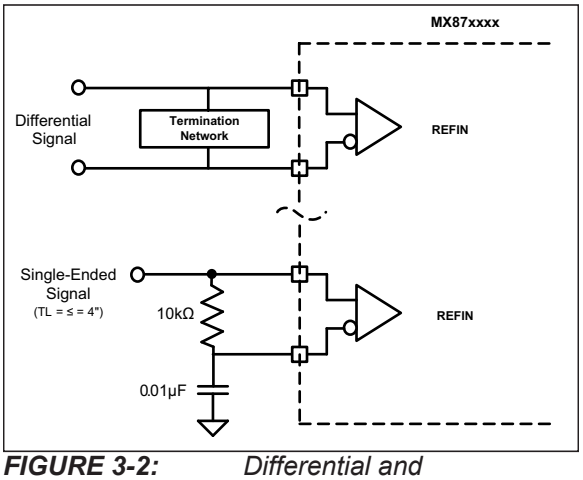


FIGURE 3-2: *Differential and Single-Ended Options.*

The single-ended reference signal input can be LVCMOS, but smaller amplitudes like >800 mV_{PP} clipped sine wave from a TCXO will also work.

3.4 Frequency Select Programming

Each of the four output banks has a frequency select pin. For each bank, two P0, P1, P2, and P3 counter values can be programmed, a primary and a secondary value. The frequency select pin toggles between the two values assigned to each counter, changing the output frequencies.

4.0 APPLICATION INFORMATION

4.1 Input Reference

When operating with the crystal input reference, do not apply an active switching signal to REF_IN.

4.2 Output Traces

Design the output signal traces according to the output logic requirements, terminations, etc. These are high edge rate signals so care must be taken in the PCB layout/traces, use best SI practices. If LVCMOS is unterminated, add a 30Ω resistor in series with the output as close as possible to the synthesizer output pin and start a 50Ω trace on the other side of the resistor.

For differential traces you can either use a differential design or two separate 50Ω traces. For EMI reasons, it is better to use a balanced differential transmission line design.

LVDS can be AC-coupled or DC-coupled to its termination.

5.0 POWER SUPPLY FILTERING RECOMMENDATIONS

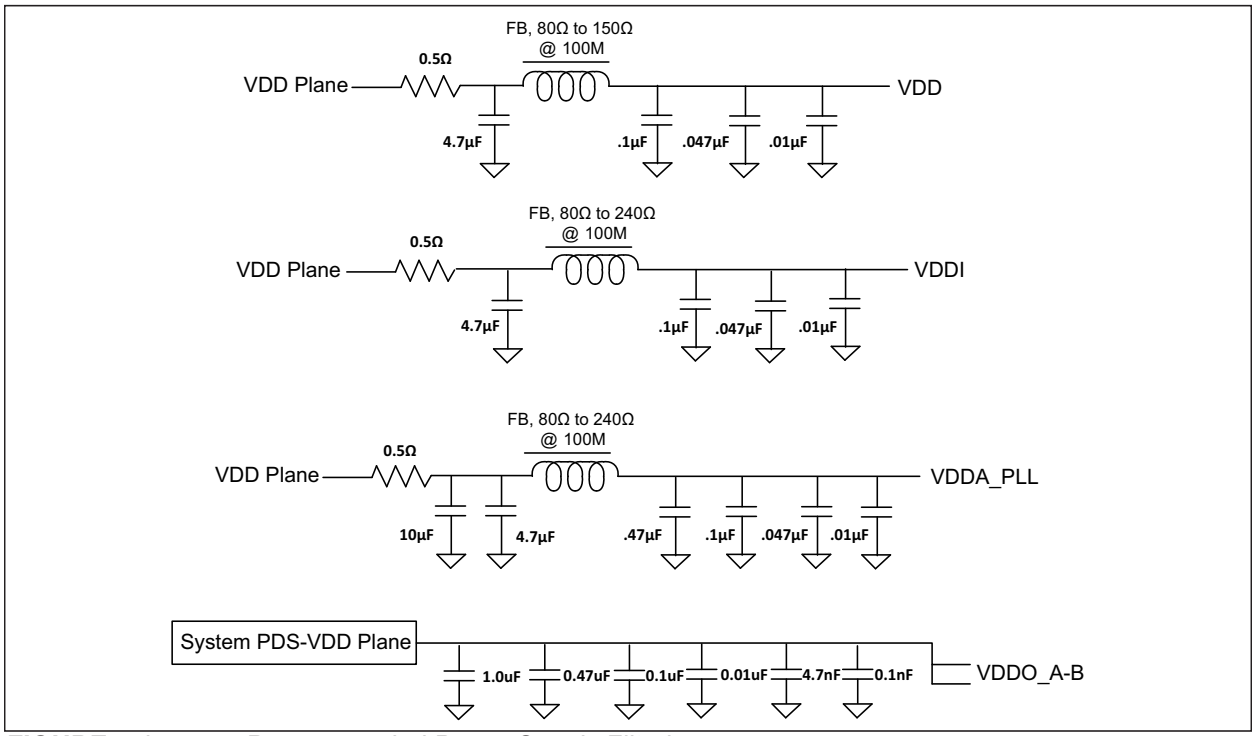


FIGURE 5-1: *Recommended Power Supply Filtering.*

- Use the power supply filtering shown in Figure 5-1 for V_{DDAPLL} and V_{DDI}.
- Connect VDDO and VDD pins directly into their power plane or power paddle. Use lowest inductance structures possible.
- Connect all VSS pins directly to the ground power plane.
- Recommended ferrite bead properties are 80Ω to 240Ω impedance and >250 mA saturation current.
- To improve power supply filtering beyond what a ferrite bead can provide, the Ripple Blocker™ provides a solution. MIC94300 or MIC94310 are recommended parts. The filter circuit with Ripple Blocker is shown in Figure 5-2 and can be used along with any of the above V_{DD} sections except V_{DDO}.

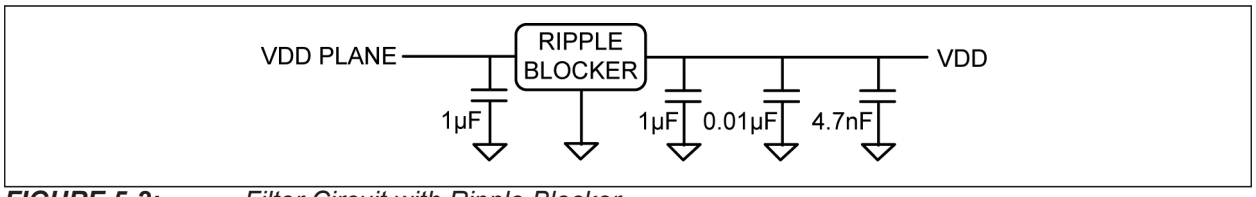


FIGURE 5-2: *Filter Circuit with Ripple Blocker.*

FIGURES AND CIRCUITS

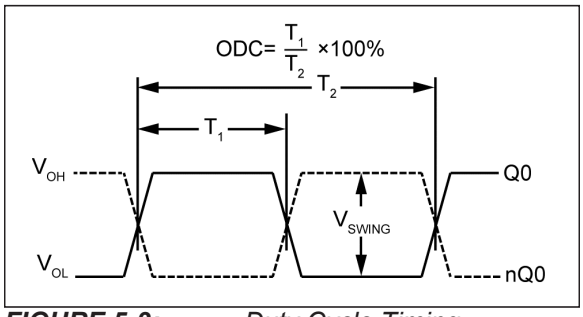


FIGURE 5-3: *Duty Cycle Timing.*

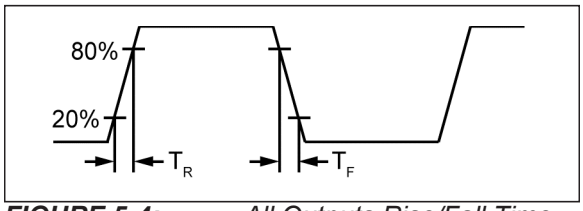


FIGURE 5-4: *All Outputs Rise/Fall Time.*

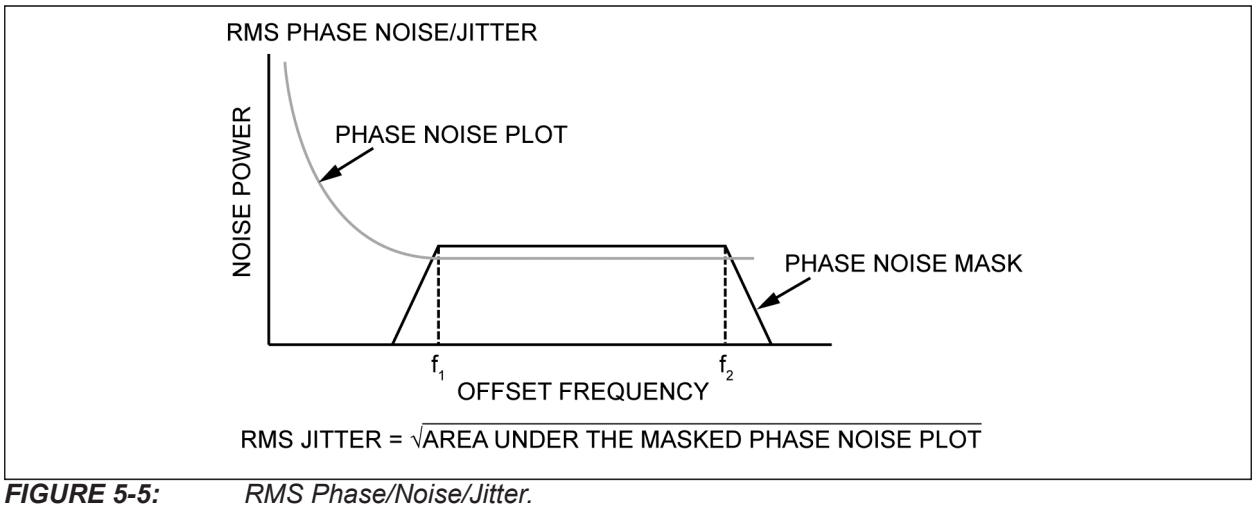


FIGURE 5-5: *RMS Phase/Noise/Jitter.*

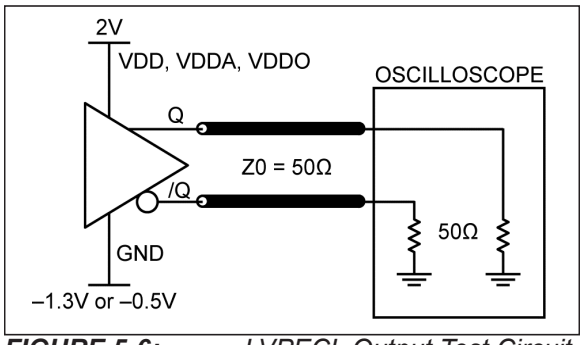


FIGURE 5-6: *LVPECL Output Test Circuit.*

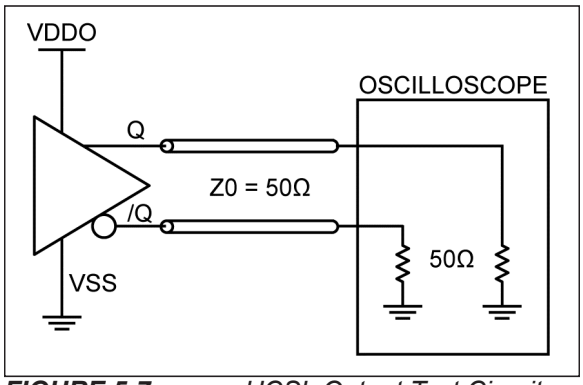


FIGURE 5-7: *HCSL Output Test Circuit.*

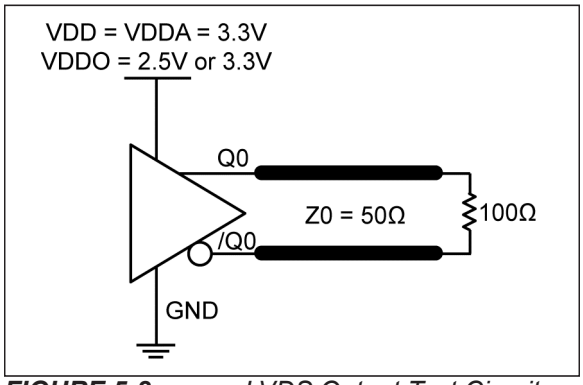


FIGURE 5-8: *LVDS Output Test Circuit.*

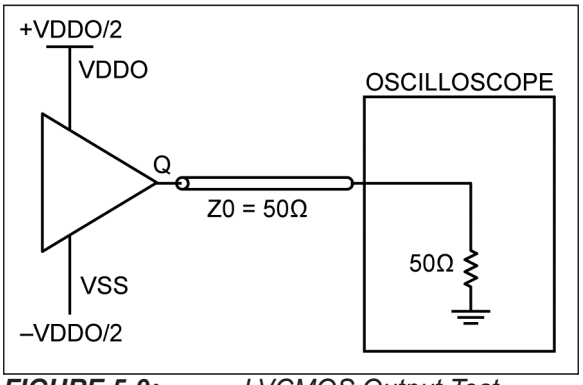


FIGURE 5-9: *LVCMOS Output Test Circuit.*

HCSL Source Terminated per JESD8-18A

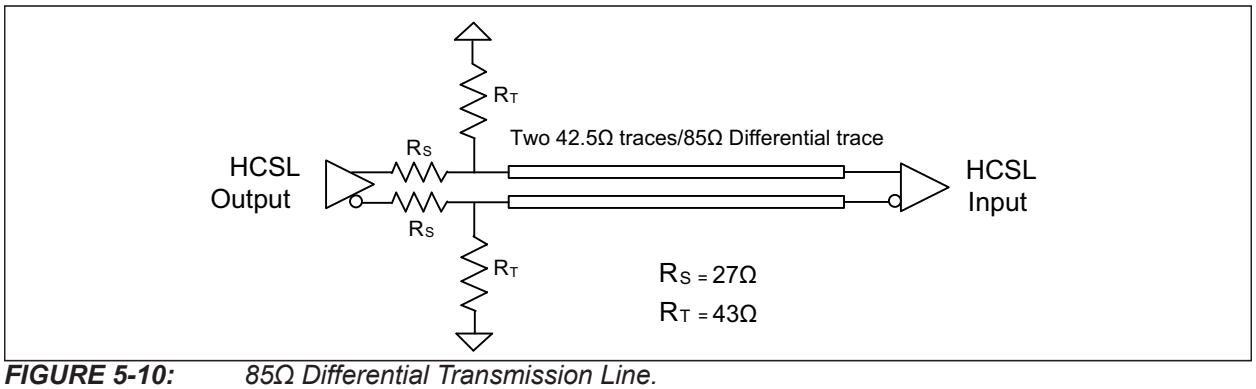


FIGURE 5-10: *85Ω Differential Transmission Line.*

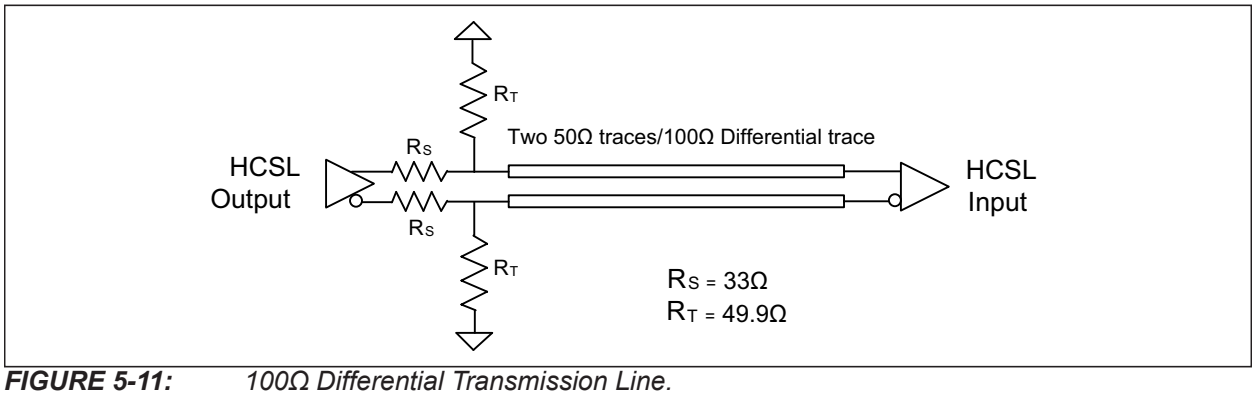


FIGURE 5-11: *100Ω Differential Transmission Line.*

6.0 PHASE NOISE PERFORMANCE

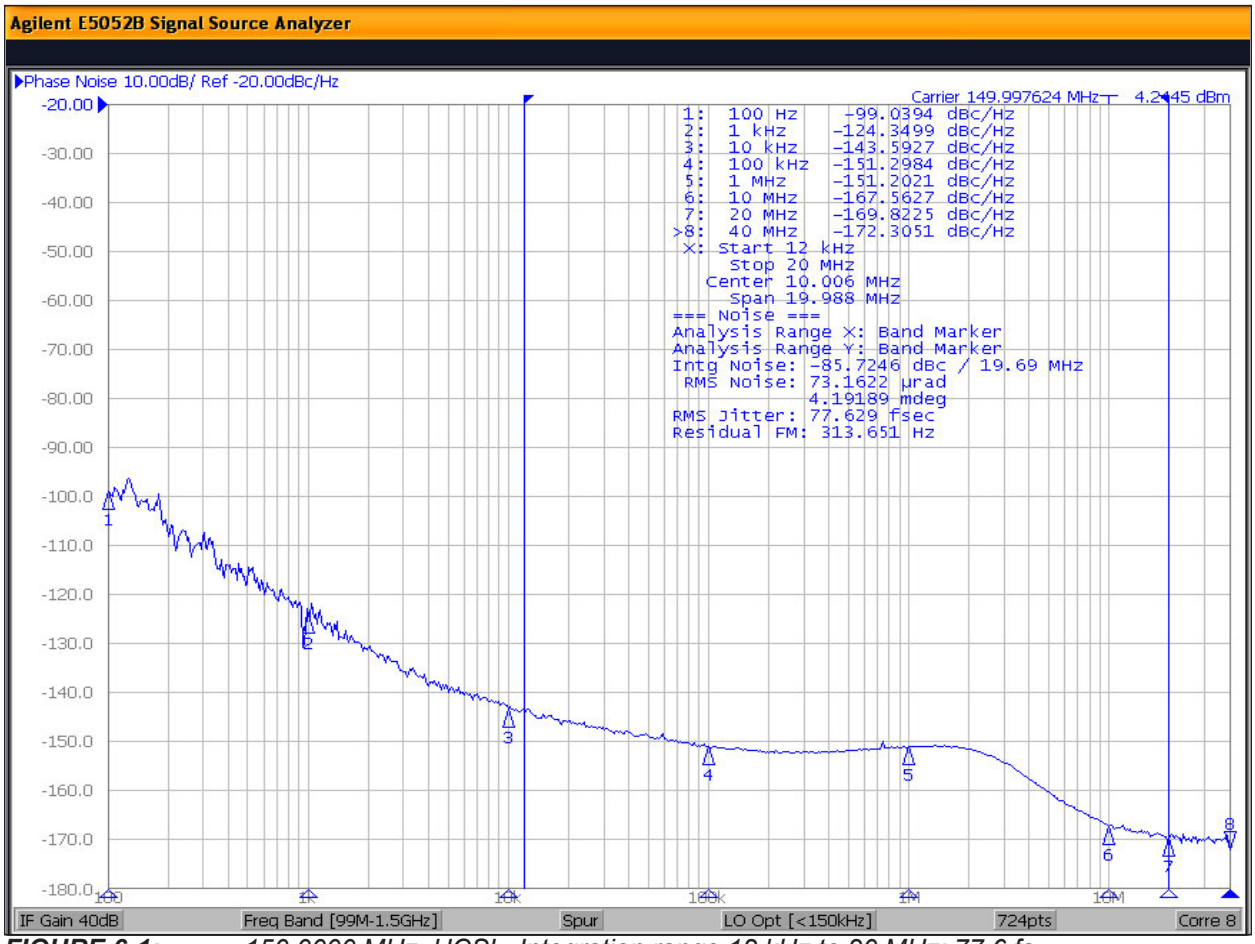


FIGURE 6-1: *150.0000 MHz, HCSL, Integration range 12 kHz to 20 MHz: 77.6 fs_{RMS}.*

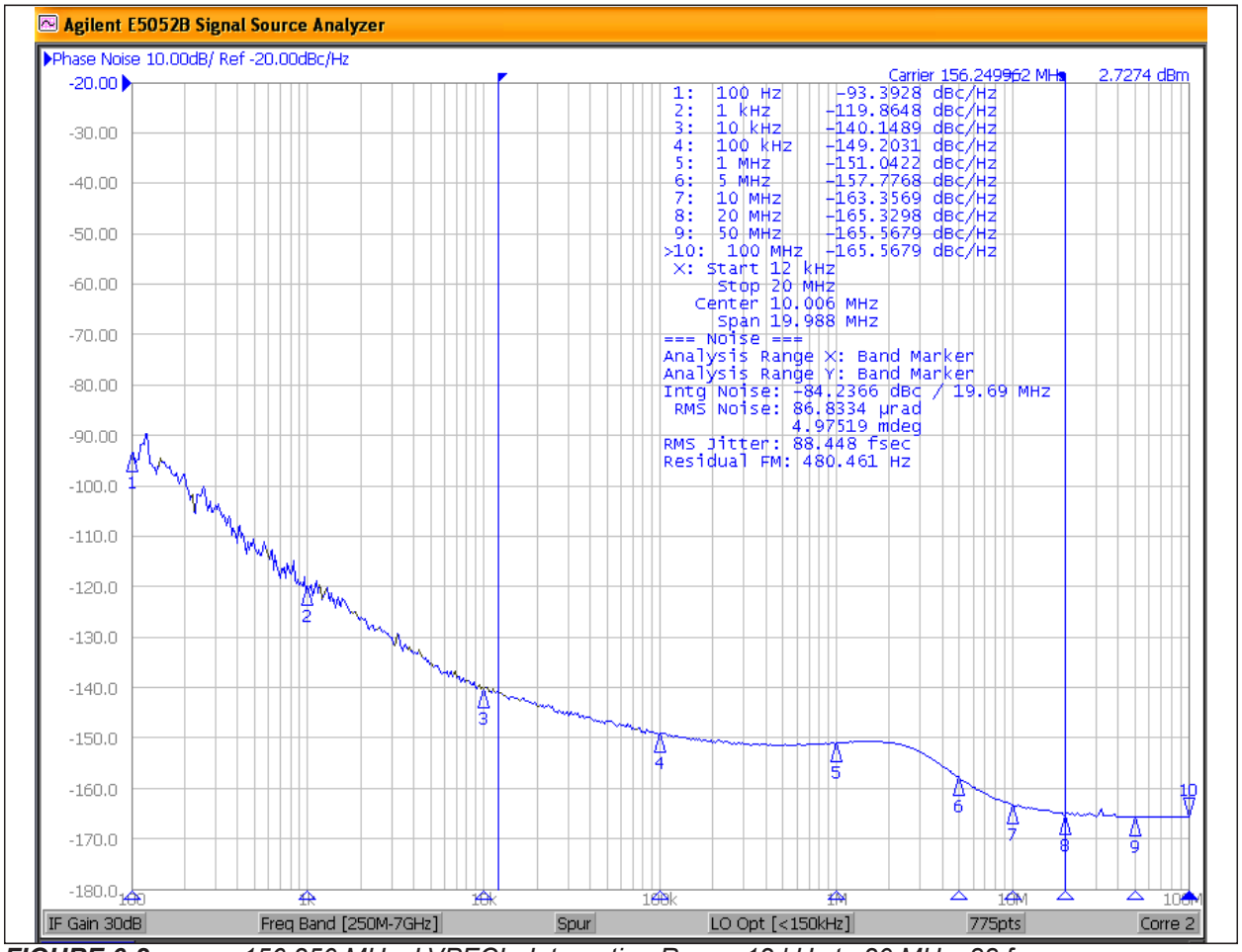


FIGURE 6-2: *156.250 MHz, LVPECL, Integration Range 12 kHz to 20 MHz: 88 fs_{RMS}.*

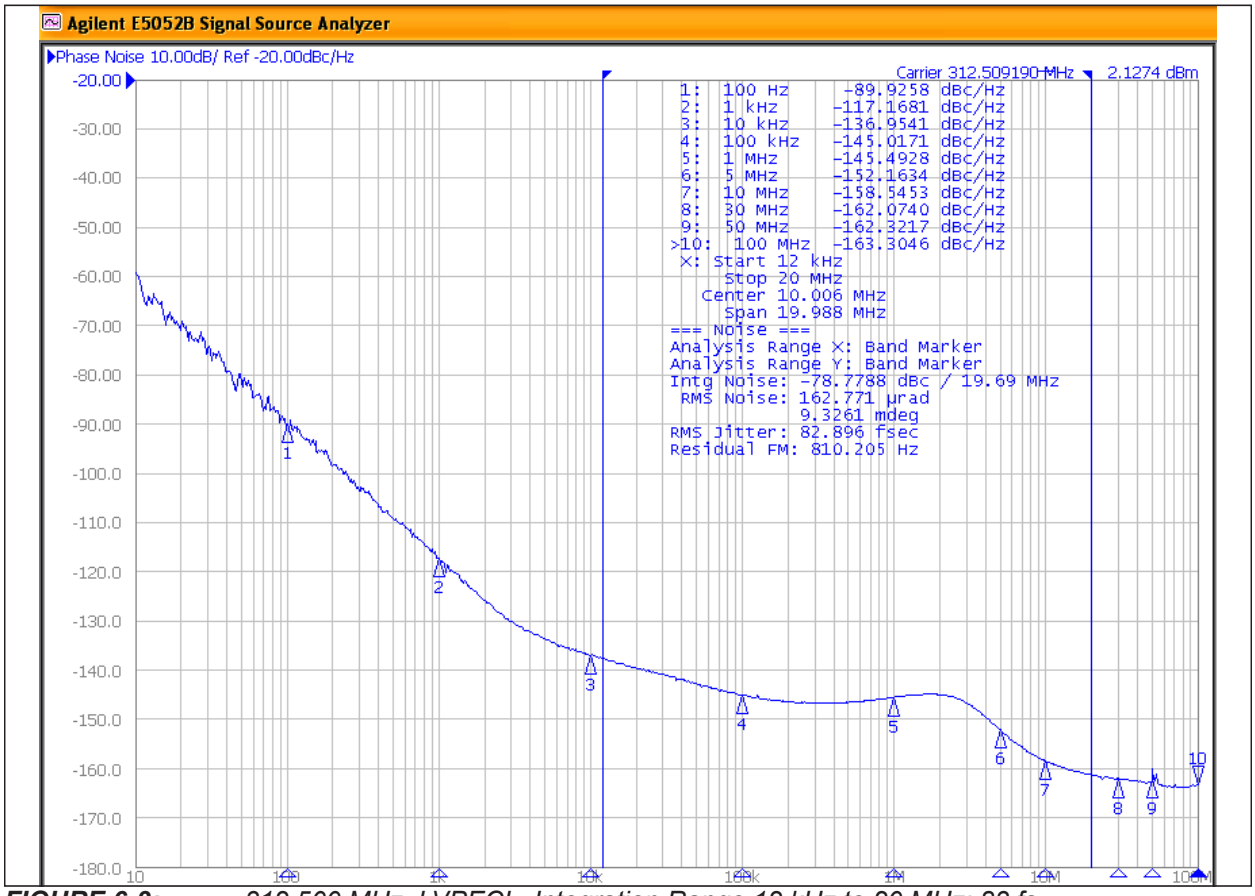


FIGURE 6-3: *312.500 MHz, LVPECL, Integration Range 12 kHz to 20 MHz: 83 fs_{RMS}.*

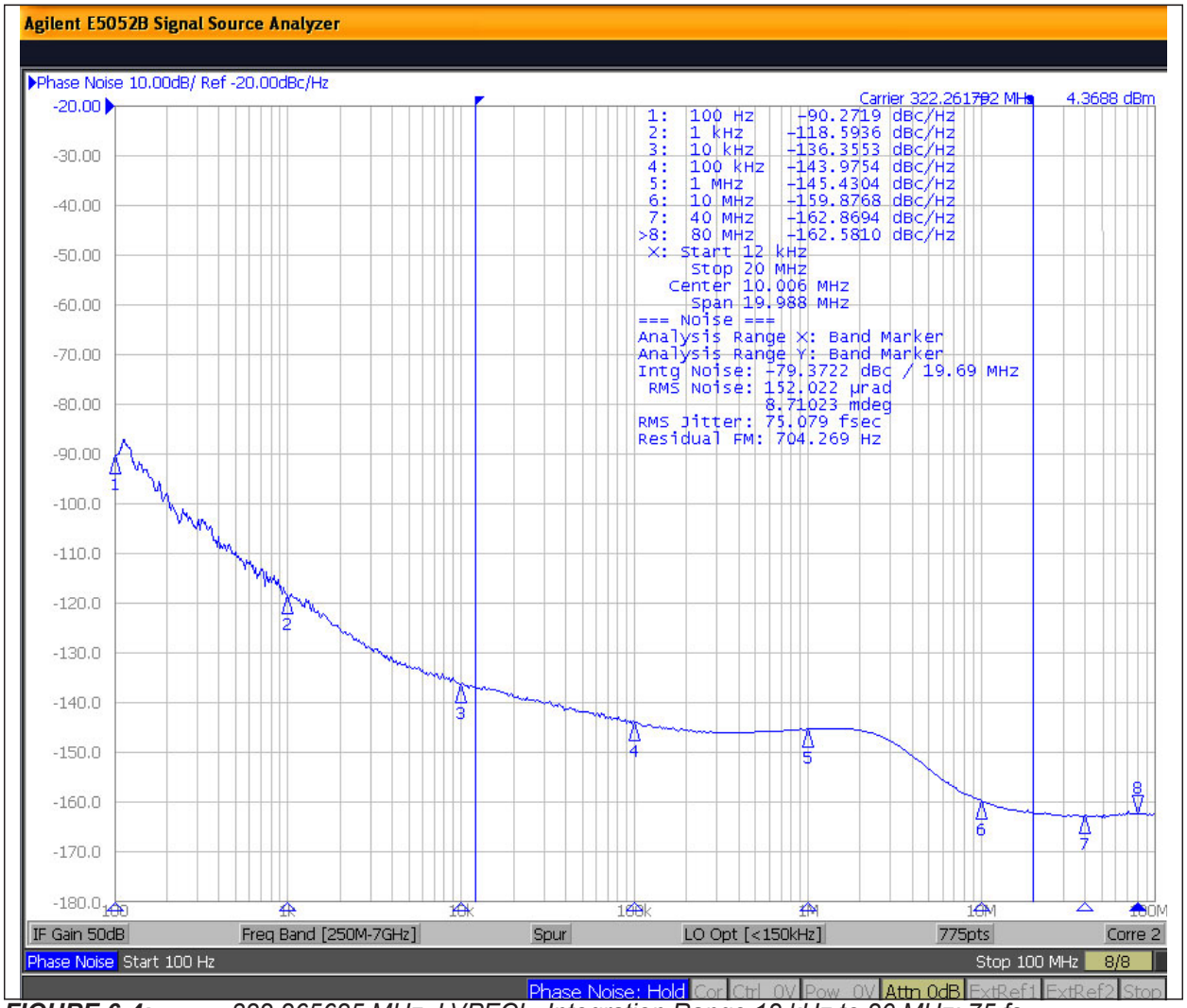


FIGURE 6-4: *322.265625 MHz, LVPECL, Integration Range 12 kHz to 20 MHz: 75 fs_{RMS}.*

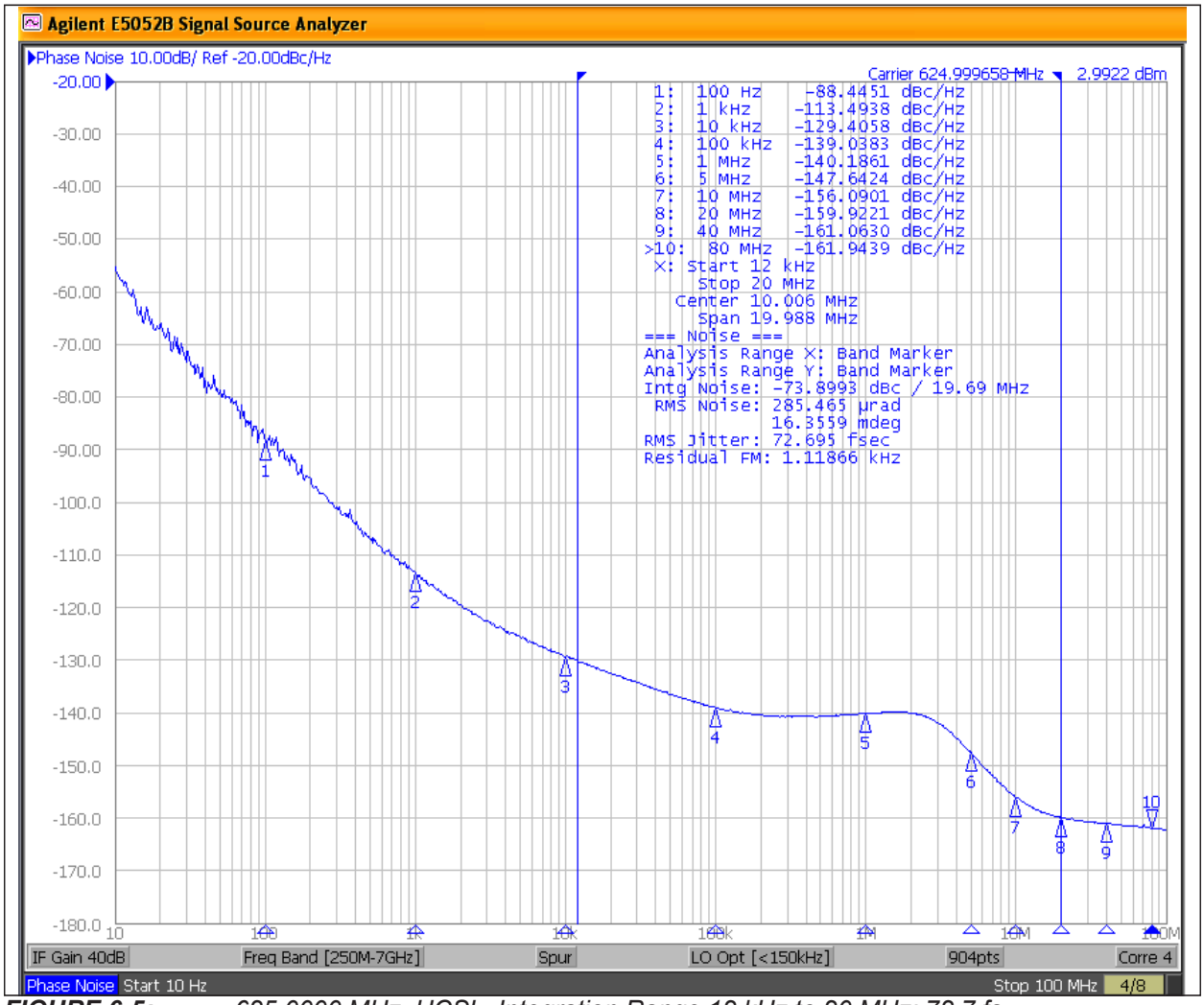


FIGURE 6-5: *625.0000 MHz, HCSL, Integration Range 12 kHz to 20 MHz: 72.7 fs_{RMS}.*

STANDARD BASE MODULES

Use the Clockworks® Configurator to generate a valid part number. Visit http://clockworks.microchip.com/timing/ to configure a part to your specifications.

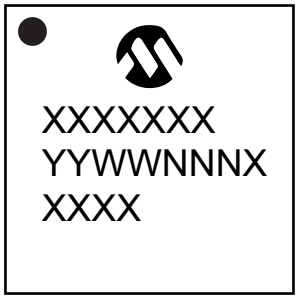
TABLE 6-1: FREQUENCY TABLE

Part Number	Base Frequency
MX875BB0000	50.000000 MHz
MX875CB0000	52.000000 MHz
MX875AB0000	52.083333 MHz
MX875DB0000	51.840000 MHz
MX875EB0000	53.710937 MHz
MX876BB0000	62.500000 MHz
MX876AB0000	64.000000 MHz
MX876CB0000	66.666666 MHz

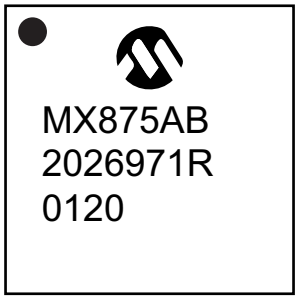
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

48-Lead TQFN*



Example

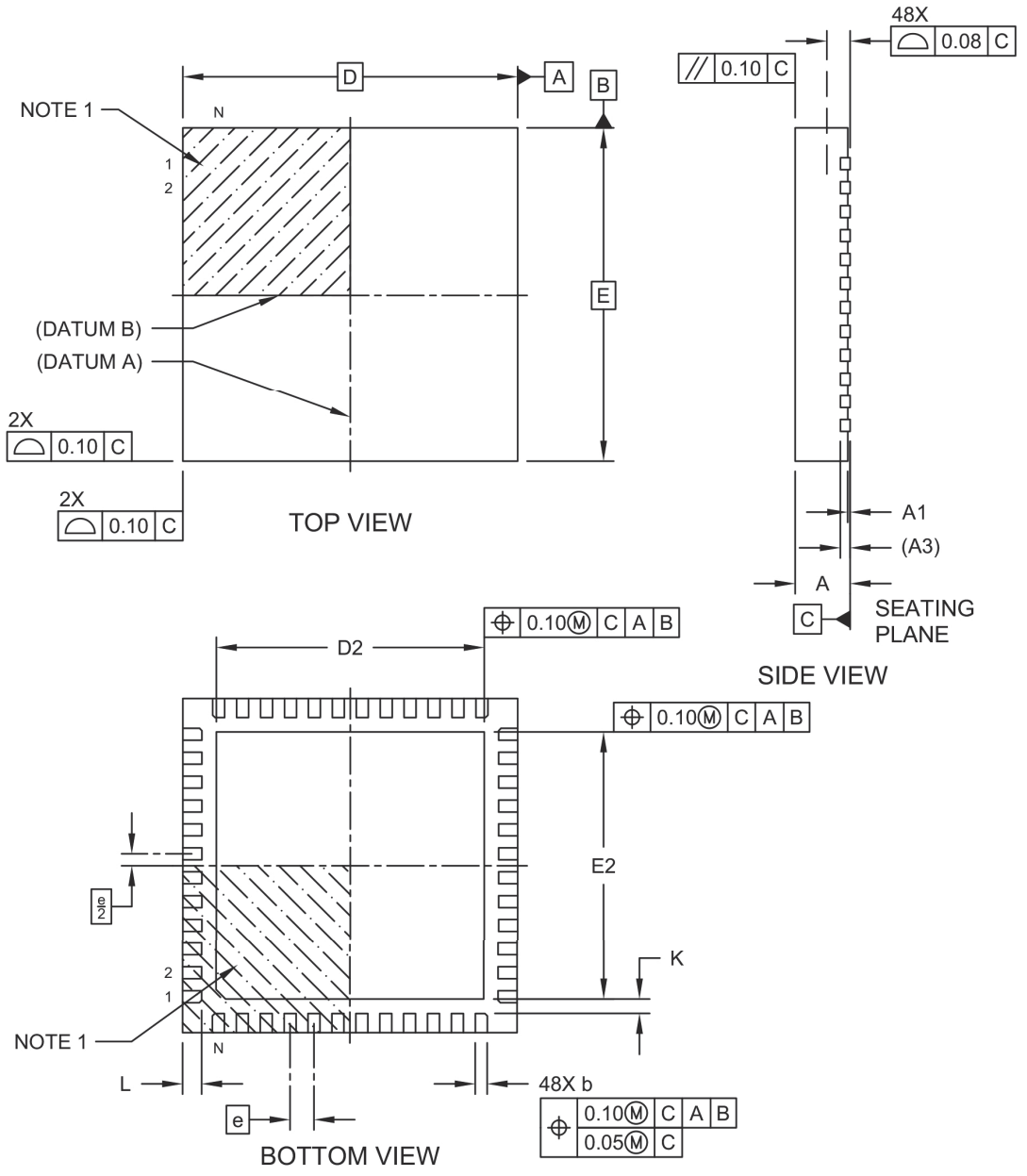


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	XXXX	Part number generated by ClockWorks Configurator (eg: 0120)
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

48-Lead TQFN 7 mm x 7 mm Package Outline and Recommended Land Pattern

48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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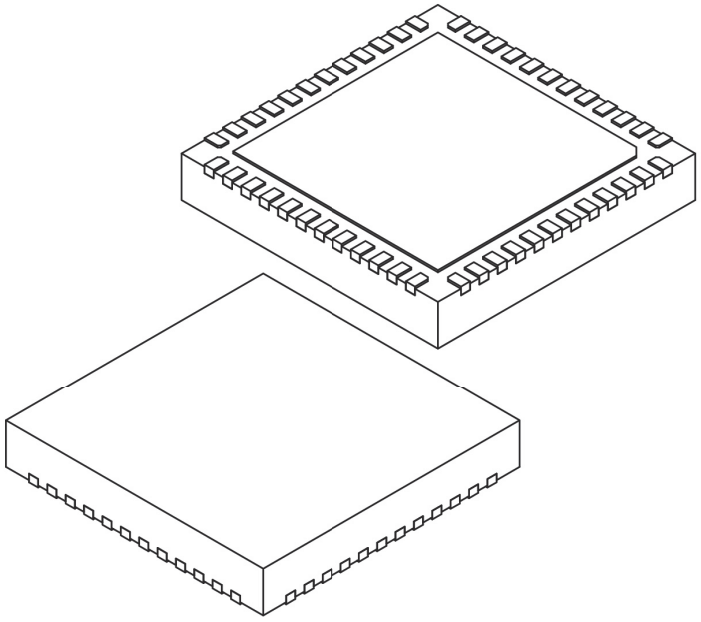
48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		48	
Pitch	e		0.50 BSC	
Overall Height	A	1.05	1.10	1.15
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		7.00 BSC	
Exposed Pad Length	D2	5.50	5.60	5.70
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	5.50	5.60	5.70
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

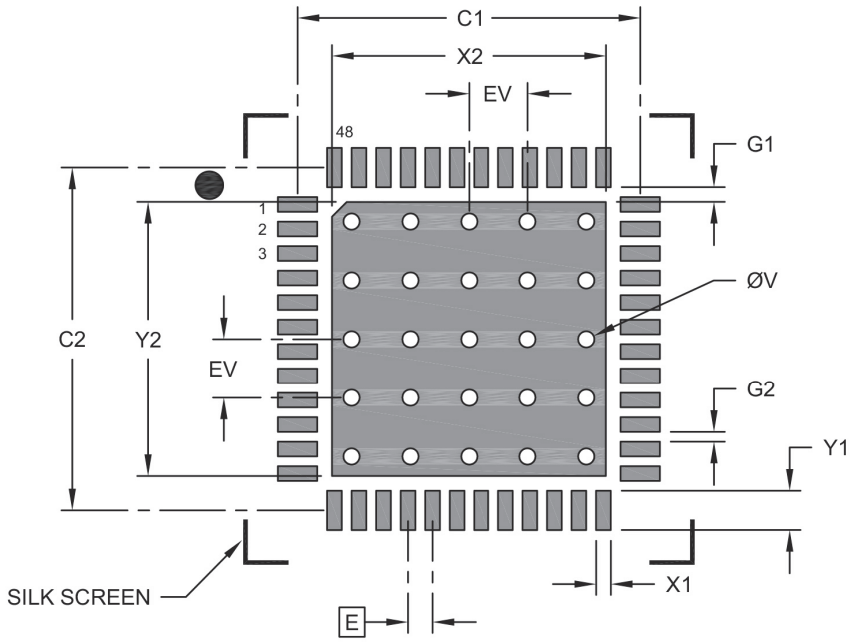
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-466 Rev A Sheet 1 of 2

48-Lead Thin Plastic Quad Flat, No Lead Package (KUX) - 7x7x1.15 mm Body [TQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Center Pad Width	X2			5.60
Center Pad Length	Y2			5.60
Contact Pad Spacing	C1		7.00	
Contact Pad Spacing	C2		7.00	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			0.80
Contact Pad to Center Pad (X48)	G1	0.20		
Contact Pad to Contact Pad (X44)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2466 Rev A

APPENDIX A: REVISION HISTORY

Revision A (April 2020)

- Initial release of MX87 as Microchip data sheet DS20006343A.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	X	XXXX	X	X	X	X
Device	Base Frequency	Stability	Unique Part Number	Voltage Option	Package	Temperature Range	Media Type

Device:	MX87:		Ultra-Low Jitter Clock Synthesizer with Integrated Quartz Crystal
Base Frequency:	5A	=	52.083333 MHz
	5B	=	50 MHz
	5C	=	52 MHz
	5D	=	51.84 MHz
	5E	=	53.710937 MHz
	6A	=	64 MHz
	6B	=	62.5 MHz
	6C	=	66.666666 MHz
Stability:	A	=	±20/10 ppm
	B	=	±50/20 ppm
	C	=	±50/50 ppm
	D	=	±15/10 ppm –10/+75C
	E	=	±25/15 ppm
	G	=	±20/15 ppm +75C
	H	=	±20/10 ppm –10/+75C
Unique Part Number:	XXXX	=	Generated by ClockWorks Configurator
Voltage Option:	U	=	2.5V/3.3V
Package:	M	=	7 mm x 7 mm 48-Lead TQFN
Temperature Range:	G	=	–40°C to 85°C (NiPdAu Lead-Free)
	Y	=	–40°C to 85°C (Matte-Sn Lead-Free)
Media Type:	<blank>	=	43/Tube
	R	=	1,000/Reel

Note 1: The TQFN package has six (6) outputs, Output Enable control, and Frequency Select control. Use the web tool at http://clockworks.microchip.com/timing/ to determine your desired configuration.

Examples:

a) MX875BBxxxUMG: MX87, 50 MHz Base Frequency, ±50/20 ppm Stability, Unique Part Number, 2.5V/3.3V Supply Voltage, 7 mm x 7 mm 48-Lead TQFN, –40°C to +85°C (NiPdAu) Temperature Range, 43/Tube

b) MX875CCxxxxUMGR: MX87, 52 MHz Base Frequency, ±50/50 ppm Stability, Unique Part Number, 2.5V/3.3V Supply Voltage, 7 mm x 7 mm 48-Lead TQFN, –40°C to +85°C (NiPdAu) Temperature Range, 1000/Reel

c) MX875DExxxxUMY: MX87, 51.84 MHz Base Freq., ±25/15 ppm Stability, Unique, Part Number, 2.5V/3.3V Supply Voltage, 7 mm x 7 mm 48-Lead TQFN, –40°C to +85°C (Matte-Sn) Temperature Range, 43/Tube

d) MX876BAxxxxUMYR: MX87, 62.5 MHz Base Freq., ±20/10 ppm Stability, Unique Part Number, 2.5V/3.3V Supply Voltage, 7 mm x 7 mm 48-Lead TQFN, –40°C to +85°C (Matte-Sn) Temperature Range, 1000/Reel

Note: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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